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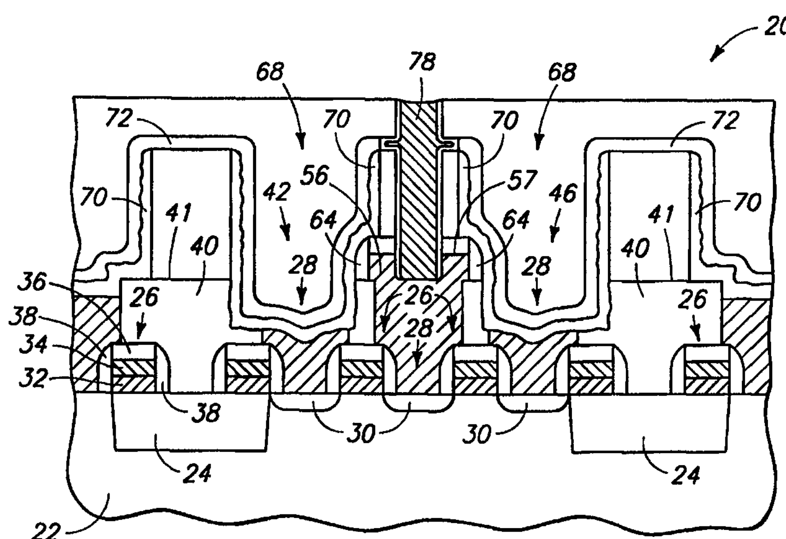
(54) Title: METHODS OF ELECTRICALLY CONTACTING TO CONDUCTIVE PLUGS, METHODS OF FORMING CONTACT OPENINGS, AND METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY CIRCUITRY

(57) Abstract



Methods of electrically contacting to conductive plugs, methods of forming contact openings, and methods of forming dynamic random access memory circuitry are described. In one embodiment, a pair of conductive contact plugs (54, 56; 56, 58) are formed to project outwardly relative to a semiconductor wafer. The plugs have respective tops, each of which being covered with different first and second (66) insulating materials. An opening (68) is etched through one of the first and second (54, 56; 56, 58) insulating materials to expose only one of the tops of the pair of plugs. Electrically conductive material (70) is formed within the opening (68) and in electrical connection with the one plug (54, 58). In a preferred embodiment, two-spaced apart conductive lines (26) are formed over a substrate and conductive plugs (54, 56, 58) are formed between, and on each side of the conductive lines (26). The conductive plug formed between the conductive lines provides a bit line contact plug (56) having an at least partially exposed top portion (60). The exposed top portion is encapsulated with a first insulating material (50, 62). A layer of second different insulating material (66) is formed over the substrate. Portions of the second insulating material are removed selectively relative to the first insulating material over the conductive plugs (54, 58) on each side of the conductive lines to provide a pair of capacitor containers. Capacitors are subsequently formed in the containers.

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DESCRIPTION

METHODS OF ELECTRICALLY CONTACTING TO CONDUCTIVE PLUGS, METHODS OF FORMING CONTACT OPENINGS, AND METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY CIRCUITRY

5 **Technical Field**

This invention relates to methods of electrically contacting to conductive plugs, to methods of forming contact openings, and to methods of forming dynamic random access memory circuitry.

Background Art

10 As circuit densities increase in semiconductor devices, the probabilities of individual device components becoming grounded to other device components increases as well. In the context of memory circuitry, and in particular dynamic random access memory circuitry, a continuing emphasis is placed upon maximizing the number of memory cells which are formed over a wafer. Balanced against 15 the concerns for maximizing efficient use of wafer real estate, are concerns associated with providing storage capacitors with desirably high storage capabilities.

This invention arose out of concerns associated with improving the usage of wafer real estate during formation of integrated circuitry. In particular, this invention arose out of concerns associated with providing improved methods of 20 forming dynamic random access memory circuitry.

Brief Description of the Drawings

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer 25 fragment in process in accordance with one embodiment of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that which is shown in Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 2.

30 Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step which 35 is subsequent to that shown in Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 7.

5 Fig. 9 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 8.

Fig. 10 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 9.

Fig. 11 is a view of the Fig. 1 wafer fragment at a processing step which
10 is subsequent to that shown in Fig. 10.

Fig. 12 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that shown in Fig. 11.

Fig. 13 is a diagrammatic side sectional view of a semiconductor wafer fragment in process, in accordance with another embodiment of the invention.

15 Fig. 14 is a view of the Fig. 13 wafer fragment at a processing step which is subsequent to that shown in Fig. 13.

Fig. 15 is a view of the Fig. 13 wafer fragment at a processing step which is subsequent to that shown in Fig. 14.

Fig. 16 is a view of the Fig. 13 wafer fragment at a processing step
20 which is subsequent to that shown in Fig. 15.

Fig. 17 is a view of the Fig. 13 wafer fragment at a processing step which is subsequent to that shown in Fig. 16.

Best Modes for Carrying Out the Invention and Disclosure of Invention

Methods of electrically contacting to conductive plugs, methods of forming
25 contact openings, and methods of forming dynamic random access memory circuitry are described. In one embodiment, a pair of conductive contact plugs are formed to project outwardly relative to a semiconductor wafer. The plugs have respective tops, one of which is covered with different first and second insulating materials. An opening is etched through one of the first and second
30 insulating materials to expose only one of the tops of the pair of plugs. Electrically conductive material is formed within the opening and in electrical connection with the one plug. In a preferred embodiment, two-spaced apart conductive lines are formed over a substrate and conductive plugs are formed between, and on each side of the conductive lines. The conductive plug formed
35 between the conductive lines provides a bit line contact plug having an at least partially exposed top portion. The exposed top portion is encapsulated with a

first insulating material. A layer of second different insulating material is formed over the substrate. Portions of the second insulating material are removed selectively relative to the first insulating material over the conductive plugs on each side of the conductive lines to provide a pair of capacitor containers. Capacitors are subsequently formed in the containers.

Referring to Fig. 1, a semiconductor wafer fragment 20 in process comprises a semiconductive substrate 22. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. A pair of isolation oxide regions 24 are provided and can be formed through conventional techniques such as shallow trench isolation techniques. A plurality of spaced-apart conductive lines 26 are formed over substrate 22. Between the conductive lines, three substrate node locations 28 are defined with which electrical communication is desired and preferably comprise diffusion regions 30. Individual conductive lines include a polysilicon layer 32, an overlying silicide layer 34, and an insulative cap 36. Sidewall spacers 38 are provided over the sidewalls of lines 26.

Referring to Fig. 2, an insulative material layer 40 is formed over substrate 22, and is subsequently patterned and etched to form openings 42, 44, and 46 over node locations 28. The insulative layer has an uppermost surface 41. An exemplary material for layer 40 is borophosphosilicate glass (BPSG).

Referring to Fig. 3, an electrically conductive material layer 48 is formed over substrate 22 and individual node locations 28. An exemplary material is polysilicon.

Referring to Fig. 4, a first deposition step deposits a first insulating material layer 50 over substrate 22 and conductive material 48. For purposes of the ongoing discussion, layer 50 comprises a first encapsulating material. An exemplary material is silicon nitride (Si_3N_4).

Referring to Fig. 5, a patterned plug masking layer 52 is formed over substrate 22 and node locations 28. Layer 52 masks over the centermost node location 28. An exemplary material is photoresist.

Referring to Fig. 6, material of first layer 50 and conductive material 48 is etched sufficiently to form electrically isolated conductive plugs 54, 56, and 58 within openings 42, 44, and 46 respectively. Plug 56 constitutes a furthermost projecting plug of the illustrated conductive plugs. Material of layer 50 is disposed only on the top of conductive plug 56. Plugs 54 and 58 are formed by etching material laterally adjacent furthestmost projecting plug 56. Such etching exposes a plug portion 60 of plug 56. Such etching can be conducted using at least two different etching chemistries to effect the etching. Where layer 40 comprises BPSG, layer 48 comprises polysilicon, and layer 50 comprises silicon nitride, suitable etch conditions are, for the nitride etch, CF_4, He, and CH_2F_2 at respective flow rates of 25 sccm, 150 sccm, and 30 sccm. For the polysilicon etch, Cl_2, CF_4 at respective flow rates of 75 sccm and 25 sccm. For a polysilicon overetch, Cl_2, HeO_2, and HBr at respective flow rates of 40 sccm, 8 sccm, and 160 sccm. In this example, conductive material within opening 44 is not etched, while some of the conductive material within openings 42, 46 is etched to recess it below uppermost surface 41 of insulative layer 40.

The conductive plugs project away or outwardly from substrate 22 and terminate proximate respective conductive plug tops 55, 57, and 59. Plugs 54 and 56 comprise a pair of first and second plugs which project away from a substrate different distances; and plugs 56, 58 comprise a different pair of first and second plugs which project away from the substrate different distances. Accordingly, plug tops 55, 57 and plug tops 57, 59 are formed at different elevations. Accordingly, some of the conductive plugs are formed elevationally below other conductive plugs.

In a preferred embodiment, and in the context of dynamic random access memory, the above-described plug formation constitutes forming conductive plugs between, and on each side of the conductive lines away from the conductive plug formed between the conductive lines. Conductive plug 56 provides a bit line contact plug having an at least partially exposed top portion 60. Top portion 60 is defined at least in part by sidewalls 61. Exposed top portion 60 joins with top 57 which defines a plug terminus.

Referring to Fig. 7, a first insulating material layer 62 is formed over the substrate and entirely covers or encapsulates exposed plug portion 60. Layer 62 constitutes a second layer of the first encapsulating material which is formed over plug portion 60. The forming of layer 62 constitutes a second first material

deposition step. Layer 62 is formed over previously-formed first insulating material 50.

Referring to Fig. 8, layer 62 is anisotropically etched to form sidewall spacers 64 over sidewalls 61. Accordingly, one of the conductive plugs is electrically insulated or encapsulated, while at least portions of the tops of the other conductive plugs are left outwardly exposed.

Referring to Fig. 9, a second insulating material layer 66 is formed over substrate 22 and is preferably different from the first insulating material. An exemplary material for layer 66 is an oxide material such as borophosphosilicate glass (BPSG). Plug top 57 of conductive plug 56 is accordingly covered with different insulating materials, e.g. the first and the second insulating materials. Plugs 54, 58 do not have their respective tops covered with both first and second insulating material.

Referring to Fig. 10, openings 68 are etched through second insulating material 66 to expose the tops of plugs 54, 58. In the illustrated example, conductive material comprising plugs 54, 58 is also removed. The etching of openings 68 preferably does not etch any of the material comprising conductive plug 56 because layer 66 is selectively etched or removed relative to the first material comprising sidewall spacers 64 and insulating material 50. Accordingly, openings 68 are self-aligned relative to plug 56. Exemplary self-aligned contact processing is described in U.S. Patent Nos. 5,651,855, 5,670,404, 5,597,763, and 5,378,654, which are incorporated by reference.

The etching of layer 66 removes selected portions of the second insulating material and provides a pair of capacitor containers over the non-furthestmost projecting conductive plugs.

Referring to Fig. 11, electrically conductive material is formed within each of openings 68 and in electrical connection with plugs 54, 58 respectively. In the illustrated example, the conductive material includes a storage node layer 70 which can comprise roughened polysilicon such as hemispherical grain (HSG) polysilicon or cylindrical grain (CSG) polysilicon. A dielectric layer (not specifically designated) is formed over storage node layer 70, with a cell plate layer 72 being formed thereover to provide storage capacitors within capacitor containers 68. A patterned masking layer 74 is formed over substrate 22 and provides an opening 76 through which a bit line contact is to be formed.

Referring to Fig. 12, a self-aligned penetrating contact is formed into conductive plug 56 to provide a bit line contact 78. Exemplary processing

methods of forming bit line contact 78 are described in U.S. Patent Nos. 5,362,666, 5,498,562, 5,338,700, and 5,292,677, which are incorporated by reference.

Referring to Fig. 13, a semiconductor wafer fragment 20a in accordance with another embodiment of the present invention comprises a semiconductive
5 substrate 22. Like numerals from the above-described embodiment are utilized where appropriate, with differences being indicated by the suffix "a". Conductive plugs 54a, 56a, and 58a are provided over substrate 22 and include respective tops 55a, 57a, and 59a which are formed proximate a substantially common elevation.

10 Referring to Fig. 14, a first insulating material layer 50a is formed over substrate 22.

Referring to Fig. 15, layer 50a is patterned and etched over conductive plug 56a.

Referring to Fig. 16, a second insulating material layer 66a is formed over
15 the substrate.

Referring to Fig. 17, layer 66a is patterned and preferably selectively etched anisotropically relative to layer 50a to form openings 68a over conductive plugs 54a and 58a respectively. Further processing can now take place in accordance with the methods described above.

20 The inventive methods permit integrated circuitry to be formed having improved densities with less risk of undesirable device grounding/shorting. In the context of memory circuitry, the inventive methods permit reductions in container cell size by reducing, if not eliminating altogether, the chances of a capacitor shorting to a bit line contact plug. Other advantages of the present invention
25 will be apparent to the skilled artisan.

CLAIMS

1. A method of electrically contacting to one of a pair of adjacent conductive plugs separated by intervening insulative material, comprising:

forming a pair of conductive contact plugs projecting outwardly relative to a semiconductor wafer, the plugs having respective tops covered with different first and second insulating materials;

etching an opening through one of the first and second insulating materials to expose only one of the tops of the pair of plugs; and

forming an electrically conductive material within the opening in electrical connection with the one plug.

2. The method of claim 1, wherein the etching of the opening comprises selectively etching the one of the first and second insulating materials relative to the other of the first and second insulating materials.

3. The method of claim 1, wherein the other of the plugs has its top covered with both the first and the second insulating materials.

4. The method of claim 1, wherein the one of the first and second insulating materials comprises an oxide material, and the other of the first and second insulating materials comprises a nitride material.

5. The method of claim 1, wherein the forming of the conductive contact plugs comprises forming the respective tops of the plugs proximate a common elevation.

6. The method of claim 1, wherein the forming of the conductive contact plugs comprises forming the respective tops of the plugs at different elevations.

7. The method of claim 6, wherein the forming of the conductive contact plugs comprises forming the one plug elevationally below the other plug.

8. A method of forming a contact opening comprising:

forming first and second conductive plugs over a substrate, the plugs projecting away from the substrate and toward respective plug tops;

electrically insulating one of the plugs with material comprising a first material, while leaving at least a portion of the top of the other of the plugs outwardly exposed;

forming a second material over both of the plug tops, the second material being different from the first material; and

selectively removing second material over the other of the plugs relative to the first material sufficiently to form a contact opening thereover.

9. The method of claim 8, wherein the forming of the first and second conductive plugs comprise forming the plug tops at different elevations.

10. The method of claim 8, wherein the forming of the first and second conductive plugs comprise forming the plug tops proximate common elevations.

11. The method of claim 8, wherein the one plug has sidewalls joined with its top, and the electrically insulating the one plug comprises forming sidewall spacers over the sidewalls.

12. The method of claim 11, wherein the top of the one plug is disposed elevationally higher than the top of the other plug.

13. The method of claim 8, wherein the electrically insulating the one plug comprises conducting two separate first material deposition steps.

14. The method of claim 13, wherein a first of the two steps comprises depositing first material only on the top of the one plug.

15. A method of forming a contact opening comprising:

providing a substrate having a pair of node locations with which electrical communication is desired;

forming a conductive plug over each node location, the conductive plugs projecting away from the substrate different distances and terminating proximate respective conductive plug tops;

encapsulating a furthestmost projecting of the two conductive plugs with a first encapsulating material, the encapsulating covering the furthermost

projecting conductive plug top and a plug portion proximate the top with first encapsulating material;

forming a second material which is different from the first material over the substrate including the two projecting plugs; and

5 selectively etching the second material relative to the first material sufficiently to form a contact opening over and expose the non-furthermost projecting of the two conductive plugs.

16. The method of claim 15, wherein the node locations comprise 10 diffusion regions.

17. The method of claim 15, wherein the encapsulating comprises forming the first encapsulating material over the furthermost projecting conductive plug in two separate steps.

15

18. The method of claim 15, wherein the encapsulating comprises:

forming a first layer of the first encapsulating material over the substrate and node locations;

etching the first layer and material laterally adjacent the furthestmost 20 projecting plug sufficiently to expose said plug portion; and

forming a second layer of the first encapsulating material over the plug portion

19. The method of claim 18, wherein the etching of the first layer and 25 material comprises using at least two different etching chemistries to effect the etching.

20. The method of claim 19 further comprising prior to the etching of the first layer and material, forming a patterned plug masking layer over the first 30 layer.

21. The method of claim 18, further comprising anisotropically etching the second layer of the first encapsulating material to provide sidewall spacers over the plug portions.

35

22. A method of forming dynamic random access memory circuitry comprising:

forming two spaced-apart conductive lines over a substrate;

forming conductive plugs between, and on each side of the conductive lines away from the conductive plug formed between the lines, the conductive plug formed between the conductive lines providing a bit line contact plug having an at least partially exposed top portion;

encapsulating the at least partially exposed top portion with a first insulating material;

forming a layer of second insulating material over the substrate, the second insulating material being different from the first insulating material; and

removing selected portions of the second insulating material selectively relative to the first insulating material over the conductive plugs on said each side of the conductive lines, the removing providing a pair of capacitor containers.

23. The method of claim 22, wherein the exposed top portion is defined at least in part by a sidewall, and the encapsulating comprises:

forming a layer of first insulating material over the substrate and sidewall; and

etching the layer sufficiently to form a sidewall spacer over the sidewall.

24. The method of claim 22, wherein the forming of the conductive plugs comprises forming said plugs to have respective tops which are disposed at a substantially common elevation.

25. The method of claim 22, wherein the exposed top portion joins with a top defining a plug terminus, and the forming of the conductive plugs on said each side of the conductive lines comprises forming said conductive plugs to be elevationally below the top.

26. The method of claim 22, wherein the encapsulating comprises forming said first insulative material over a previously-formed layer of first insulative material disposed over the top portion.

27. A method of forming dynamic random access memory circuitry comprising:

forming two spaced-apart conductive lines over a substrate, the lines defining three substrate node locations with which electrical communication is desired;

forming an insulative layer of material over the substrate:

forming openings through the insulative layer over the three substrate node locations;

forming electrically conductive material over the individual node locations and electrically isolated within the openings, the conductive material projecting away from the substrate, conductive material within one of the openings having a portion which is outwardly exposed;

forming a first insulating material over and entirely covering the conductive material outwardly exposed portion;

forming a second insulating material over the first insulating material which is different from the first material;

selectively etching the second insulating material relative to the first insulating material sufficiently to form capacitor containers over and to expose conductive material not within the one opening; and

forming capacitors received by the capacitor containers.

28. The method of claim 27, wherein the forming of the electrically conductive material comprises:

forming a patterned masking layer over the node locations;

etching the conductive material sufficiently to electrically isolate the conductive material within the openings.

29. The method of claim 28, wherein the etching of the conductive material comprises not etching conductive material within the one opening.

30. The method of claim 28, wherein the etching of the conductive material comprises recessing the conductive material to below an uppermost surface of the insulative layer within openings other than the one opening.

31. The method of claim 28, wherein the forming of the first insulating material and the covering of the conductive material exposed portion comprises

forming a first insulating material layer over the substrate and anisotropically etching the first insulating material layer.

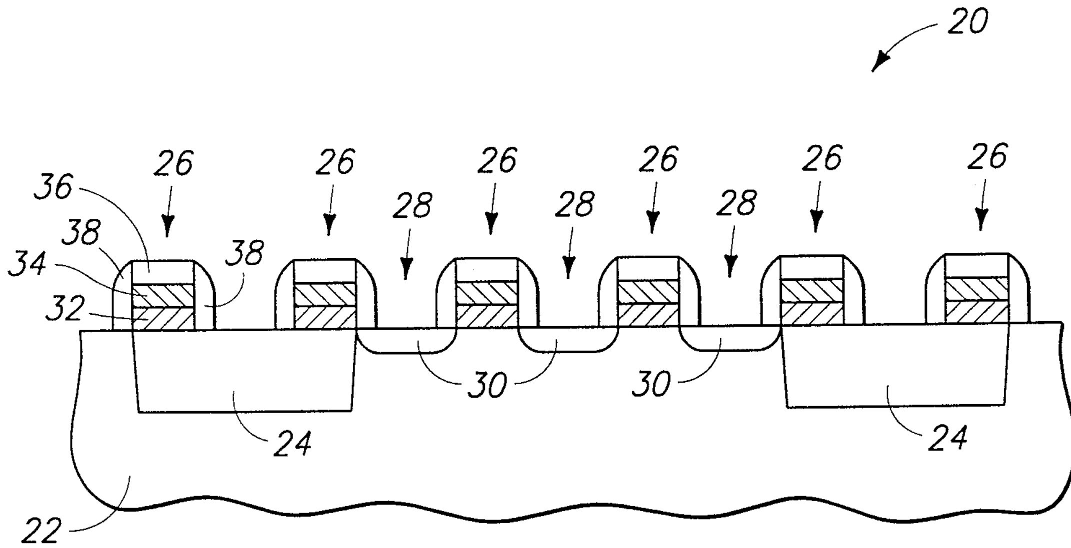

Fig 1

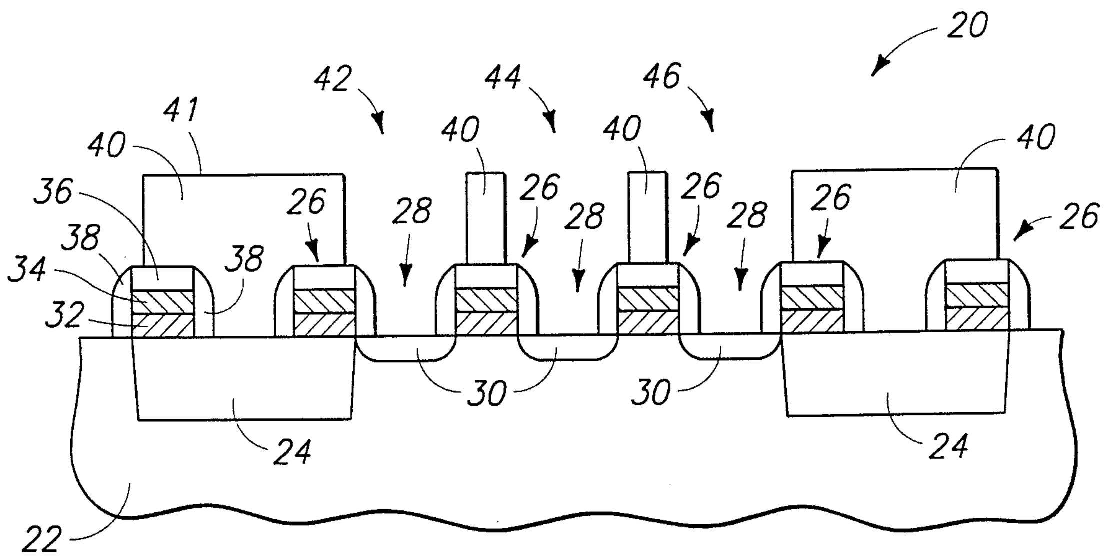

Fig 2

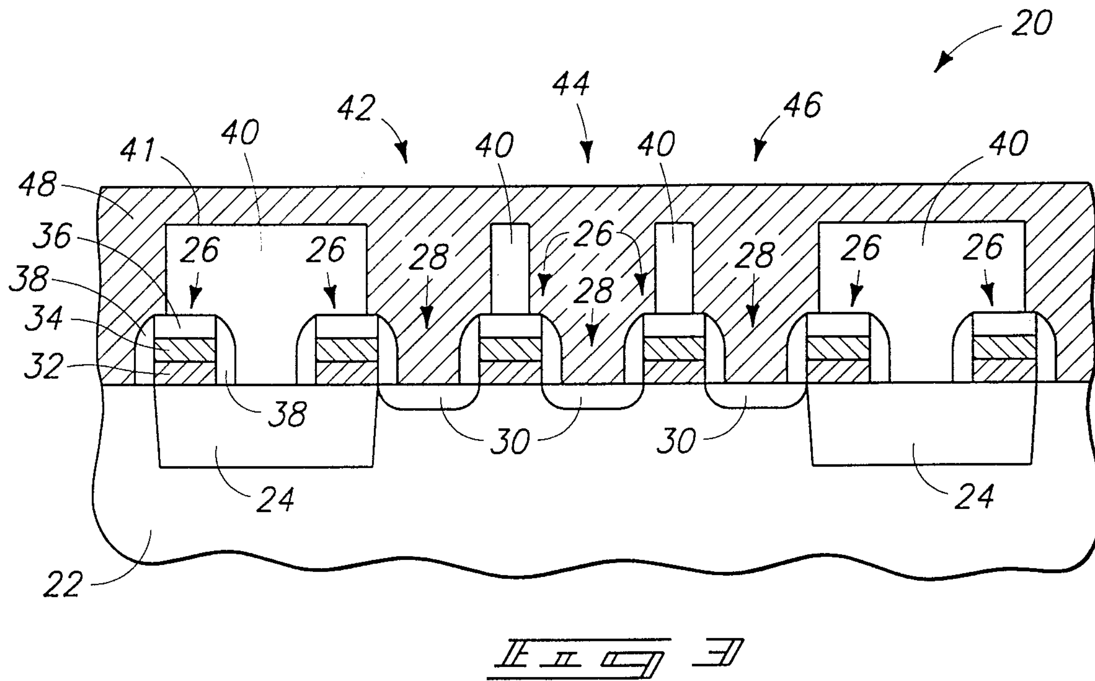

Fig 3

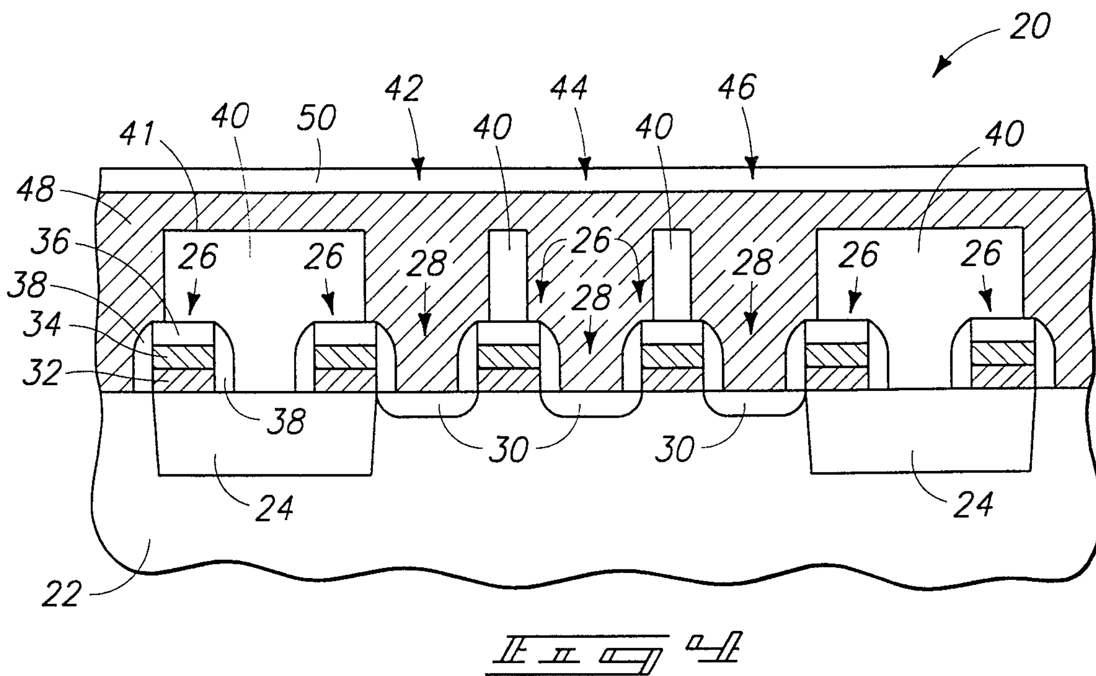

Fig 4

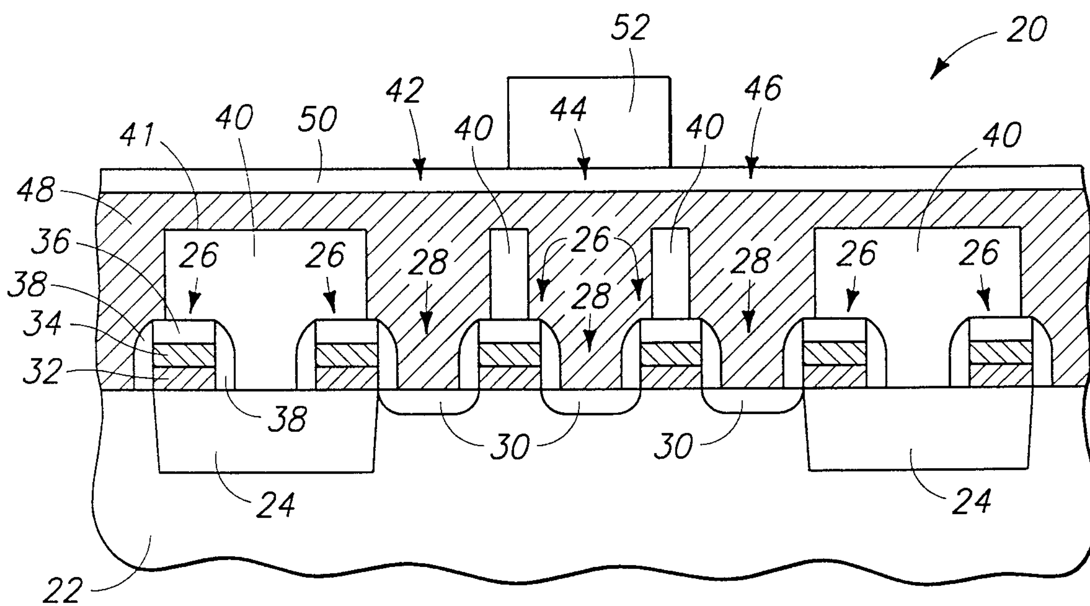

Fig 5

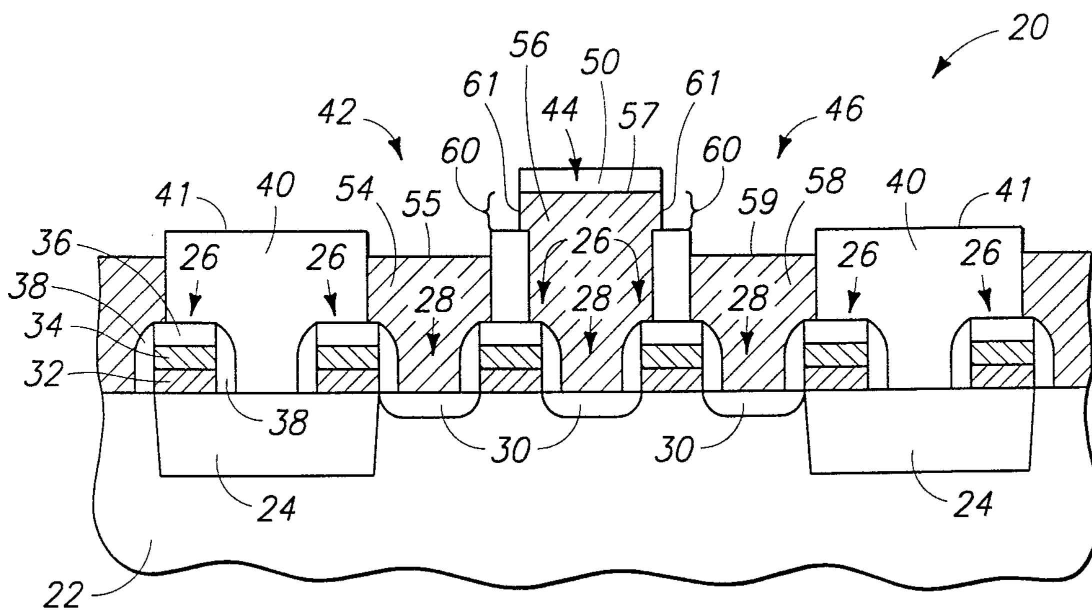

Fig 6

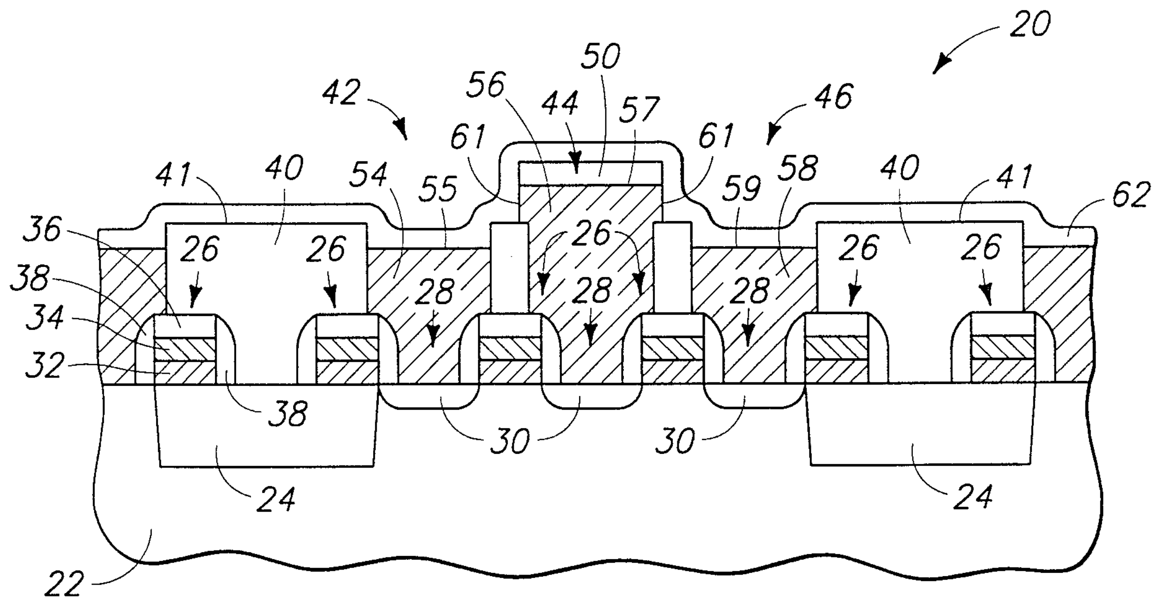

Fig 7

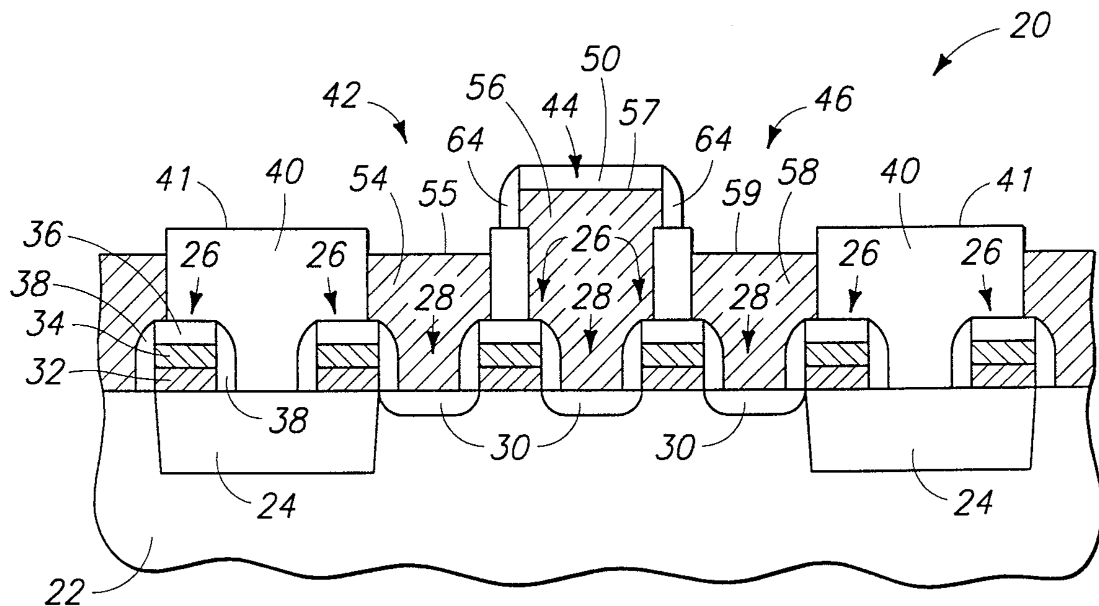

Fig 8

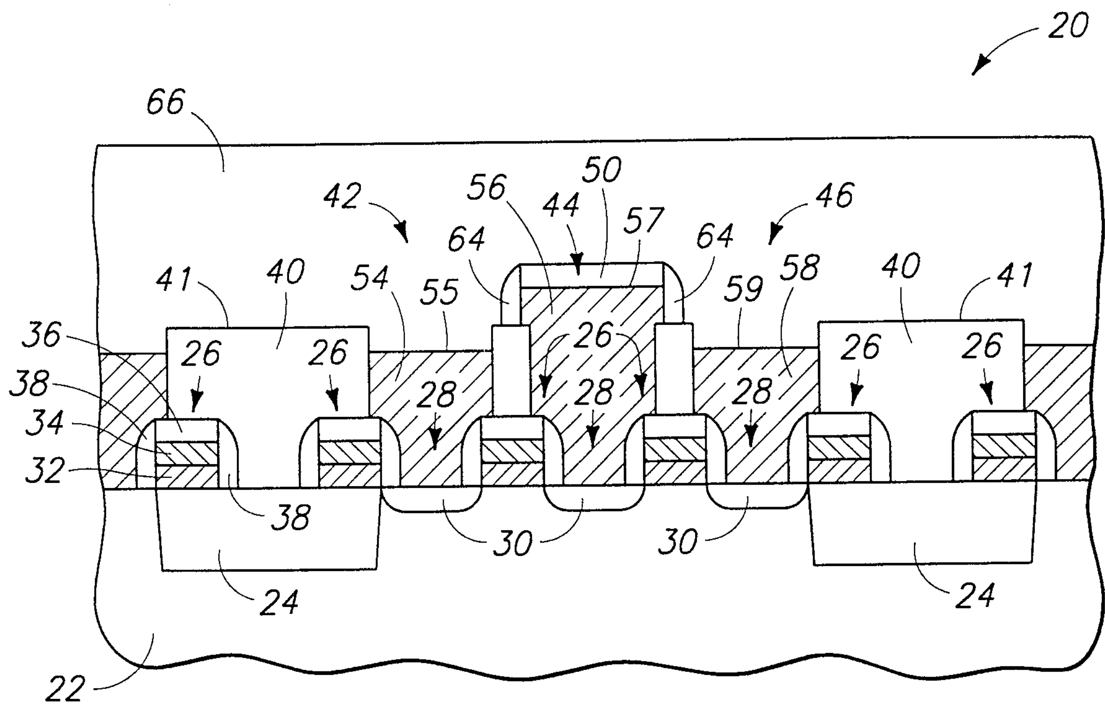

Fig 9

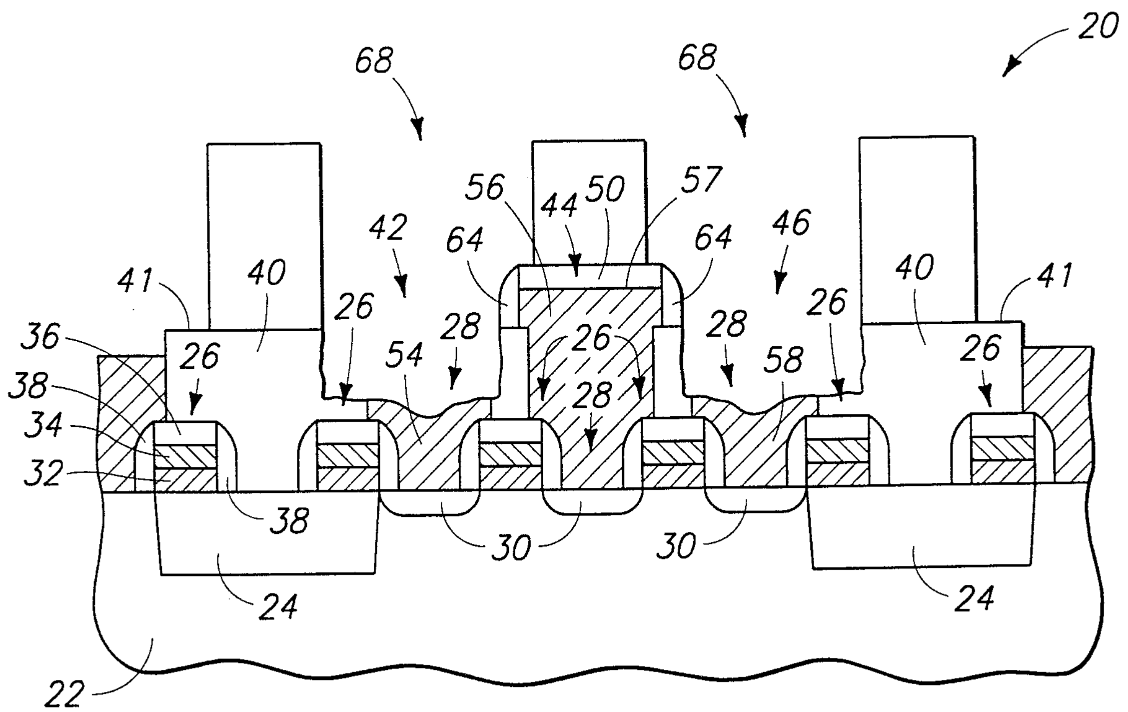

Fig 10

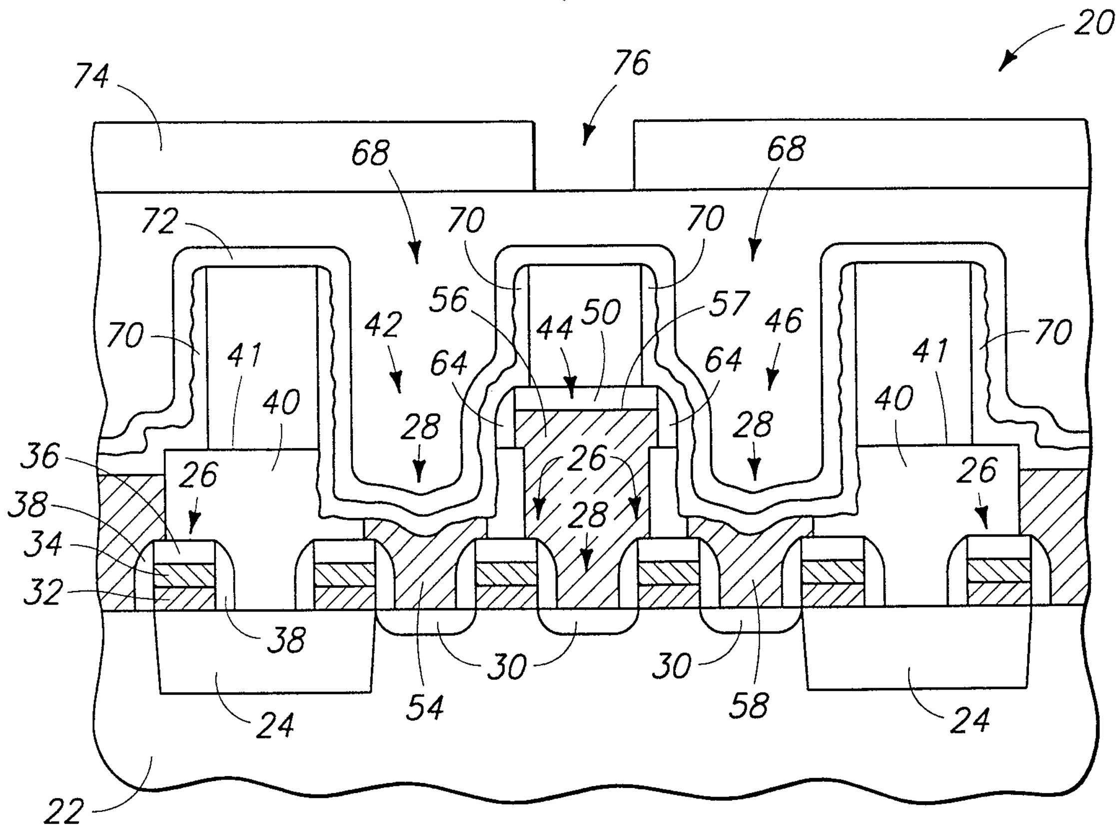

Fig 11

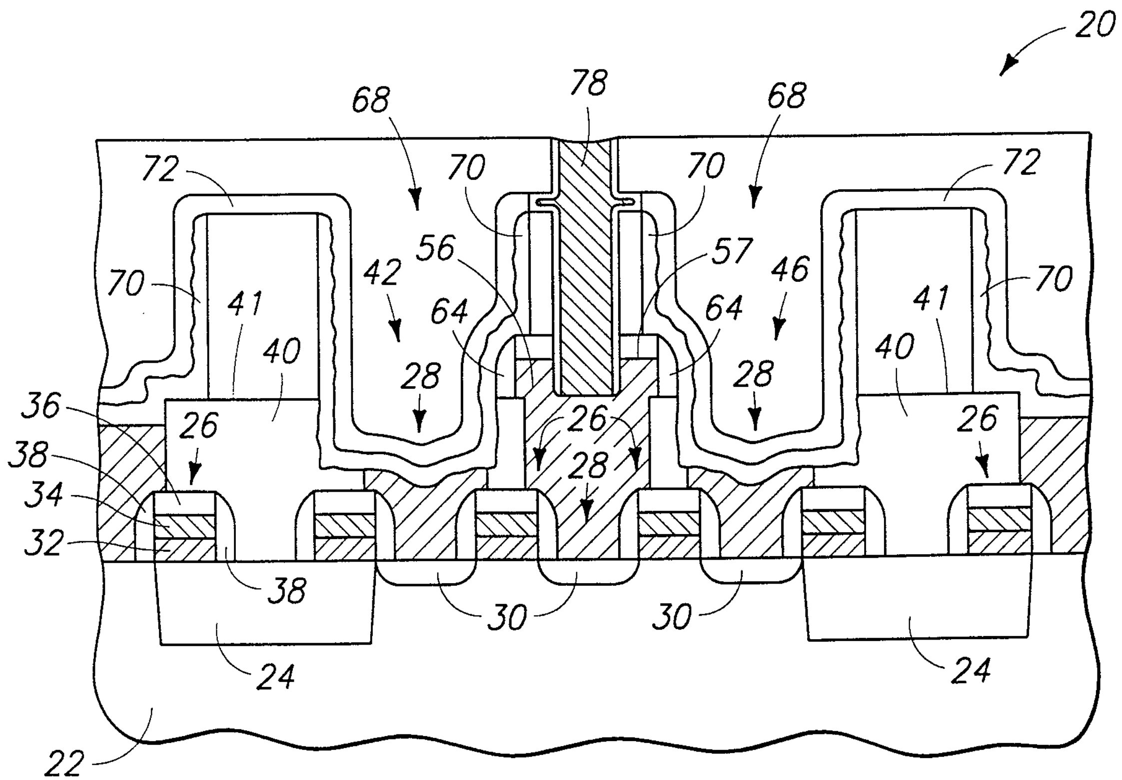

Fig 12

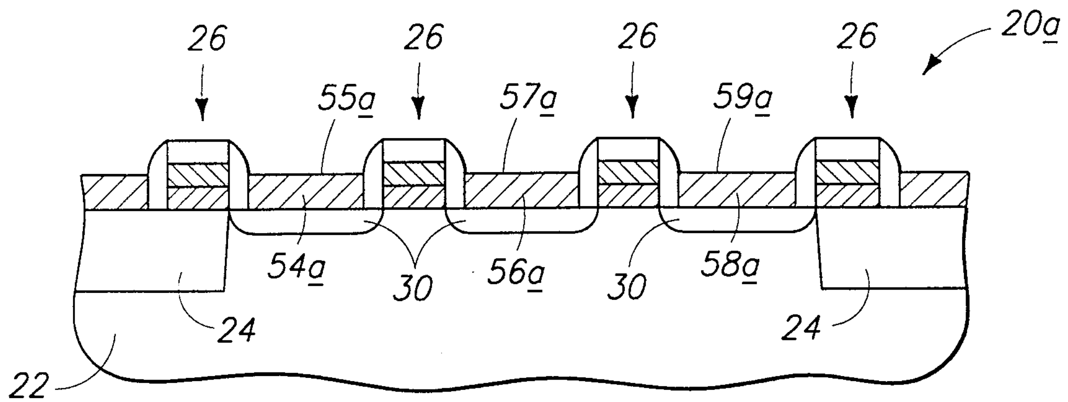

Fig 13

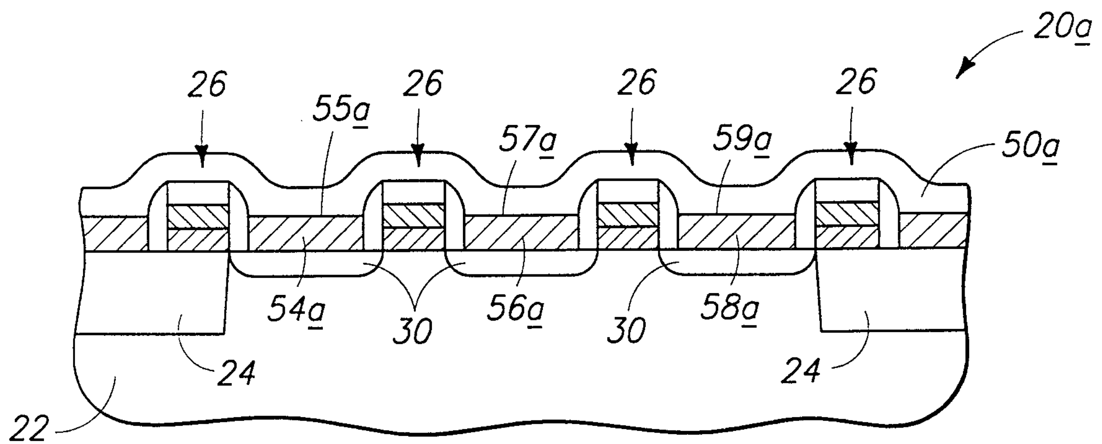

Fig 14

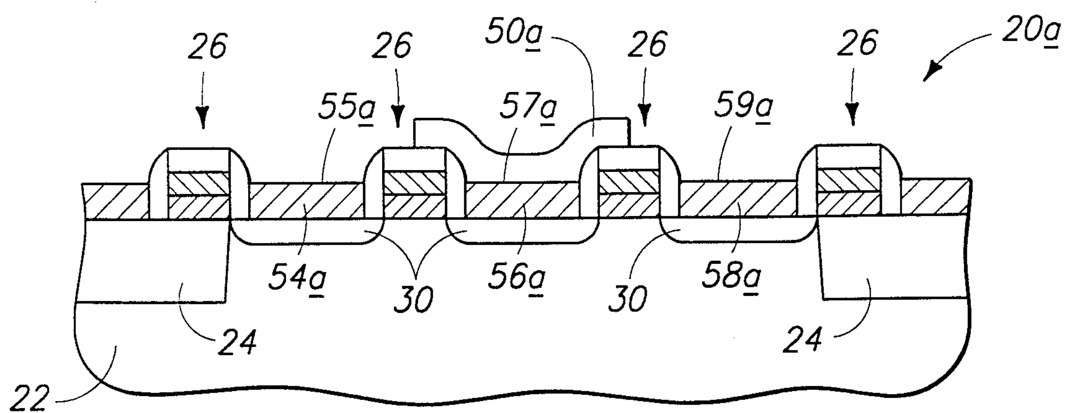

Fig 15

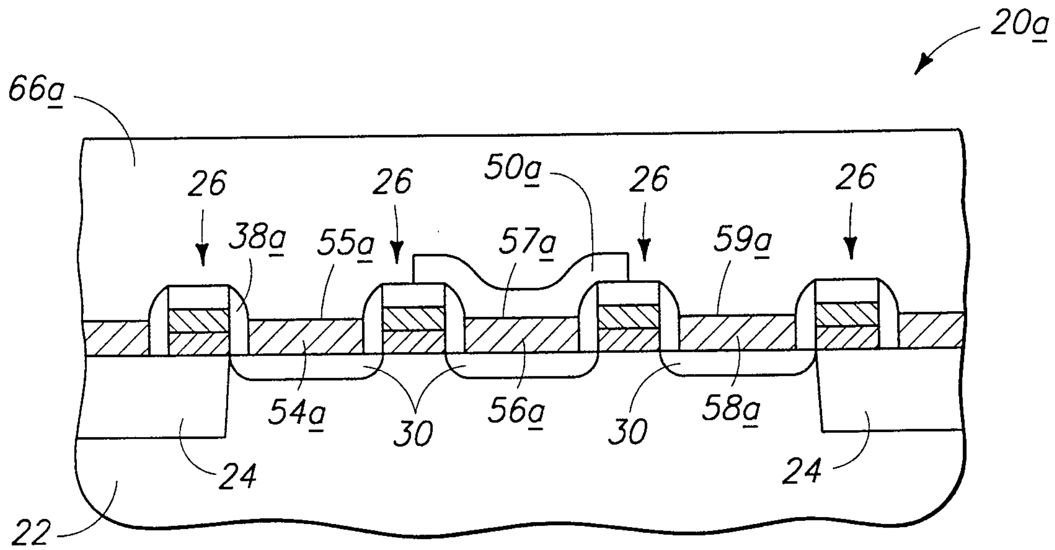

Fig 16

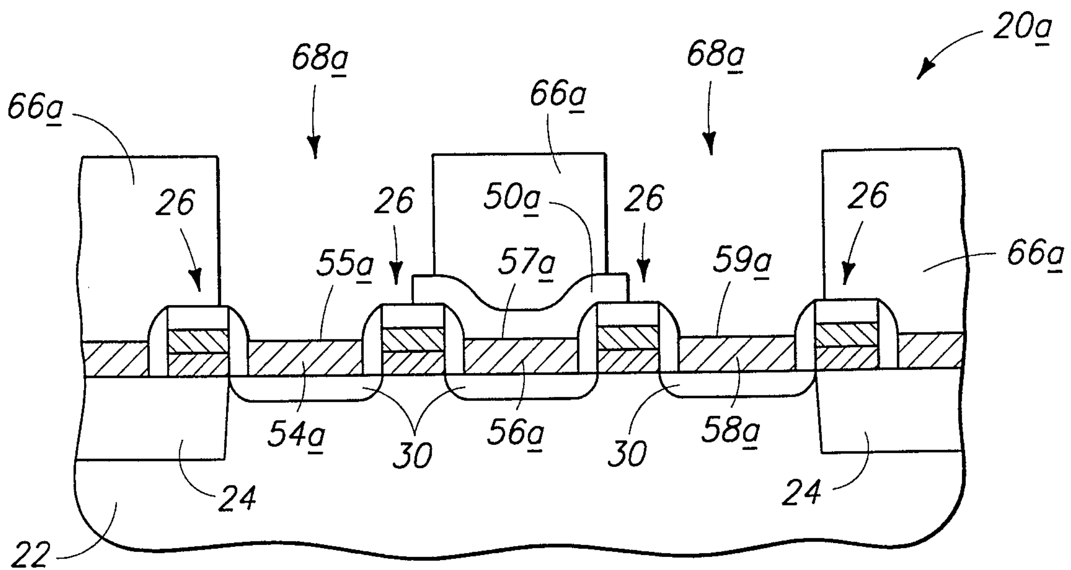

Fig 17

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 99/10369

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 569 948 A (KIM JAE K) 29 October 1996 (1996-10-29)	1,2,6,7, 15-18, 20-23, 25,26
A	column 5, line 60 - column 7, line 33; figures 6A-I	8-14
P,X	PATENT ABSTRACTS OF JAPAN vol. 099, no. 003, 31 March 1999 (1999-03-31) & JP 10 341005 A (SHIJIE XIANJIN JITI ELECTRIC CO LTD), 22 December 1998 (1998-12-22) abstract; figure	8,9, 11-18, 21,22

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 August 1999	09. 09. 1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Micke, K

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 99/10369

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 27-31
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 27-31

Claim 27, and therefore also claims 28-31 that depend on claim 27, are incomprehensible, even after consulting the drawings and the description.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte ional Application No
PCT/US 99/10369

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5569948 A	29-10-1996	KR 9707830 B	17-05-1997
		DE 4445796 A	22-06-1995
		JP 2575002 B	22-01-1997
		JP 7201999 A	04-08-1995
JP 10341005 A	22-12-1998	NONE	