BUILT OFF TESTING APPARATUS

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Appl. No.: 14/165,924

Filed: Jan. 28, 2014

Related U.S. Application Data

Division of application No. 12/730,314, filed on Mar. 24, 2010, now Pat. No. 8,674,718.

Foreign Application Priority Data

May 13, 2009 (KR) 10-2009-0041749

Publication Classification

Int. Cl. G01R 31/28 (2006.01)

U.S. Cl.

CPC G01R 31/2831 (2013.01)

USPC 324/762.05

ABSTRACT

A built off testing apparatus coupled between a semiconductor device and an external testing apparatus to test a semiconductor device. The built off testing apparatus can include a frequency multiplying unit to generate a test clock frequency by multiplying the frequency of a clock input by the external testing apparatus according to the operation speed of the semiconductor device, an instruction decoding unit to generate test information by decoding test signals input by the external testing apparatus according to the test clock frequency, and a test execution unit to test the semiconductor device according to the test information, and can determine whether the semiconductor device is failed or not based on test data output by the semiconductor device, and can transmit resulting data to the external testing apparatus.
FIG. 1 (RELATED ART)

WRITE

READ
FIG. 3
BUILT OFF TESTING APPARATUS

CROSS-REFERENCE TO RELATED APPLICATIONS


BACKGROUND

[0002] 1. Field of the Invention

[0003] The present general inventive concept relates to a built off testing apparatus, and more particularly, to a built off testing apparatus coupled between a semiconductor device and an external testing apparatus to test the semiconductor device.

[0004] 2. Description of the Related Art

[0005] Generally, after being fabricated, semiconductor devices are functionally tested to evaluate electrical characteristics of the semiconductor device. For example, dynamic random access memory (DRAM) undergoes tests to detect defects in internal memory cells or to evaluate DC characteristic of the DRAM.

[0006] FIG. 1 is a block diagram of a conventional external testing apparatus 10.

[0007] Referring to FIG. 1, the external testing apparatus 10 may be coupled to a device under test (DUT) 20 by contacting probes (not illustrated) electrically connected to the external testing apparatus 10 via connection cables, to the DUT 20. Then, the DUT 20 may be tested by a predetermined testing program stored in the external testing apparatus 10. For example, in cases where the DUT 20 is a DRAM, the external testing apparatus 10 transmits test information to emulate a writing operation synchronized with the operating frequency of the DRAM to the DRAM, and performs a reading operation to read out information stored in the DRAM in synchronization with the operating frequency of the DRAM. Next, the external testing apparatus 10 determines whether the DRAM is failed or not by comparing an expected value and information obtained from the reading operation.

[0008] However, in general, since precision of the waveform and speed of a test signal generated by the conventional external testing apparatus 10 are low relative to the operation frequency of the state of the art semiconductor devices operating at high speed and having high capacity, it is difficult to perform a reliable test with respect to the semiconductor devices. Due to recent increases in operation speed and capacities of these semiconductor devices, conventional external testing apparatuses are becoming outdated or unusable.

[0009] Since an external testing apparatus is a relatively expensive apparatus, it is economically beneficial to make use of an existing testing apparatus to test high performance semiconductor devices. As a technique to test high performance semiconductor devices by using a conventional external testing apparatus operating at a relative low speed, a technique to install a built in self test (BIST) circuit in semiconductor devices has been researched. However, the BIST circuit has a challenge to be applied to the semiconductor devices, since the BIST circuit increases the size of the semiconductor devices, and the additional process for fabricating the BIST circuit incurs increase in production costs of the semiconductor device.

SUMMARY

[0010] Exemplary embodiments of the present general inventive concept may be achieved by providing an economic and reliable testing apparatus to test semiconductor devices operating at a high speed by using a conventional external testing apparatus operating at a relative low speed.

[0011] Additional embodiments of the present general inventive concept will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the general inventive concept.

[0012] Example embodiments of the present general inventive concept may also be achieved by providing a built off testing apparatus coupled between a semiconductor device and an external testing apparatus to test the semiconductor device, the built off testing apparatus can include a frequency multiplying unit to generate a test clock frequency by multiplying the frequency of a clock input by the external testing apparatus according to the operation speed of the semiconductor device, an instruction decoding unit to generate test information by decoding test signals input by the external testing apparatus according to the test clock frequency, and a test execution unit to test the semiconductor device according to the test information, determines whether the semiconductor device is failed or not based on test data output by the semiconductor device, and transmits resulting data to the external testing apparatus.

[0013] The frequency multiplying unit may include a phase locked loop (PLL) frequency synthesis circuit. Furthermore, the test execution unit may include at least one finite state machine (FSM) that transmits test signals to the semiconductor device according to a stored testing program; and a comparing unit that generates the resulting data by comparing the test data and a stored expectation value.

[0014] The semiconductor device may be a wafer-level circuit, a chip-level circuit, or a package-level circuit. The semiconductor device may be a DDR memory device which may operate at high speed.

[0015] Example embodiments of the present general inventive concept may also be achieved by providing a built off testing apparatus coupled between a semiconductor device and an external testing apparatus to test the semiconductor device, the built off testing apparatus including a frequency multiplying unit to generate a test clock frequency by multiplying the frequency of a clock input by the external testing apparatus according to the operation speed of the semiconductor device, an instruction decoding unit to generate test information by decoding test signals input by the external testing apparatus according to the test clock frequency, at least one finite state machine (FSM) to transmit test signals to the semiconductor device according to a stored test program, and a comparing unit to determine whether the semiconductor device is failed based on test data output by the semiconductor device and transmits a resulting data to the external testing apparatus.

[0016] The built off testing apparatus may further include at least one of a connection terminal and a connection socket to connect the built off testing apparatus to the external testing apparatus and the semiconductor device.
Example embodiments of the present general inventive concept may also be achieved by providing a method of testing a semiconductor device, including generating a test signal frequency from a clock frequency of an external testing apparatus according to an operation speed of the semiconductor device, generating test information from a test signal of the external testing apparatus according to the test signal frequency, and inputting the test information to the semiconductor device according to the test signal frequency to determine whether the semiconductor device is failed.

The method may further include receiving result data from the semiconductor device based on the input test information, and transmitting the result data to the external testing apparatus according to the clock frequency of the external testing apparatus.

The method may further include comparing output values of the semiconductor device to expected output values according to the test signal frequency to determine whether the semiconductor device is failed.

The generating a test signal frequency may include multiplying the clock signal according to the operating speed of the semiconductor device.

The generating of test information may include decoding testing information of the external testing apparatus according to the test signal frequency.

Example embodiments of the present general inventive concept may also be achieved by providing a first unit to generate a first test signal frequency, and a second unit to generate a second test signal frequency from the first test frequency according to an operation speed of the semiconductor device, to transmit the second test signal frequency to the semiconductor device, and to receive a result signal from the semiconductor device based on the second test signal frequency to determine whether the semiconductor device is failed.

The second unit may also include a frequency multiplier to multiply the first test signal frequency according to the operating speed of the semiconductor device.

The second unit may also include a decoding unit to decode the first test signal frequency according to the second test signal frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the present general inventive concept will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram of a conventional external testing apparatus;

FIG. 2 is a block diagram of a built off testing apparatus according to an example embodiment of the present general inventive concept; and

FIG. 3 illustrates a state transition diagram of a FSM for a DRAM as the semiconductor device to be tested.
SDRAM)), the test signal output from the external testing apparatus 100 may include a clock CLK, an address ADDR, data DQs, and control signals /RAS, /CAS, and DQS. However, the test signals stated above are mere examples, and the test signal may simply include a test initiating signal to initiate a testing operation of the built off testing apparatus 300, as described below.

[0038] As illustrated in FIG. 2, a built off testing apparatus 300 according to an example embodiment of the present general inventive concept may be coupled between the external testing apparatus 100 and the semiconductor device 200. In the example embodiment of FIG. 2, the built off testing apparatus 300 may include input and output units I/Oa and I/Ob to respectively input and output signals between the external testing apparatus 100 and the semiconductor device 200. The input and output units I/Oa and I/Ob may include at least one connection terminal and at least one connection socket to be connected to the external testing apparatus 100 and the semiconductor device 200, respectively. For example, the input and output unit I/Ob may be connected to the semiconductor device 200 via pogo pins.

[0039] The exemplary built off testing apparatus 300 may include a frequency multiplying unit 310, an instruction decoding unit 320, and a test execution unit 330. The frequency multiplying unit 310 may generate a test clock frequency fb by multiplying a test clock frequency fa input by the external testing apparatus 100 according to the operation speed of the semiconductor device 200.

[0040] The frequency multiplying unit 310 may be implemented by a phase locked loop (PLL) frequency synthesis circuit, for example. The PLL frequency synthesis circuit may include a frequency divider to divide the test clock frequency fa input by the external testing apparatus 100 according to a predetermined division ratio, a frequency multiplier to multiply the frequency of the frequency-divided signal input by the frequency divider, and a voltage controlled oscillator to generate a test clock frequency fb in response to a signal input by the frequency multiplier. The semiconductor device 200 may be tested according to the test clock frequency fb generated by the frequency multiplying unit 310.

[0041] The instruction decoding unit 320 can generate second test information by decoding first test information input by the external testing apparatus 100 and can transmit the generated second test information to the test execution unit 330. The test execution unit 330 can test the semiconductor device 200 according to the second test information, can determine whether the semiconductor device 200 is failed based on test data output by the semiconductor device 200, and can transmit the resulting data of the test to the external testing apparatus 100 via the input and output unit I/Oa.

[0042] The test execution unit 330 may include a finite state machine (FSM) 340. For example, it is possible that the FSM 340 can include a circuit to generate an output value based on a current value of an input value and a previous value of the input value. The FSM 340 can be synchronized to the test clock frequency fb output by the frequency multiplying unit 310 and can make the state of the semiconductor device 200 change sequentially according to a predetermined testing mode. The exemplary FSM 340 of the present general inventive concept may have a plurality of states, for example, n states, and each state can be either maintained or shifted to a next state according to conditions (or control signals).

[0043] For example, each of the (n) states may be defined to correspond to each of predetermined operation modes of the semiconductor device 200 to be tested, wherein the operation modes may have a collective meaning determined by classifying various operations of the semiconductor device 200. FIG. 3 illustrates an exemplary state transition diagram of a FSM for a DRAM as the semiconductor device to be tested.

[0044] Referring to FIG. 3, no operation (NOP), activation (for example, activation of wordlines of a specific memory bank (ACTIVE)), memory read command (READ), memory write command (WRITE), and prechargeing of all banks (PRECHARGE) may be defined as respective operation modes of a DRAM. The basic operation modes of a DRAM listed above may be referred to in “Semiconductor Memories Technology, Testing and Reliability,” written by A. K. Sharma and published by IEEE press in 1996.

[0045] The arrows in FIG. 3 indicate state transitions according to fulfillment of respective conditions. For example, a basic reading operation of a memory cell of a DRAM may be performed in the sequence of ACTIVE, NOP, READ, NOP, and PRECHARGE. A basic writing operation of a memory cell of a DRAM may be performed in the sequence of ACTIVE, NOP, WRITE, NOP, and PRECHARGE. Furthermore, basic reading/writing operations of a memory cell may include an interleaving mode or a pipeline mode as known in the art. A MARCH test pattern or a REFRESH test pattern may be tested by using the FSM 340.

[0046] Although only one FSM 340 is illustrated in FIG. 3, the example embodiments of the present general inventive concept are not limited thereto, and it is possible that the test execution unit 330 may include two or more FSMs to perform two or more different sets of tests.

[0047] Moreover, in the example embodiments of the present general inventive concept, since the semiconductor device 200 can be tested by using the FSM 340, each state of testing the semiconductor device can be shifted to another state under state transition conditions, and thus comparative operations other than to test the state transition condition may not be required. Thus, the testing of the FSM 340 can be clearly defined, thereby improving stability of the built off testing apparatus and reliability of a test result. Furthermore, while a conventional built off testing apparatus which uses memory typically requires a significant amount of channel resource of the external testing apparatus 100, the FSM according to example embodiments of the present general inventive concept may use less resources of the external testing apparatus 100, making it possible to implement a parallel process by dividing channels of the external testing apparatus 100.

[0048] Referring again to FIG. 2, the test execution unit 330 may include a control unit 350 to control the FSM 340 and a stored expectation value 360. A comparing unit 370 can compare test data obtained from a result of testing the semiconductor device 200 using the FSM 340 and the stored expectation value 360 to determine whether the semiconductor device 200 is failed, and the resulting data can be output to the external testing apparatus 100. In this case, the resulting data may be transmitted to the external testing apparatus 100 at a reduced frequency equal to the operating frequency of the external testing apparatus 100.

[0049] It is possible that the built off testing apparatus 300 of the present general inventive concept may also be applied to a semiconductor device 200 provided with a conventional BIST circuit.
Although a few embodiments of the present general inventive concept have been illustrated and described, it will be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the general inventive concept, the scope of which is defined in the appended claims and their equivalents.

What is claimed is:

1. A method of testing a semiconductor device, comprising:
   - generating a test signal frequency from a clock frequency of an external testing apparatus according to an operation speed of the semiconductor device;
   - generating test information from a test signal of the external testing apparatus according to the test signal frequency; and
   - inputting the test information to the semiconductor device according to the test signal frequency to determine whether the semiconductor device is failed.

2. The method of claim 1, further comprising:
   - receiving result data from the semiconductor device based on the input test information; and
   - transmitting the result data to the external testing apparatus according to the clock frequency of the external testing apparatus.

3. The method of claim 1, further comprising:
   - comparing output values of the semiconductor device to expected output values according to the test signal frequency to determine whether the semiconductor device is failed.

4. The method of claim 1, wherein the generating a test signal frequency comprises multiplying the clock signal according to the operating speed of the semiconductor device.

5. The method of claim 1, wherein the generating test information comprises decoding test information of the external testing apparatus according to the test signal frequency.