(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 September 2010 (10.09.2010)

PCT

(10) International Publication Number
WO 2010/100391 A1

(51) International Patent Classification:
H02H 9/02 (2006.01)

(21) International Application Number:
PCT/GB2009/000619

(22) International Filing Date:
5 March 2009 (05.03.2009)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **SHORELINE PRODUCTS LIMITED** [GB/GB]; 49 Meadow Gate Avenue, Sheffield S20 2PG (GB).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **SHAW, Jonathan Robert** [GB/GB]; 65 Manor Park Road, Glossop, Derbyshire SK13 7SH (GB).

(74) Agent: **FRANKS & CO LIMITED**; 15 Jessops Riverside, Brightside Lane, Sheffield S9 2RX (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

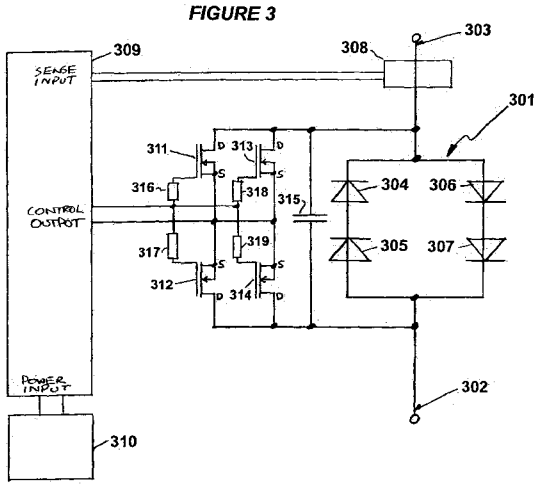
Published:

— *with international search report (Art. 21(3))*

WO 2010/100391 A1

(54) Title: IMPROVEMENTS IN GALVANIC ISOLATORS

FIGURE 3



(57) Abstract: A galvanic isolator is disclosed, which comprises a plurality of semiconducting elements, earth connecting means for connecting the plurality of semiconducting elements to at least two sources of electric potential having a current flow there between and control means adapted to switch the plurality of semiconducting elements into a low impedance state when a threshold voltage of the galvanic isolator is exceeded. The galvanic isolator further comprises an electronic bypass element adapted to bypass the plurality of semiconducting elements, and an electronic control circuit adapted to monitor the current flowing through the earth connecting means and to switch the electronic bypass element from a high resistance state suitable for a current flow below a first preset level, to a very low resistance state when the current flow increases above the first preset level. A method of reducing the power dissipation of a galvanic isolator is also disclosed.

Improvements in Galvanic Isolators

Field of the invention

The present invention relates to galvanic isolators and, more particularly, to a galvanic isolator having means for reducing its power dissipation. The present invention also relates to a method for reducing the power dissipation of a galvanic isolator.

Background to the Invention

Galvanic isolators are used to provide electrical safety earthing of exposed metallic parts associated with marine craft, pipelines, electrical supply distribution transformers and related equipment, or any other exposed metalwork or structure, which may pose a safety hazard to animals or humans under certain unusual conditions such as an electrical supply fault or lightning strike. A galvanic isolator may also be used to provide safety earthing of cathodic protected metallic structures, which are normally isolated from ground and have a small DC voltage deliberately applied thereto, in order to prevent electrochemical corrosion.

Galvanic isolators provide electrical isolation of exposed metalwork up to a certain voltage level of direct current (DC), the galvanic isolator threshold voltage, which is deemed sufficient to prevent the flow of electrochemically generated currents, or currents generated by nearby DC electrical installations, whilst providing a low impedance path to alternating or transient currents, such as mains electrical supply current or lightning. The electrical safety earth function is maintained, whilst allowing the exposed metalwork to be isolated from the ground up to a certain DC voltage level, which is sufficient to prevent electrochemical corrosion or other undesirable effects of DC, for instance power transformer core biasing.

Known galvanic isolators have used a parallel configuration of 2 or more electronic semiconductors such as silicon diodes silicon controlled rectifiers or transistors which are automatically switched into a low impedance when the galvanic isolator threshold voltage is exceeded and the safety earth function is required.

In the present disclosure, the specific field of application of a galvanic isolator using silicon diodes, and used with marine crafts, will be considered by way of example only, and it will be understood by persons skilled in the art that the principles explained herein are equally applicable to any other field of application for galvanic isolators.

For purposes of electrical safety in marine crafts, it is necessary to connect the exposed metalwork of a marine craft to the shore-based electrical safety earth, whereby in the event of a mains electrical fault on-board the craft, the potential difference between the craft and shore may be kept within safe limits, and overcurrent protective devices in the supply circuit may isolate the fault quickly and safely.

An undesirable result of this connection between the craft's metalwork and the shore safety earth is that low level direct current (DC) generated by electrochemical interaction between submerged dissimilar metals, such as the craft's propeller (possibly aluminium or bronze) and the mooring pier (typically steel), are allowed to flow through the safety earth connection. This results in undesirable electrolytic corrosion of submerged metalwork.

A galvanic isolator can be installed between the shore safety earth and the craft's safety earth to reduce this problem. The flow of low level DC is reduced to near zero, thereby reducing underwater electrolytic corrosion, whilst maintaining the electrical safety earth function.

With reference to Figure 1, an example of a prior art galvanic isolator 101 is shown, which comprises a plurality of semiconducting elements, in the example four diodes 104, 105, 106 and 107. The diodes are connected to at least two sources of electric potential having a current flow there between, in the example shore earth 102 and craft earth 103. With this configuration, there is substantially no current flow, unless the potential difference between shore earth 102 and craft earth 103 exceeds the combined threshold voltage of one pair of diodes or the other, hereafter referred to as the galvanic isolator threshold voltage. The galvanic isolator threshold voltage is typically in the range of 1 to 2 Volts. The potential difference generated by electrochemical interaction of submerged dissimilar metals in this situation is generally less than 1 Volt, whereby current flow and therefore electrochemical corrosion, amount to substantially zero.

In the event of a potential difference between shore earth 102 and craft earth 103 which exceeds the galvanic isolator threshold voltage, such as would occur in the event of a mains power fault, the diodes conduct and current flows. The galvanic isolator therefore maintains a safe potential difference in the range of 1 to 2 Volts between shore earth 102 and craft earth 103, whilst allowing fault current to flow.

Because of its safety function, it is necessary for the galvanic isolator to maintain electrical integrity with a high degree of reliability under the worst possible mains fault conditions (hereafter referred to as a worst-case fault). A worst-case fault comprises two distinct stages. The first stage is characterised by a partial insulation breakdown between live and earth, which is sufficient to pass a medium fault current of up to 150% of the nominal circuit current, but insufficient for triggering any overcurrent protection in the circuit.

The first stage of a typical worst-case fault, which may last several minutes or hours, may eventually be followed by a second stage characterised by a complete insulation breakdown (a short-circuit), which results in a very

high current surge, until such time as the overcurrent protection opens the circuit and isolates the fault, usually within a few milliseconds.

By way of reference, overcurrent protection in the circuit may comprise an overcurrent protective device such as an enclosed high breaking current (HBC) fuse or a miniature circuit breaker (MCB), which is connected to the AC mains electrical circuit and which is designed to limit the circuit current to safe levels, apt to prevent heating of the circuit conductors to a level at which insulation or connections would be damaged or compromised. A typical overcurrent protective device should pass the nominal circuit current indefinitely, allow an overcurrent of between 125% and 150% of the nominal circuit current to pass for a period of time up to 4 hours, allow an overcurrent of 500% or more of the nominal circuit current to pass for up to 5 seconds, and isolate a very high current surge of 100 times the nominal circuit current within approximately 10 milliseconds.

A worst-case fault, as described above may last for several minutes or hours, causing all parts of the circuit, including the galvanic isolator components, to heat up to the limits of maximum safe operating temperature for insulation, connections and reliability.

Under these fault conditions, heat is generated in the galvanic isolator within each diode 104, 105, 106 and 107, due to the voltage drop at the diode junction, in the range of 0.5 to 1 Watt per Amp per diode. The diode junctions and the surrounding material may therefore soon be operating at an elevated temperature, typically in the range of 120°C to 190°C. This long period of heating may at some point in time be followed by a complete insulation breakdown (a short-circuit), which results in a very high current surge, until such time as the overcurrent protection opens the circuit and isolates the fault, if overcurrent protection is present at all. In this latter context, some authorities advocate that galvanic isolators should be able to withstand mains surges as if overcurrent protection where entirely absent or inoperable and, in such cases,

the galvanic isolator must be able to handle a fault current surge equivalent to that required to melt the safety earth conductor itself.

The current surge may be close to the maximum prospective current available in the circuit. In a marine craft-shore environment, 5000 Amps RMS for a few tens of milliseconds can be expected in a 16 Amp or 32 Amp shore power circuit. This surge occurs at a time when the galvanic isolator diodes 104, 105, 106 and 107 are least able to withstand high current surges, due to their elevated junction temperature.

It is therefore desirable to improve the reliability and fault tolerance of a galvanic isolator under adverse operating conditions, particularly worst-case fault conditions.

Summary of the Invention

The invention relates to improvements in the reliability and fault tolerance capacity of a galvanic isolator, under the worst foreseeable operating conditions. Such improvements are achieved through a significant reduction in overall power dissipation, such as by a factor of ten or more, relative to the power dissipation characteristics of prior art designs.

According to a first aspect, there is provided a galvanic isolator, which comprises a plurality of semiconducting elements, earth connecting means for connecting the plurality of semiconducting elements to at least two sources of electric potential having a current flow there between and control means adapted to switch the plurality of semiconducting elements into a low impedance state when a threshold voltage of the galvanic isolator is exceeded. The galvanic isolator is characterised by further comprising an electronic bypass element adapted to bypass the plurality of semiconducting elements, and an electronic control circuit adapted to monitor the current flowing through the earth connecting means and to switch the electronic bypass element from a high resistance state suitable for a current flow below a first preset level, to a

very low resistance state when the current flow increases above the first preset level.

The electronic control circuit is preferably further configured to switch the electronic bypass element from the very low resistance state suitable for a current flow above the first preset level, to the high resistance state when the current flow increases above a second preset level higher than the first preset level.

The first preset level may be comprised in the range of 20 Amps to 30 Amps, and the second preset level may be comprised in the range of 100 Amps to 140 Amps.

The semiconducting elements are preferably selected from the group comprising diodes, silicon controlled rectifiers and transistors.

Preferably, the electronic bypass element comprises metal oxide semiconductor field effect transistors (MOSFETs).

Preferably, the electronic bypass element comprises a pair, or parallel connected pairs, of MOSFETs having body diodes, the body diodes being connected in opposition to prevent current flow when the MOSFETs are switched into a high impedance state. Alternatively, the electronic bypass element comprises two pairs, or parallel connected pairs, of MOSFETs having body diodes, the body diodes being connected to conduct and allow current flow. In this case the body diodes themselves form the plurality of diodes of the galvanic isolator.

The galvanic isolator may advantageously further comprise status indicating means adapted to indicate AC fault current flowing or direct current flowing to a user. The status indicating means may for instance be light emitting diodes (LEDs).

The galvanic isolator may comprise a current transformer means adapted to power the electronic control circuit. Alternatively, the galvanic isolator may further comprise mains supply connection means adapted to power the electronic control circuit.

The galvanic isolator may further comprise an enclosure for housing the galvanic isolator, the enclosure also having an overcurrent device or a residual current device or both an overcurrent device and a residual current device for limiting the prospective fault current available from a mains power supply, thereby limiting the maximum fault current flowing through the galvanic isolator.

The galvanic isolator may advantageously further comprise a monitoring element adapted to record events of significant amplitude, such as current surges and lightning strikes.

The galvanic isolator may advantageously further comprise surge protection means, the surge protection means comprising a transient voltage suppressor connected in parallel with the galvanic isolator or a series connected inductor, or both a transient voltage suppressor connected in parallel with the galvanic isolator and a series connected inductor.

Preferably, a current transducer of the electronic control circuit is a current transformer. Alternatively, the current transducer is a magnetic field detection device such as a hall-effect device adapted to detect the magnetic field generated by the fault current. Alternatively, the current transducer may be a low value series resistor with a voltage measuring circuit.

According to a second aspect, there is provided a galvanic isolator comprising an electronic bypass element comprising an array of metal oxide semiconductor field effect transistors (MOSFETs) having intrinsic body diodes, earth connecting means for connecting the plurality of intrinsic body diodes to

at least two sources of electric potential having a current flow there between, and an electronic control circuit adapted to monitor the current flowing through the earth connecting means, and to switch the electronic bypass element from a high resistance state suitable for a current flow below a first preset level, to a very low resistance state when the current flow increases above the first preset level.

The electronic control circuit is preferably further adapted to switch the electronic bypass element from the very low resistance state suitable for a current flow above the first preset level, to the high resistance state when the current flow increases above a second preset level higher than the first preset level.

The first preset level may be comprised in the range of 20 Amps to 30 Amps, and the second preset level may be comprised in the range of 100 Amps to 140 Amps.

The array is preferably a parallel connected MOSFET array comprising N channel enhancement mode MOSFETs.

According to a third aspect, there is provided a method of reducing the power dissipation of a galvanic isolator substantially as recited above, the method comprising the steps of monitoring current flowing through the earth connecting means, and switching the electronic bypass element in dependence on the monitoring, between a high resistance state when the current flows below a first preset level, and a very low resistance state when the current flow increases above the first preset level.

The method preferably comprises the further step of switching the electronic bypass element from the very low resistance state to the high resistance state when the current flow increases above a second preset level which is higher than the first preset level.

The first preset level may be comprised in the range of 20 Amps to 30 Amps, and the second preset level may be comprised in the range of 100 Amps to 140 Amps.

According to a fourth aspect, there is provided a craft equipped with a galvanic isolator substantially as recited above, wherein the at least two sources of electric potential respectively comprise a shore source and a craft source.

Brief Description of the Drawings

For a better understanding of the invention and to show how the same may be carried into effect, there will now be described by way of example only, specific embodiments, methods and processes according to the present invention with reference to the accompanying drawings in which:

Figure 1 shows a circuit diagram of a prior art galvanic isolator.

Figure 2 shows a graph of surge current rating of a diode.

Figure 3 shows a circuit diagram of a first embodiment of a galvanic isolator according to the invention.

Figure 4 shows a circuit diagram of a second embodiment of a galvanic isolator according to the invention.

Figure 5 shows a circuit diagram of a third embodiment of a galvanic isolator according to the invention, having overcurrent protection features.

Figure 6 shows a circuit diagram of a fourth embodiment of a galvanic isolator according to the invention, having very high power MOSFETs.

Figure 6 shows an oscillograph of the AC voltage drop of a prior art galvanic isolator.

Figure 7 shows an oscillograph of the AC voltage drop of a galvanic isolator according to the invention.

Detailed Description

There will now be described by way of example a specific mode contemplated by the inventors. In the following description numerous specific details are set forth in order to provide a thorough understanding. It will be apparent however, to one skilled in the art, that the present invention may be practiced without limitation to these specific details. In other instances, well known methods and structures have not been described in detail so as not to unnecessarily obscure the description.

Figure 2 is a graph of surge overload current for a typical silicon rectifier diode, which illustrates the improvement in surge current handling that may be expected when the starting junction temperature is reduced from 140°C to 45°C. If the temperature is reduced from 140°C to 45°C, under a fault current of 6000 Amps peak for example, the duration of surge which can be handled increases from 30 milliseconds to 110 milliseconds.

A first embodiment of the invention relates to a galvanic isolator for preventing corrosion of submerged metallic parts of a marine craft, while moored and connected to a land-based source of alternating current (AC) mains electrical power, by reducing the flow of electrochemically generated current.

This particular example of the invention is described here for purposes of demonstrating and understanding the principles of the invention and to provide an example of a practical use thereof, however without restricting the invention to this particular example.

A block diagram showing the component parts of the galvanic isolator is shown in Figure 3 and comprises a galvanic isolator substantially as illustrated in, and detailed with reference to, Figure 1, with the addition of an electronic bypass element, which can be automatically switched between a high resistance state and a very low resistance state by an electronic control circuit, which responds to changes in current flowing through the galvanic isolator.

The galvanic isolator 301 therefore comprises semiconducting elements, in the example diodes 304, 305, 306 and 307, and further comprises a parallel connected MOSFET array comprising N channel enhancement mode MOSFETs 311, 312, 313 and 314.

The MOSFET array is controlled by an electronic control circuit, which is powered by a power supply 310, and which responds to changes in alternating current flowing between craft earth 303 and shore earth 302. The MOSFET array is made up of one or more pairs of series connected MOSFETS connected source to source.

There is a diode junction, the intrinsic body diode, which is inherent in the manufacture of each MOSFET. The cathode of the body diode is the channel itself, while the anode is internally connected to the source terminal. The body diode therefore appears as if it were connected in parallel with the MOSFET from source to drain terminals, with the cathode connected to the drain terminal and the anode connected to the source terminal. It is therefore necessary to use series connected pairs in this way, to prevent current flowing through the body diode when the MOSFET is turned off and the source terminal is more positive than the drain terminal.

In the example, two series-connected pairs are used in parallel, in order to increase the overall current rating of the array and to reduce the power dissipation, by virtue of the overall lower resistance of the parallel connected

paths. Depending on the current handling requirements of the application, more parallel pairs of MOSFETs may be used in parallel in order to increase the current handling and/or reduce the power dissipation. The 'on' resistance of MOSFETs increases with rising temperature, whereby MOSFETS connected in parallel will tend to share current equally due to the thermal feedback effect.

Resistors 316, 317, 318 and 319 prevent ringing or oscillation phenomena, due to the parasitic inductance and capacitance around the MOSFETs.

The MOSFET array can be switched into a conducting state by applying a positive control voltage between 5 and 15 Volts with respect to the source terminals, to the gate terminals via the resistors 316, 317, 318 and 319. The resistance from source to drain when in the conducting state is less than 1 milliohm for each MOSFET used in this example. If the gate voltage is near zero with respect to the source, then the MOSFET is switched into a high impedance state. When the array is switched into the conducting mode, it appears as a near short-circuit across the galvanic isolator 301, amounting to approximately 1 milliohm in total in this example.

Under normal operating circumstances, the gate and source terminals of the MOSFETS are kept at the same potential, whereby the MOSFETS are in a high impedance state and this allows the galvanic isolator to function substantially as described above.

In the event of a mains fault above a certain preset magnitude as measured by the current transducer 308 and the control circuit 309, for example comprised between 20 and 30 Amps, for instance 28 Amps, the MOSFET array is automatically switched into the low-impedance state. As a consequence, the voltage drop across the galvanic isolator is considerably reduced, whereby the dissipated power and consequent heating of the galvanic isolator components are correspondingly reduced. Notably, the diodes 304,

305, 306 and 307 are now not conducting any current at all, because the applied voltage is below their threshold voltage for conduction. Their junction temperatures will therefore be close to ambient temperature.

The MOSFET array remains in the conducting state as long as the AC fault current flows. When the fault is isolated by the mains circuit overcurrent protection, the AC current drops to near zero, the MOSFET array is automatically switched into the high-impedance state and the galvanic isolator returns to normal operation.

Capacitor 315 is present in order to provide a low impedance path to low-level AC current, such as that from the AC line filters in connected equipment, and leakage current up to a few milliamps that may occur under normal non-fault circumstances.

The low impedance path provided by capacitor 315 prevents low-level AC currents from compromising the effectiveness of the corrosion inhibiting function of the galvanic isolator, by reducing the likelihood that the diodes 304, 305, 306 and 307 will become forward-biased or nearly forward-biased under normal operating conditions.

The power-supply 310 may be derived from an external source, or may be derived from the AC fault current via a current transformer.

The MOSFET array may not be able to handle the maximum expected fault current, in which case the control circuit may employ an overcurrent protection function which switches the MOSFET array into the high-impedance state when the current through the galvanic isolator exceeds a pre-set value, for example comprised between 100 Amps and 140 Amps, for instance 140 Amps peak.

The current transducer 308 may be a current transformer, a Hall-effect device, or a low value series resistor (approximately 0.5 milliohm) with a voltage measuring circuit.

Protection against lightning strikes can be added for increased reliability. This function can be implemented by using a series inductor which limits the peak current of high speed transients, and a transient voltage suppressor which dissipates the remaining lightning energy and limits the voltage applied to the galvanic isolator to a safe level.

The galvanic isolator can be built into an enclosure through which the AC mains power supply to the craft must pass, and which contains a residual current device (RCD) and a current limiting circuit breaker (MCB) for protecting the craft's electrical wiring from overcurrent and earth leakage faults. A more economical design can therefore be used for the galvanic isolator, because the expected fault currents are well defined.

Status indicators such as light emitting diodes (LEDs) can be fitted to advise of situations such as fault current flowing.

With reference to Figure 4, a second embodiment of a galvanic isolator is shown, wherein the galvanic isolator 401 again comprises four diodes 304, 305, 306 and 307, a MOSFET array 311, 312, 313 and 314 with gate resistors 316, 317, 318 and 319, and a capacitor 315, the apparatus operating substantially as explained with reference to Figure 3 above.

In this embodiment, the current transducer 308, the control circuit 309 and the power-supply 310 having respective functionalities substantially as explained with reference to Figure 3 above, are combined.

When an AC fault current flows between craft earth 303 and shore earth 302, the current transducer 308 applies a corresponding AC voltage at the input

terminals of a bridge-rectifier 420. The rectified DC output of the bridge rectifier 420 is smoothed into steady DC by reservoir capacitor 422. The smoothed DC voltage is applied to voltage regulator 421, which maintains the DC voltage on its output terminals at 12 Volts or less. Capacitors 423 and 424 provide decoupling and prevent self-oscillation of the voltage regulator 421.

The output voltage from the voltage regulator 421 is connected between gate and source connections of the MOSFET array, whereby the MOSFET array will be automatically switched into the conducting mode when the current flowing between craft earth 303 and shore earth 302 is such that the voltage regulator output exceeds approximately 5 Volts, therefore above the gate threshold voltage of the MOSFETs.

LED 425 and current limiting resistor 426 provide visual indication that the device is active, i.e. that fault current is flowing.

The MOSFET array will remain in the conducting state until the fault current between craft earth 303 and shore earth 302 reduces below a certain value which corresponds to the voltage on the output of the voltage regulator 421 falling below the gate threshold voltage of the MOSFETs.

Resistor 451 ensures that the gate-source voltage is close to zero when there is no AC fault current flowing, and ensures the MOSFETs remain in the high-impedance state unless a fault-current is detected.

With reference to Figure 5, a third embodiment of a galvanic isolator is shown, wherein the galvanic isolator is designed to withstand a long-term fault of 100 Amps RMS for 4 hours at an ambient temperature of 50°C, immediately followed by a surge of 5000 Amps RMS for half a second.

The diodes 304, 305, 306 and 307 are chosen with characteristics apt to withstand a surge of substantially 5000 Amps for approximately 0.5 seconds from a starting temperature of substantially 50°C.

The MOSFET array is designed to reduce power dissipation during the first part of the fault (100 Amps for 4 hours) by short-circuiting the diodes 304, 305, 306 and 307. The MOSFET array uses four pairs of MOSFETS in parallel, however only two pairs are shown in Figure 5 for not obscuring the Figure unnecessarily.

The resistance of the array when switched into the conducting state is 0.5 milliohms or less, whereby the array will dissipate only approximately 5 Watts.

Because the expected fault current is so high in this example, an overcurrent protection circuit is incorporated in the control circuit, whereby the MOSFET array will be automatically switched off in the event of a high current surge.

The overcurrent protection circuit is designed to operate in such a way as to ensure the MOSFET array is always operating within safe limits. The array can handle the continuous 100 Amps RMS. without any significant temperature rise, but cannot handle the 5000 Amps surge for more than 100 microseconds. The protection circuit is designed to turn the MOSFET array off in less than 5 microseconds if the current rises above 140 Amps peak, which keeps the MOSFETs operating within safe limits.

The overcurrent protection circuit uses a differential amplifier to measure the voltage drop across the MOSFET array, which is proportional to the current flowing.

The galvanic isolator 401 again comprises four diodes 304, 305, 306 and 307, a MOSFET array 311, 312, 313 and 314 with gate resistors 316, 317, 318

and 319, and a capacitor 315, the apparatus operating substantially as explained with reference to Figures 3 and 4 above.

Power for the control circuit is derived from the fault current via current transformer 530, which develops an alternating voltage which is rectified and smoothed by bridge rectifier 554 and reservoir capacitor 555, and regulated at 12 Volts by voltage regulator 556.

Varistor 552 and capacitor 553 provide transient voltage suppression along with the inductance and resistance inherent in the current transformer 530. Zener diode 564 is a high power transient suppressor, which protects the voltage regulator 556 from voltages greater than approximately 30 Volts. Capacitor 557 provides decoupling and prevents self-oscillation of the voltage regulator 556.

Voltage regulator 562 provides a regulated 5 Volt supply. Capacitor 563 provides decoupling and prevents self-oscillation of the voltage regulator 562. Switched capacitor inverter 570 generates minus 5 Volts for use by the overcurrent sense amplifier 533.

The control circuit is activated and the MOSFET array is automatically switched into the low resistance state when the SHUNT-ON signal is generated by zener diode 558, resistors 559, 560 and capacitor 561.

Zener diode 558 starts to conduct when the power supply reaches about 9 Volts, this causes the voltage on capacitor 561 to rise until after approximately a 2 seconds time delay, the SHUNT-ON signal will reach the logic 1 threshold voltage of AND gate 549. Resistors 559 and 560 and capacitor 561 are configured to provide a 2 second delay to avoid triggering the control circuit under transient conditions, for instance a lightning strike or a high current surge from short-circuit faults, wherein such transient conditions are not expected to last more than 1 second.

The overcurrent sense amplifier comprises an operational amplifier (op-amp) 533 and gain-setting resistors 529, 530, 531 and 532, which amplify the voltage between point A and point B on the diagram. The resistance between point A and point B is about 0.7 milliohm with the MOSFET array in the low-impedance state. Therefore, a current of plus or minus 140 Amps peak will generate an output from op-amp 533 of approximately plus or minus 1.5 Volts peak.

The output of the overcurrent sense amplifier 533 in response to an AC fault current flowing between craft earth 303 and shore earth 302 is a corresponding AC waveform with a magnitude proportional to the current and centred about 0 Volts. The output is AC coupled by capacitor 534, whereby any DC offset errors from the amplifier 533 are eliminated.

Op-amps 538 and 540, resistors 535, 536 and 537 and diode 539 are configured as an absolute value circuit, whereby both negative and positive current peaks can be detected by the overcurrent threshold circuit, which consists of a comparator 546 and associated components. The absolute value circuit operates as follows: for positive inputs, the diode 539 is reverse-biased and has no influence on the circuit, op-amp 538 and resistors 535, 536, 537 operate as a simple unity-gain voltage follower; when the input voltage to the absolute value circuit becomes negative, the diode 539 is forward-biased and the output of op-amp 540 holds the non-inverting input of op-amp 538 at 0 Volts, whereby op-amp 538 and resistors 536, 537 now form a simple unity-gain inverting amplifier.

For this circuit to operate properly from a single supply, as required in the example, and for reasons of response time, the common-mode input range of op-amp 540 must extend below the negative supply of 0 Volts in this case. Moreover, the inputs of op-amp 540 must remain at high- impedance within the entire operating range of the input to the absolute value circuit, down to

approximately – 2 Volts in this case. Also both op-amps 539, 540 must be capable of driving their outputs to the negative power supply rail (0 Volts).

The threshold detection circuit comprises comparator 546, resistors 542, 543 and capacitor 545.

Comparator 546 compares the output of the absolute value circuit with a preset threshold voltage derived from the + 5 Volt supply via the divider chain of resistors 542, 543, which is decoupled by capacitor 545.

If the maximum design current threshold of 140 Amps peak is exceeded, then this condition will be detected by comparator 546, the output of which will swing to ground if the output of the absolute value circuit exceeds the threshold voltage of 1.5 Volts applied to the non-inverting input of comparator 546.

Therefore, the output of AND gate 549 swings to ground and the MOSFET array is driven into the high impedance state by the MOSFET driver 550. In this case the fault current will now flow through the diodes 304, 305, 306 and 307 until the fault current drops below the overcurrent threshold.

The use of schmitt-trigger inputs and a high speed MOSFET driver i.c. 550 is intended to reduce the turn-on and turn-off time of the MOSFET array, to keep it operating within reliable limits of current and power dissipation.

Pull-down resistor 551 ensures that the gate-source voltage is close to zero when there is no AC fault current flowing and therefore no power supply voltage, and ensures the MOSFETs remain in the high-impedance state unless a fault-current is detected.

Capacitors 563, 564, 565, 566, 567, 568 and 569 are power supply decoupling capacitors.

With reference to Figure 6, a fourth embodiment of a galvanic isolator is shown, which uses MOSFETs apt to withstand the 5000 Amp surge for 0.5 seconds, and wherein the overcurrent protection circuit is not necessary, because the intrinsic body diodes are able to handle this high current surge and can be used in place of the discrete diodes 304, 305, 306 and 307 used in the previous embodiments.

The galvanic isolator 601 comprises four diodes 604, 605, 606 and 607 and a capacitor 315, operating as previously explained in relation to Figures 3, 4 and 5. The diodes 604, 605, 606 and 607 are the intrinsic body diodes of the four MOSFETs 684, 685, 686 and 687.

When an AC fault current flows between craft earth 303 and shore earth 302, current transformer 697 applies a corresponding AC voltage at the input terminals of the bridge-rectifier 1000.

The rectified DC output of the bridge rectifier 1000 is smoothed into steady DC by reservoir capacitor 1010. The smoothed DC voltage is applied to voltage regulator 1070, which maintains the DC voltage on its output terminal at 12 Volts or less. Capacitors 1020 and 1010 provide decoupling and prevent self-oscillation of the voltage regulator 1070.

The MOSFET array will remain in the conducting state until the fault current between craft earth 303 and shore earth 302 reduces below a value, which corresponds to the voltage on the output of the voltage regulator 621 falling below the gate threshold voltage of the MOSFETs.

Zener diode 1050 starts to conduct when the power supply reaches about 9 Volts, this causes the voltage on capacitor 1060 to rise until after approximately a 2 seconds time delay, it will reach the logic 1 threshold voltage of the MOSFET driver 696. Resistors 1030, 1040 and capacitor 1060 are configured to provide a 2 second delay to avoid triggering the control circuit

under transient conditions, such as a lightning strike or high current surges from short-circuit faults. Such transient conditions are expected not to exceed approximately 1 second.

The output voltage from the MOSFET driver i.c. 696 forward-biases the diodes 604, 605, 606 and 607, switching the MOSFETs into the conducting mode.

Resistors 684, 685, 686 and 687 prevent ringing or oscillation caused by the parasitic inductance and capacitance around the MOSFETs.

Resistors 688, 689, 690 and 691 ensure the MOSFETs remain in the high-impedance state when the diodes 604, 605, 606 and 607 are reverse-biased, i.e. when no fault current is flowing.

Figures 7 and 8 are oscillographs, which compare the respective AC voltage drop of a prior art galvanic isolator with the much lower voltage drop of the improved galvanic isolator according to the invention, with 100 Amps RMS flowing there through in both cases. The measured power dissipation is reduced from 110 Watts RMS to 6.7 Watts RMS.

The fault current handling capacity may be increased in a number of ways.

The current handling of the MOSFET array may be increased by using more devices in parallel.

The response time of the overcurrent protection circuit may be reduced.

The maximum rate of change of current (di/dt) may be reduced with a series connected inductor, whereby the overcurrent protection circuit is given more time to act.

Improvements in the reliability and fault tolerance capacity of a galvanic isolator under the worst foreseeable operating conditions are therefore disclosed herein. Such improvements are achieved through a significant reduction in overall power dissipation, such as by a factor of ten or more, relative to power dissipation characteristics of prior art designs.

The control circuit monitors the current flowing through the galvanic isolator and, at a predetermined level, automatically switches the bypass element into a very low resistance state, thereby reducing the potential difference across the galvanic isolator and proportionally reducing the power dissipation. During medium level fault conditions, such as the first phase of a worst-case fault as described above, the rise in temperature caused by the power dissipation within the safety critical components is reduced to substantially zero, whereby the surge handling capability of a galvanic isolator according to the invention is significantly increased, with a corresponding improvement in safety and reliability.

During high level fault conditions, such as the second phase of a worst-case fault as described above, the control circuit may automatically switch the bypass element into a high resistance state, particularly in the case of a high current surge which might otherwise damage the bypass element.

Additional benefits of low power dissipation and reduced temperature rise include improving the reliability of other components and equipment installed within or near the galvanic isolator, reducing the heat danger to nearby personnel and animals, and reducing the need for conventional cooling techniques based on the use of heatsinks, finned or otherwise, which are augmented by natural convection or forced air, thereby reducing the space and volume which the galvanic isolator occupies, as well as its cost and complexity of assembly.

Claims

1. A galvanic isolator comprising

a plurality of semiconducting elements;

earth connecting means for connecting the plurality of semiconducting elements to at least two sources of electric potential having a current flow there between;

control means adapted to switch the plurality of semiconducting elements into a low impedance state when a threshold voltage of the galvanic isolator is exceeded;

characterised in that the galvanic isolator further comprises an electronic bypass element adapted to bypass the plurality of semiconducting elements; and

an electronic control circuit adapted to monitor the current flowing through the earth connecting means and to switch the electronic bypass element from a high resistance state suitable for a current flow below a first preset level, to a very low resistance state when the current flow increases above the first preset level.

2. A galvanic isolator according to claim 1, wherein the electronic control circuit is further adapted to switch the electronic bypass element from the very low resistance state suitable for a current flow above the first preset level, to the high resistance state when the current flow increases above a second preset level higher than the first preset level.

3. A galvanic isolator according to claim 1 or 2, wherein the first preset level is comprised in the range of 20 Amps to 30 Amps.

4. A galvanic isolator according to claim 2 or claim 3 when depending on claim 2, wherein the second preset level is comprised in the range of 100 Amps to 140 Amps.

5. A galvanic isolator according to any preceding claim, wherein the semiconducting elements are selected from the group comprising diodes, silicon controlled rectifiers and transistors.

6. A galvanic isolator according to any preceding claim, wherein the electronic bypass element comprises an array of metal oxide semiconductor field effect transistors (MOSFETs).

7. A galvanic isolator according to claim 6, wherein the array is a parallel connected MOSFET array comprising N channel enhancement mode MOSFETs.

8. A galvanic isolator according to claim 6 or claim 7, wherein the electronic bypass element comprises a pair, or parallel connected pairs, of MOSFETs having body diodes, the body diodes being connected in opposition to prevent current flow when the MOSFETs are switched into a high impedance state.

9. A galvanic isolator according to claim 6 or claim 7, wherein the electronic bypass element comprises two pairs, or parallel connected pairs, of MOSFETs having body diodes, the body diodes being connected to conduct and allow current flow.

10. A galvanic isolator according to any preceding claim, further comprising status indicating means adapted to indicate AC fault current flowing or direct current flowing to a user.

11. A galvanic isolator according to claim 10, wherein the status indicating means comprises light emitting diodes (LEDs).

12. A galvanic isolator according to any preceding claim, further comprising a current transformer means adapted to power the electronic control circuit.

13. A galvanic isolator according to any preceding claim, further comprising mains supply connection means adapted to power the electronic control circuit.

14. A galvanic isolator according to any preceding claim, further comprising an enclosure for housing the galvanic isolator, the enclosure further comprising an overcurrent device or a residual current device or both an overcurrent device and a residual current device for limiting the prospective fault current available from a mains power supply, thereby limiting the maximum fault current flowing through the galvanic isolator.

15. A galvanic isolator according to any preceding claim, further comprising a monitoring element adapted to record events of significant amplitude, such as current surges and lightning strikes.

16. A galvanic isolator according to any preceding claim, further comprising surge protection means, the surge protection means comprising a transient voltage suppressor connected in parallel with the galvanic isolator or a series connected inductor, or both a transient voltage suppressor connected in parallel with the galvanic isolator and a series connected inductor.

17. A galvanic isolator according to any preceding claim, wherein a current transducer of the electronic control circuit is a current transformer.

18. A galvanic isolator according to any of claims 1 to 16, wherein a current transducer of the electronic control circuit is a magnetic field detection device such as a hall-effect device adapted to detect the magnetic field generated by the fault current.

19. A galvanic isolator according to any of claims 1 to 16, wherein a current transducer of the electronic control circuit is a low value series resistor with a voltage measuring circuit.

20. A galvanic isolator according to any preceding claim, wherein the diodes are adapted to withstand a surge of substantially 5000 Amps for approximately 0.5 seconds from a starting temperature of substantially 50°C.

21. A method of reducing the power dissipation of a galvanic isolator comprising a plurality of semiconducting elements, earth connecting means for connecting the plurality of semiconducting elements to at least two sources of electric potential having a current flow therebetween, an electronic bypass element adapted to bypass the plurality of semiconducting elements, and an electronic control circuit, the method comprising the steps of:

monitoring current flowing through the earth connecting means with the electronic control circuit; and

switching the electronic bypass element with electronic control circuit in dependence on the monitoring, from a high resistance state suitable for a current flow below a first preset level, to a very low resistance state when the current flow increases above the first preset level.

22. A method according to claim 21, wherein the step of switching comprises the further step of switching the electronic bypass element from the very low resistance state suitable for a current flow above the first preset level,

to the high resistance state when the current flow increases above a second preset level higher than the first preset level.

23. A method according to claim 21 or 22, wherein the first preset level is comprised in the range of 20 Amps to 30 Amps.

24. A method according to claim 22 or 23 when depending on claim 22, wherein the second preset level is comprised in the range of 100 Amps to 140 Amps.

25. A method according to any preceding claim, comprising the further step of switching the plurality of semiconducting elements into a low impedance state when a threshold voltage of the galvanic isolator is exceeded.

26. A galvanic isolator comprising an electronic bypass element comprising an array of metal oxide semiconductor field effect transistors (MOSFETs) having intrinsic body diodes;

earth connecting means for connecting the plurality of intrinsic body diodes diodes to at least two sources of electric potential having a current flow there between; and

an electronic control circuit adapted to monitor the current flowing through the earth connecting means, and to switch the electronic bypass element from a high resistance state suitable for a current flow below a first preset level, to a very low resistance state when the current flow increases above the first preset level.

27. A galvanic isolator according to claim 26, wherein the electronic control circuit is further adapted to switch the electronic bypass element from the very low resistance state suitable for a current flow above the first preset

level, to the high resistance state when the current flow increases above a second preset level higher than the first preset level.

28. A galvanic isolator according to claim 26 or 27, wherein the first preset level is comprised in the range of 20 Amps to 30 Amps.

29. A galvanic isolator according to claim 27 or claim 28 when depending on claim 28, wherein the second preset level is comprised in the range of 100 Amps to 140 Amps.

30. A galvanic isolator according to any of claims 26 to 29, wherein the array is a parallel connected MOSFET array comprising N channel enhancement mode MOSFETs.

31. A craft incorporating a galvanic isolator according to any of claims 1 to 20, wherein the at least two sources of electric potential respectively comprise a shore source and a craft source.

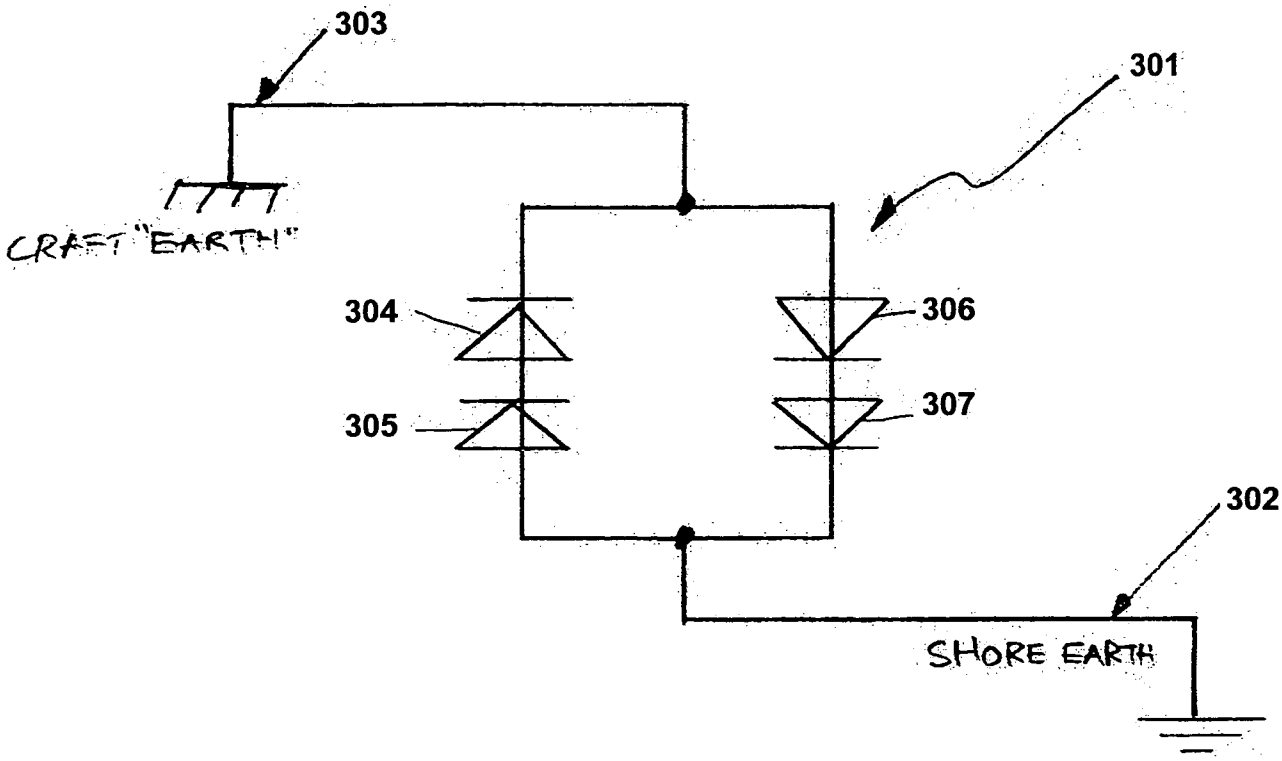
32. A craft incorporating a galvanic isolator according to any of claims 26 to 30, wherein the at least two sources of electric potential respectively comprise a shore source and a craft source.

33. A galvanic isolator substantially as hereinbefore described, with reference to and as shown in Figure 3 of the accompanying drawings.

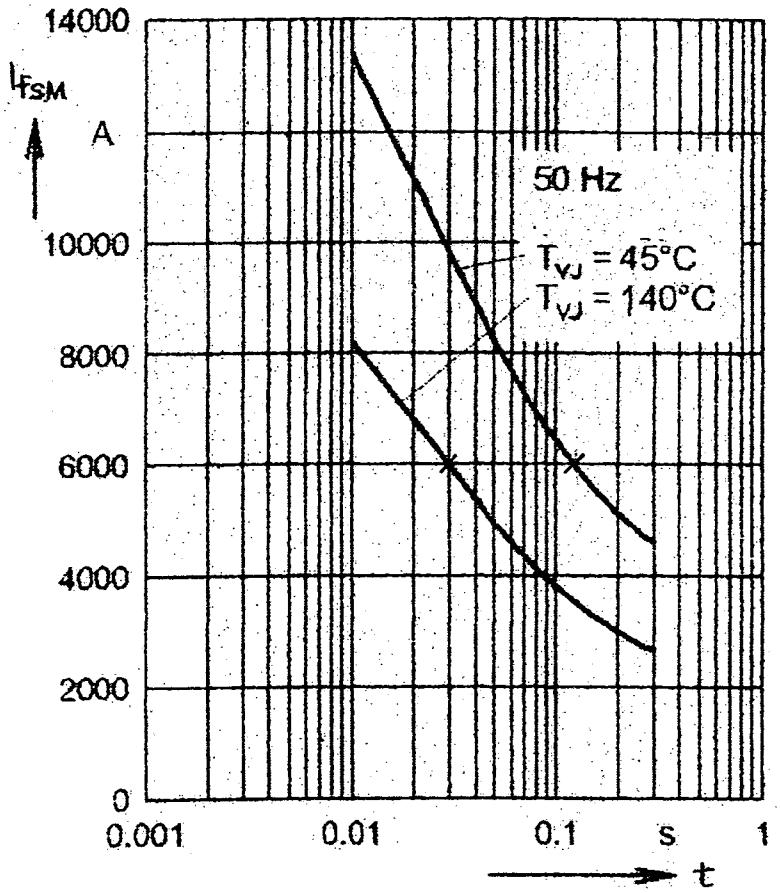
34. A galvanic isolator substantially as hereinbefore described, with reference to and as shown in Figure 4 of the accompanying drawings.

35. A galvanic isolator substantially as hereinbefore described, with reference to and as shown in Figure 5 of the accompanying drawings.

36. A galvanic isolator substantially as hereinbefore described, with reference to and as shown in Figure 6 of the accompanying drawings.



(PRIOR ART)
FIGURE 1



Surge overload current
I_{FSM}: Crest value, t: duration

FIGURE 2

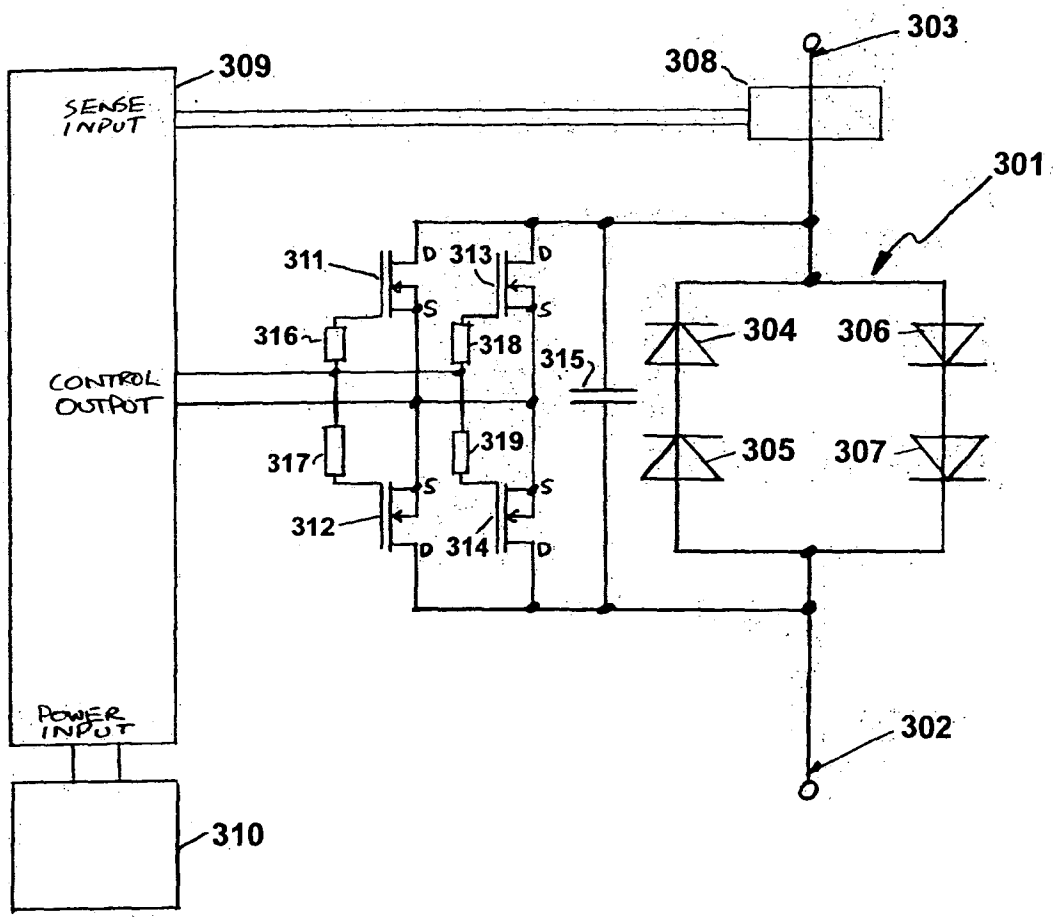

303
309
308
SENSE INPUT
301
311
313
D
S
316
318
315
304
306
CONTROL OUTPUT
317
319
312
314
305
307
302
POWER INPUT
310

FIGURE 3

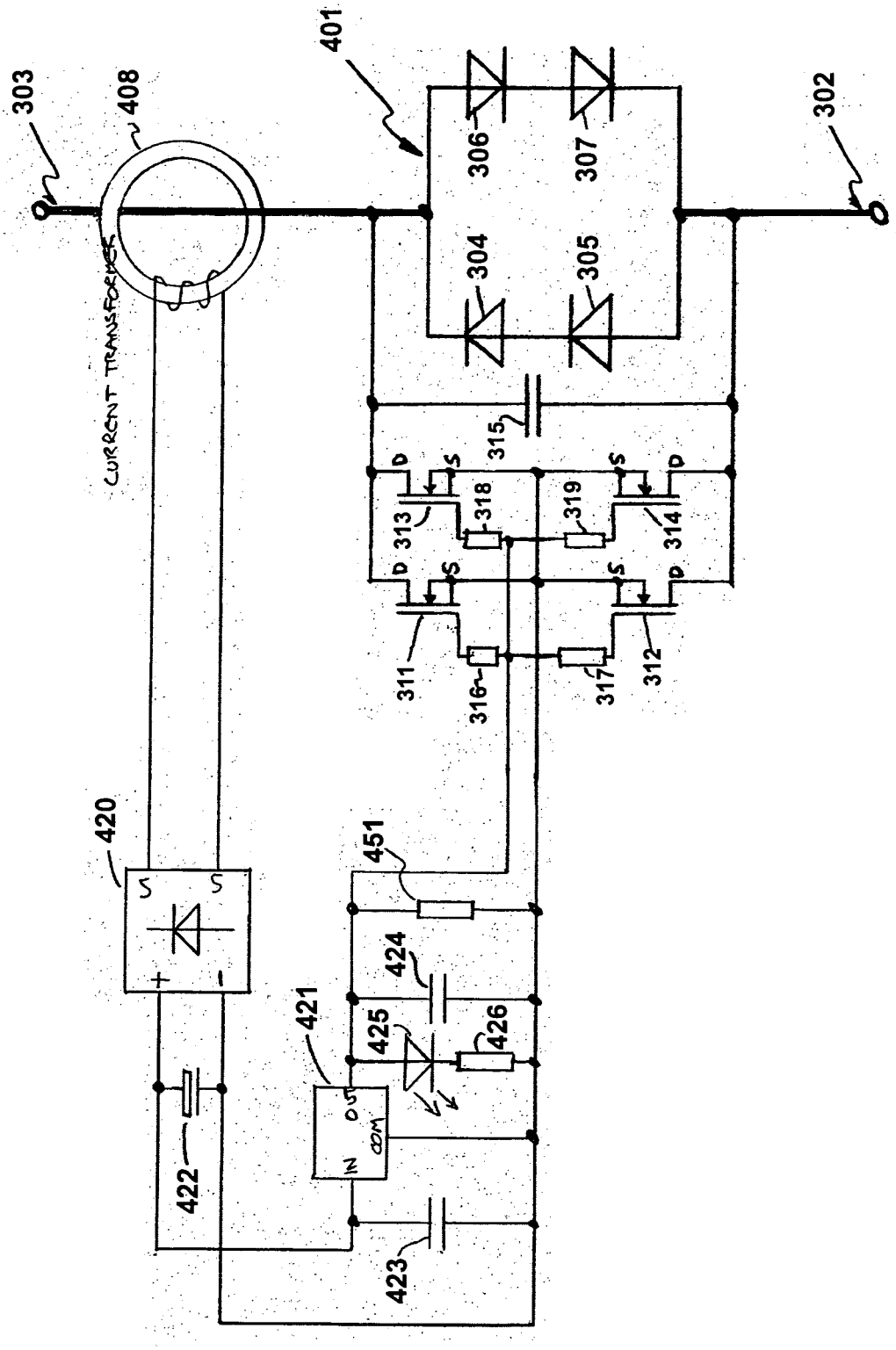

303
408
401
302
306
307
304
305
315
313
318
319
314
311
316
317
312
420
451
424
421
425
426
422
423
CURRENT TRANSFORMER
S
D
IN
COM
OUT
+
-

FIGURE 4

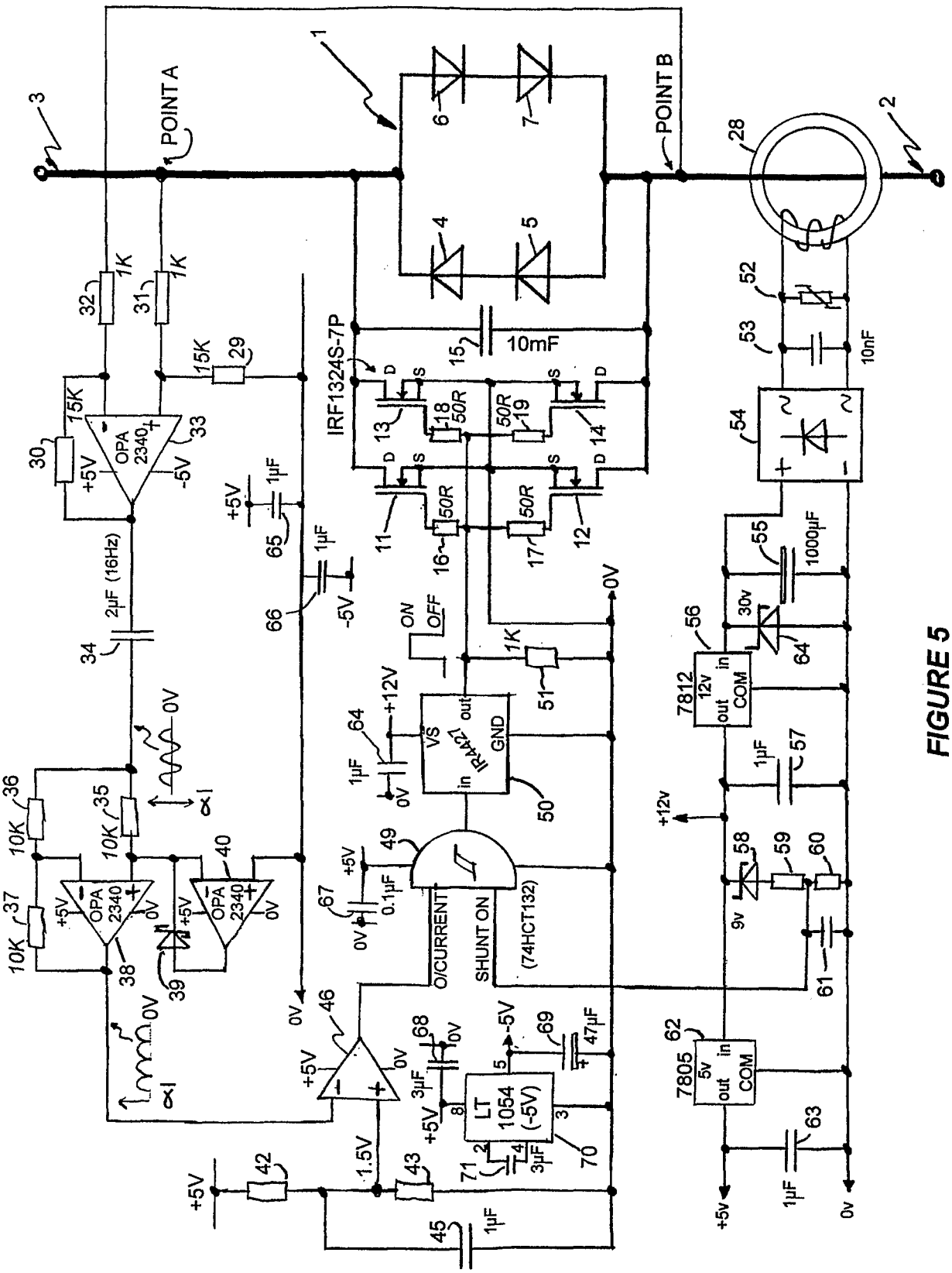

POINT A
POINT B
IRF1324S-7P
10mF
OPA 2340
LT 1054 (-5V)
74HCT132
O/CURRENT
SHUNT ON
ON
OFF
7812
7805
1K
15K
10K
50R
2µF (16Hz)
1µF
3µF
47µF
0.1µF
1000µF
10nF
+5V
-5V
+12V
0V
1.5V
9v
30v

FIGURE 5

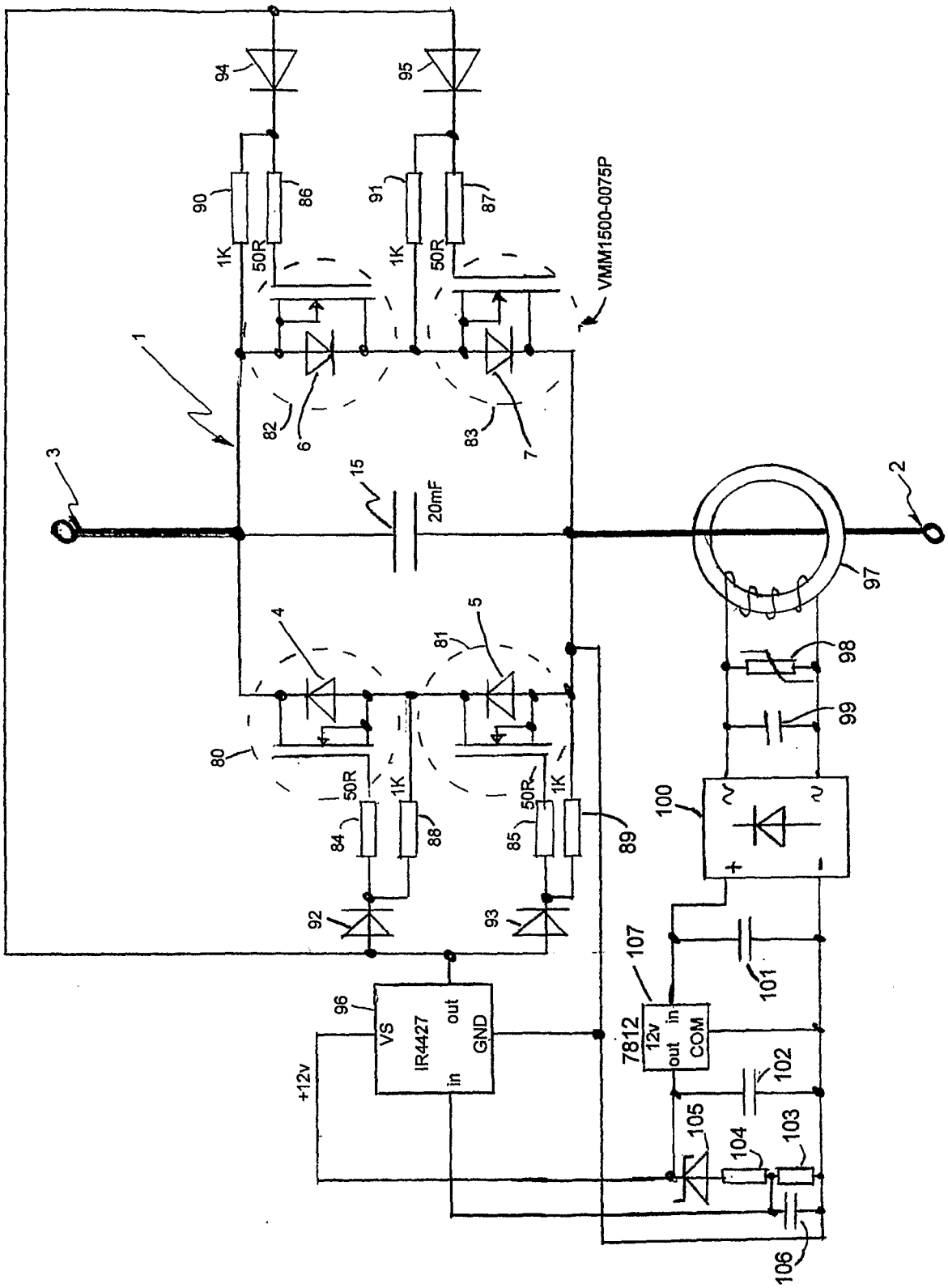
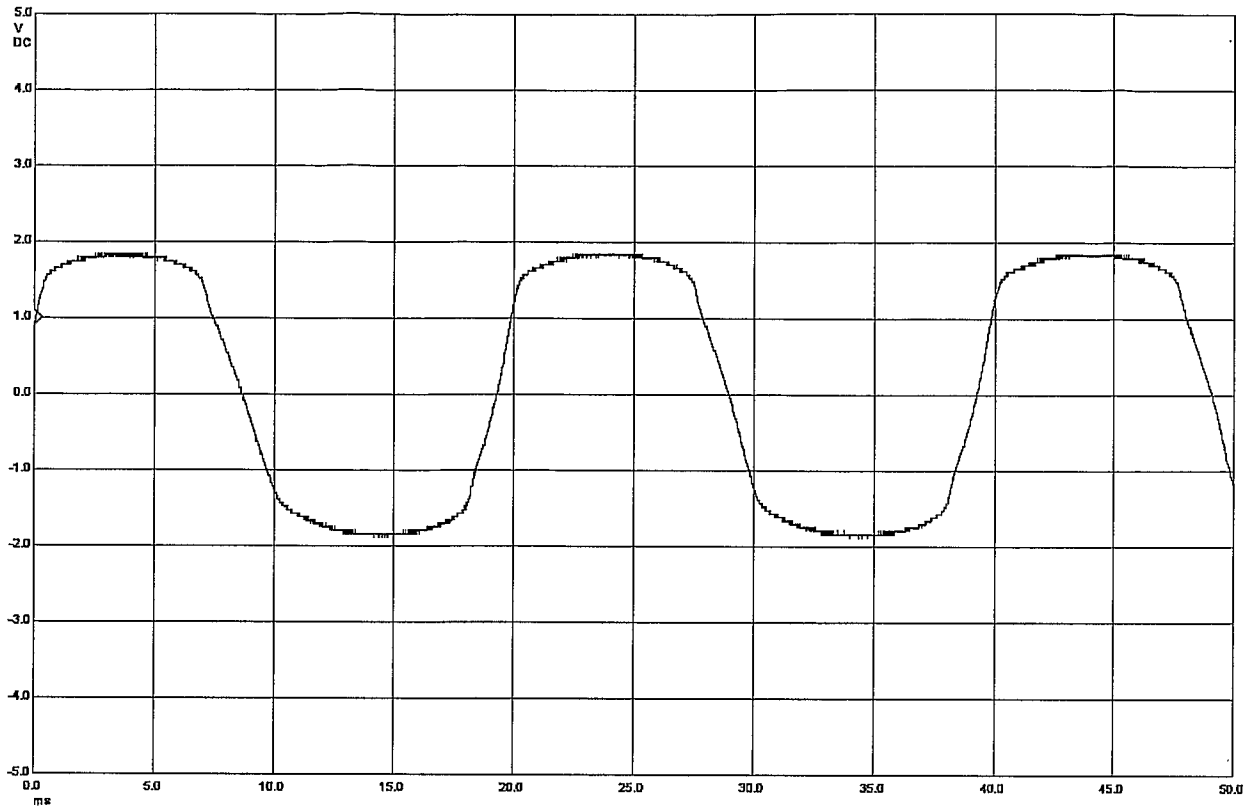

94
95
90
86
91
87
1K
50R
1K
50R
VMM1500-0075P
1
82
6
83
7
3
15
20mF
2
97
4
81
5
98
99
80
50R
1K
50R
1K
84
88
85
89
100
92
93
107
101
96
VS
IR4427
out
in
GND
+12v
7812
12v
out in
COM
102
105
104
103
106

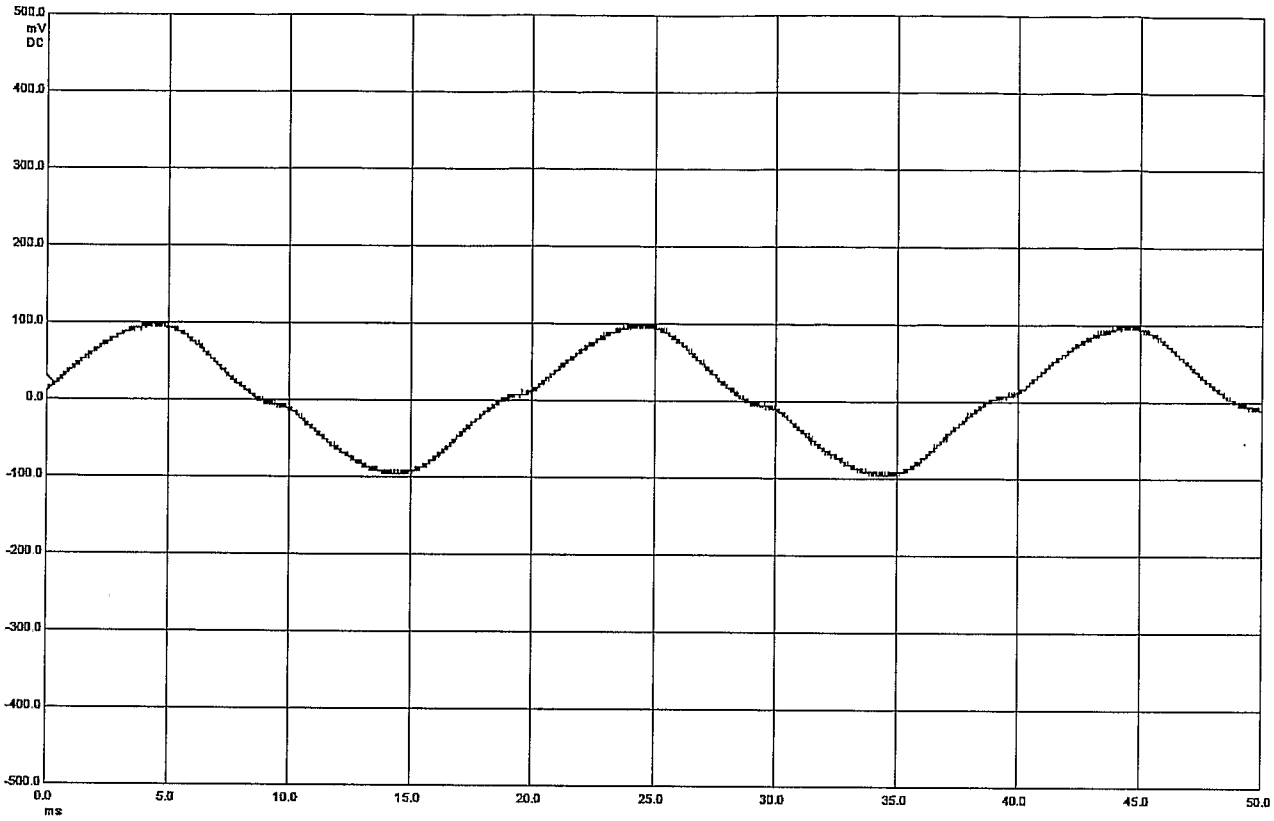
FIGURE 6



Prior art galvanic isolator carrying 100 Amps r.m.s.

Horizontal scale:	*5 millisec per division.*
Vertical scale:	*500 millivolt per division.*
Power dissipation:	*110 Watts*

Figure 7 (Prior art)



Galvanic isolator (per Figure 5) carrying 100 Amps r.m.s.

Horizontal scale:	*5 millisec per division.*
Vertical scale:	*50 millivolt per division.*
Power dissipation:	*7 Watts*

Figure 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2009/000619

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02H9/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 856 904 A (PELLY BRIAN R [US] ET AL) 5 January 1999 (1999-01-05) column 1, line 1 - column 17, line 23; figures 2-4	1-32
X	US 5 751 530 A (PELLY BRIAN R [US] ET AL) 12 May 1998 (1998-05-12) column 7, line 33 - column 10, line 5; figures 2-4	1-32

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 November 2009	01/12/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Meulemans, Bart

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2009/000619

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [X] Claims Nos.: 33-36
because they relate to subject matter not required to be searched by this Authority, namely:

Claims 33 to 36 rely on references to the drawings, which does not comply with Rule 6.2(a) PCT.

2. [X] Claims Nos.: 33-36
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

see FURTHER INFORMATION sheet PCT/ISA/210

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. [ ] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

[ ] The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

[ ] No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.1

Claims Nos.: 33-36

Claims 33 to 36 rely on references to the drawings, which does not comply with Rule 6.2(a) PCT.

Continuation of Box II.2

Claims Nos.: 33-36

Claims 33 to 36 rely on references to the drawings, which does not comply with Rule 6.2(a) PCT.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.2), should the problems which led to the Article 17(2)PCT declaration be overcome.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2009/000619

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5856904 A	05-01-1999	CA 2214586 A1	15-05-1998
US 5751530 A	12-05-1998	NONE	