Dec. 2, 1969 G. C. M. E. WOLFRUM ET AL 3,482,150

PLANAR TRANSISTORS AND CIRCUITS INCLUDING SUCH TRANSISTORS

Filed June 14, 1967 4 Sheets-Sheet 1

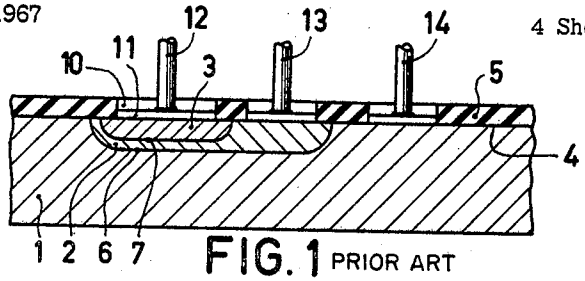

FIG. 1 PRIOR ART

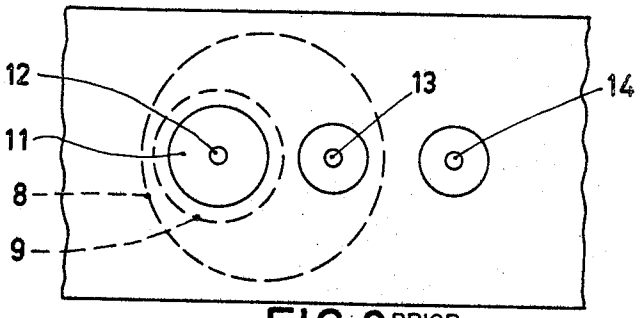

FIG. 2 PRIOR ART

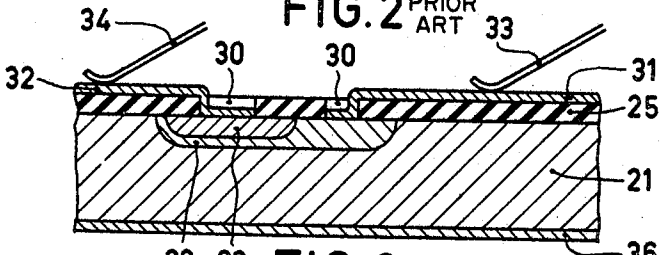

FIG. 3 PRIOR ART

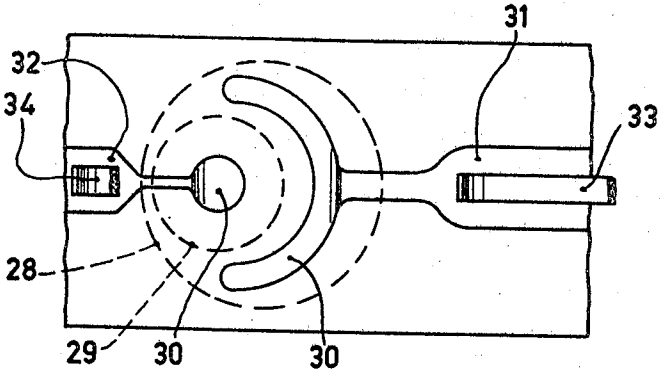

FIG. 4 PRIOR ART

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PLANAR TRANSISTORS AND CIRCUITS INCLUDING SUCH TRANSISTORS

Filed June 14, 1967

4 Sheets-Sheet 2

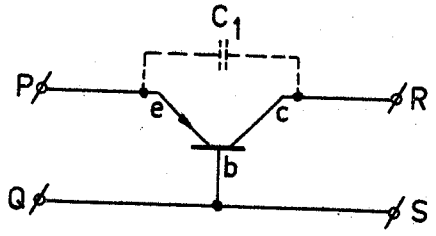

FIG. 19

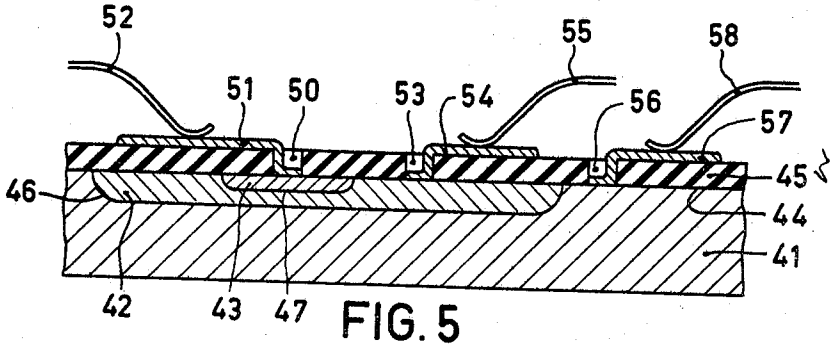

FIG. 5

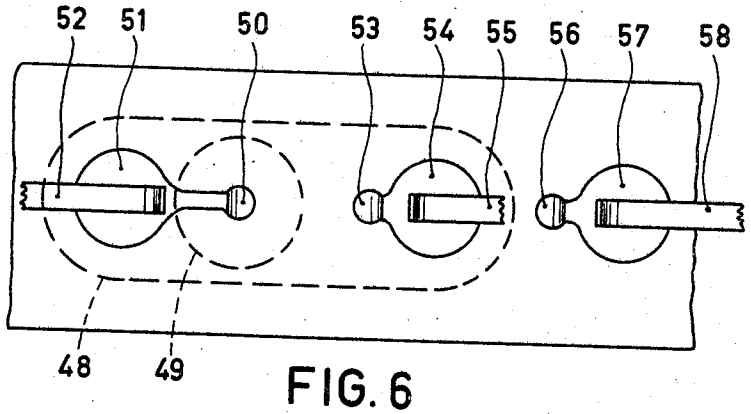

FIG. 6

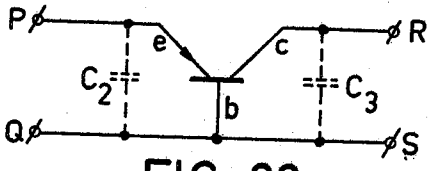

FIG. 20

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Dec. 2, 1969 G. C. M. E. WOLFRUM ET AL 3,482,150

PLANAR TRANSISTORS AND CIRCUITS INCLUDING SUCH TRANSISTORS

Filed June 14, 1967

4 Sheets-Sheet 3

FIG. 7

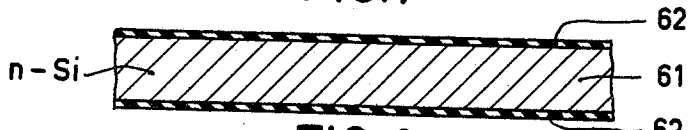

FIG. 8

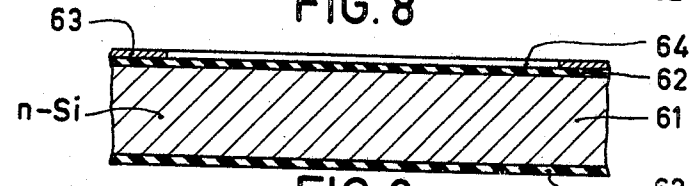

FIG. 9

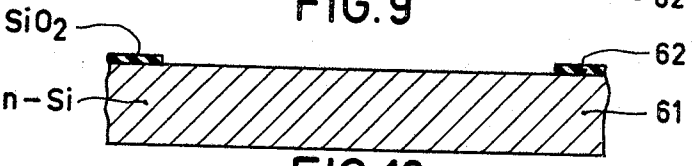

FIG. 10

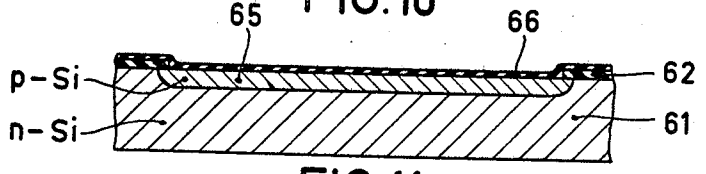

FIG. 11

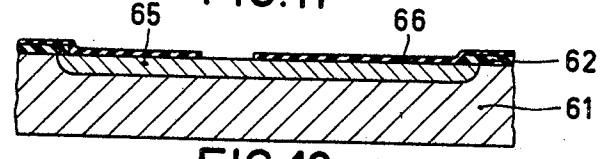

FIG. 12

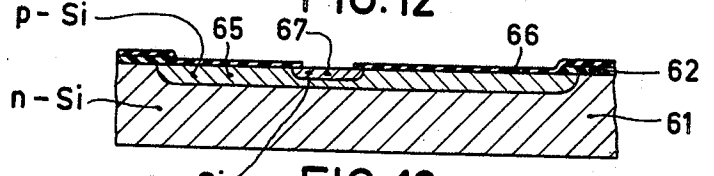

FIG. 13

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PLANAR TRANSISTORS AND CIRCUITS INCLUDING SUCH TRANSISTORS

Filed June 14, 1967 4 Sheets-Sheet 4

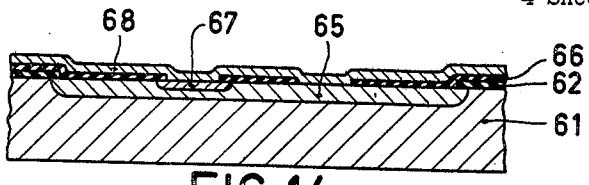

FIG. 14

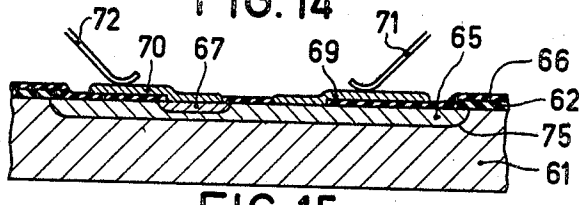

FIG. 15

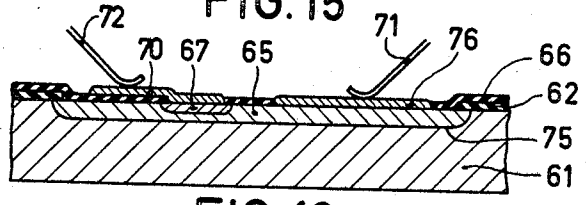

FIG. 16

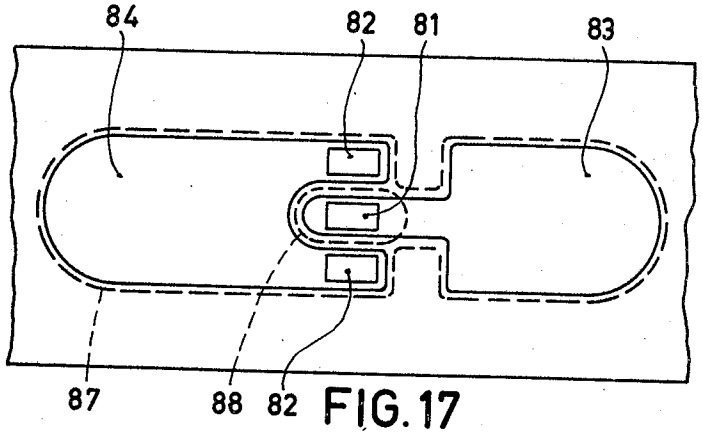

FIG. 17

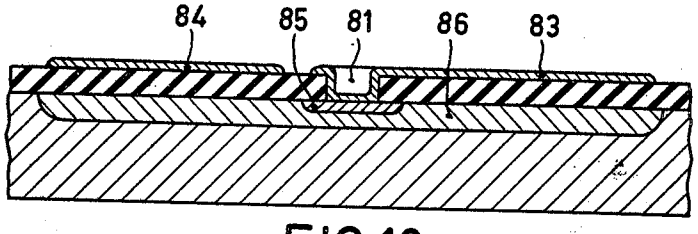

FIG. 18

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Patented Dec. 2, 1969

3,482,150

PLANAR TRANSISTORS AND CIRCUITS INCLUDING SUCH TRANSISTORS

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Filed June 14, 1967, Ser. No. 646,041
Claims priority, application Netherlands, June 29, 1966, 6609002
Int. Cl. H01l 3/00, 5/00
U.S. Cl. 317—234 4 Claims

ABSTRACT OF THE DISCLOSURE

A planar transistor intended for high frequency applications and containing a tiny emitter region and a tiny hole in an overlying insulating layer for making connection to the emitter via a wire lead or supply conductor which is too large to fit through the emitter window. The contact to the emitter is made by a conductive deposit or pad on the insulator and extending into the window. To reduce feedback capacitance when the transistor is used in a grounded base circuit, the base region is laterally extended so that the wire lead connection to the emitter pad lies wholly over the base spaced laterally from the collector.

This invention relates to transistors comprising a semiconductor body having a first region, the collector region, of a first conductivity type, a second region, the base region, of the opposite conductivity type, and a third region, the emitter region, of the first conductivity type, the third region being surrounded by the second and the second region being surrounded by the first, in each case except an area defined by a boundary surface of the body, the regions being separated by junctions which are intersected by the said surface in accordance with closed figures and the said surface carrying a thin insulating layer covering the areas at which the junctions intersect the surface, which layer carries a conductive layer which contacts the emitter region through a window in the insulating layer and which extends over the insulating layer laterally of the window, forming in situ a contact area located above the collector region for connection of a supply conductor. Such a transistor constitutes one determined embodiment of a planar transistor.

In an embodiment described in U.S. patent specification No. 3,025,589 supply wires are secured in windows of the insulating layer located above the areas at which the emitter and base regions are bounded by the said boundary surface. Since these windows, especially the window for the emitter region, are very small in practical embodiments of said transistors, it has been suggested in U.S. patent specification No. 2,981,877 to cover the insulating layer with enlarged conductive layers which contact the emitter and base regions through windows and which extend over the collector region laterally of the windows but are insulated from this region by the insulating layer, so that a much larger surface area is available for connection of supply conductors.

It has been found that in such transistors the potential between the collector region on the one hand and the emitter or base region on the other must be maintained below a comparatively low limit, which may lie much lower than the breakdown voltage of the junction between the collector and base regions. If the limit is exceeded breakdown of the insulating layer occurs.

An object of the invention is inter alia to provide a construction of a planar transistor in which the maximum

potential between the collector region on the one hand and the base or emitter region on the other is not limited or hardly by properties of the insulating layer, but is limited by the junction betwen the collector and base regions, while the said conductive layer may still be extended sufficiently for the attachment of supply conductors.

In transistors of the kind described, in which the insulating layer is covered by a conductive layer which contacts the emitter region through a window in the insulating layer and which extends over the collector region, a capacity occurs between the conductive layer and the collector region. This capacity causes feedback, for example, when the transistor is used as an amplifying element in a grounded-base connection for amplifying an electrical signal. This feedback may become very troublesome in high-frequency uses.

In a grounded-base connection the base of the transistor is common to the input and output circuits, while the signals to be amplified are fed to the emitter and the amplified signals are derived from the collector.

Another object of the invention is to eliminate the capacity causing feedback.

According to the invention the base region extends beside the emitter region to such an extent that the contact area connected to the emitter region lies wholly above the base region. This contact area or bonding pad is separated from the collector region not only by the insulating layer but also by the base region and the junction between the base and collector regions.

When the transistor according to the invention is used in grounded-base or common base connection, the said capacity causing feedback does not occur since the base region constitutes a shield layer between the collector region and the metal layer connected to the emitter-region. This is at the expense of an increase in base-collector capacity and base-emitter capacity. In circuits of the kind described, these increased capacities are often less interfering than the capacity causing feedback.

If the transistor according to the invention is a high voltage transistor, it is not the total emitter-collector voltage which appears across the insulating layer in operation but only the considerably lower emitter-base voltage, thus avoiding the risk of breakdown of the insulating layer under the metal layer connected to the emitter region.

One important preferred embodiment of a transistor according to the invention is characterized in that a further conductive layer or bonding pad is provided which contacts the base region through a window in the insulating layer and which forms a contact area located wholly above the base region for connection of a further supply conductor.

The conductive layer connected to the base region thus extends completely above the base region, thus avoiding breakdown of the insulating layer if a large potential difference occurs between the base and collector regions.

As will appear hereinafter, the said insulating layer, insofar located between the base region and the conductive layer connected thereto, no longer has an insulating function. Consequently, in one embodiment of the invention, the conductive layer connected to the base region lies completely within a window of the insulating layer.

The invention also relates to a circuit for amplifying electrical signals, including a transistor according to the invention, which is characterized in that the base is common to the input and output circuits, the signals to be amplified being fed to the emitter and the amplified signals being derived from the collector.

In order that the invention may be readily carried into effect it will now be described in detail, by way of

example, with reference to the accompanying diagrammatic drawings, in which:

FIGURES 1 and 3 are sectional views of known transistors;

FIGURES 2 and 4 are plan views of these transistors;

FIGURE 5 is a sectional view of a transistor according to the invention;

FIGURE 6 is a plan view of this transistor;

FIGURES 7 to 16 show several stages of the manufacture of such a transistor;

FIGURE 17 is a plan view and

FIGURE 18 is a sectional view of a transistor according to the invention;

FIGURES 19 and 20 show circuit diagrams to which the invention relates.

All the figures are shown diagrammatically and on a greatly enlarged scale.

The transistor of FIGURE 1 comprises a collector region **1**, which may consist of, for example, n-type silicon, a p-type base region **2** and an n-type emitter region **3**. Each of the last-mentioned two regions are surrounded by the preceding region, except at the areas at which they are bounded by the surface **4**. This surface is covered with a thin insulating layer **5** which cover inter alia the areas at which junctions **6** and **7** between the regions intersect the surface **4**. This intersection takes place along closed lines which are shown as broken lines in FIGURE **2** and indicated by the numerals **8** and **9**. Above the emitter region the insulating layer **5** is provided with a window **10** whose contact layer **11** and a supply conductor **12** form the emitter connection. A base connection **13** and a collector connection **14** are formed in a similar manner. It will be evident that in such a transistor very little space is available, especially for forming the emitter and base connections.

A much large space is available therefor in the transistor shown in FIGURES 3 and 4. This transistor comprises a collector region **21**, a base region **22** and an emitter region **23**. Above the last-mentioned two regions, an insulating layer **25** is provided with windows **30**, but the conductors contacting the associated regions now have the form of enlarged metal layers **31** and **32** which extend at the sides of the windows and above the collector region **21** to form bonding pads where they are connected to supply conductors **33** and **34**. It will be evident that in this case the full potential occurring between the collector on the one hand and the base on the other appears across the insulating layer **25**. The same is true of the potential between the collector and the emitter, which is usually almost equally high. If these potentials are high, for example higher than 300 volts, there is a great chance of breakdown occurring in the layer **25**.

When the transistor is used as an amplifying element in a grounded-base connection for amplifying electrical signals the capacity between the metal layer **32** and the collector region **21** causes feedback. FIGURE 19 shows a diagram of such a circuit. The emitter, the base and the collector of the transistor are indicated by E, B and C respectively, and the capacity causing feedback is indicated by C_1. The signals to be amplified are fed to terminals P and Q and the amplified signals are derived from terminals R and S.

It should be noted that in this transistor, as will be be seen from FIGURE 4, the window located above the base region partly surrounds the window above the emitter reigon. The junctions between the regions are again shown in broken lines in FIGURE 4 and indicated by the numerals **28** and **29**. The collector connection is in this case formed as a conductive layer **36** at the underside of the transistor.

A first embodiment of a transistor according to the invention is shown in FIGURES 5 and 6. This transistor comprises a collector region **41**, a base region **42** and an emitter region **43**. These regions are bounded by the surface **44** which carries an insulating layer **45**. Junc-

tions **46** and **47** between the regions intersect the said surface along closed curves **48** and **49** shown in broken lines in FIGURE 6. Above the emitter region **43**, the insulating layer **45** is provided with a small window **50** where a conductive layer **51** contacts the said region. The layer **51** is enlarged relative to the window **50** to extend beside the window, over the insulating layer to form an enlarged bonding pad and is connected in situ to a supply conductor **52**. Similarly, above the base region **42**, a small window **53** is provided together with an enlarged conductive layer **54** and a supply conductor **55**. In this transistor the base region **42** extends on each side of the emitter region **43** to an extent such that the conductive layers **51** and **54** lie completely above the base region and hence within the boundary defined by the line **48** (FIGURE 6).

In this case the breakdown voltage between the conductive layers **51** and **54** on the one hand and the collector region **41** on the other, is determined not only by the properties of the insulating layer **45** but also and substantially by the junction **46** between the collector and base regions.

When the transistor is used in the circuit shown in FIGURE 19, the capacity C_1 causing feedback does not occur. Instead of the capacity C_1 there occurs inter alia a capacity C_2 (see FIGURE 20). This is the capacity between the metal layer **51** and the base region **42**. Further, an additional base-collector capacity C_3 occurs which is caused by an enlargement of the base region. So the capacity C_1 may be regarded to be replaced by the capacities C_2 and C_3, which in many cases are considerably less interfering than the capacity C_1.

The connection to the collector region is obtained by means of a window **56** in the insulating layer **45**, a conductive layer **57** which in the window contacts the collector region, and a current-supply conductor **58**.

The manufacture of such a transistor will now be described by way of example, A silicon disc **61** of the n-type having a resistivity of 100 Ω cm., a cross-section of 25 mms. and a thickness of 250 microns (FIGURE 7) is covered with an insulating silicon-dioxide layer **62** (FIGURE 8) by heating in moist oxygen at 1200° C. for two hours. A large number of transistors will be manufactured from the disc simultaneously and in the same usual manner. The manufacture of one of these transistors will be described hereinafter.

The upper side of the disc is covered with a photosensitive masking layer **63** which is illuminated in accordance with a determined pattern representing the outlines of the base region to be formed, then developed and partly dissolved, resulting in apertures **64** being formed in the layer **63** (FIGURE 9). Subsequently the disc **62** is introduced into an etching bath consisting of 40 gms. of ammonium fluoride (NH_4F) dissolved in 60 mls., of water, to which 6 mls. of concentrated hydrofluor (HF) have been added. The silicon dioxide, insofar not covered by the masking layer **63**, is dissolved in the said bath (FIGURE 10), whereupon the residue of the mask **63** is removed.

The base region is manufactured in three stages. First a thin layer of boron oxide (B_2O_3) is vapour deposited at 900° C. in dry nitrogen for 30 minutes. Subsequently a first diffusion in moist oxygen takes place at 1200° C. for 2 hours, followed by an after-diffusion in dry nitrogen at 1280° C. for 24 hours. Now a base region **65** of the p-type has been formed, while the window in the layer **62** is closed again by a vitreous boron-containing oxide layer **62** (FIGURE 11).

In a similar manner as described above, a window having the size of the emitter region to be formed is etched in the insulating layer **66** (FIGURE 12) with the aid of a photosensitive masking layer which is illuminated, developed and dissolved. The disc **61** is subsequently heated in phosphorous vapour at 1070° C. for two hours, resulting in an emitter region **67** consisting of n-type silicon being formed.

In the manner previously described, windows are again formed in the insulating layer **66** with the aid of a photosensitive masking layer, whereupon an aluminium layer **68** is vapour deposited onto the whole upper side of the disc (FIGURE 14). Lastly, the unwanted portions of the aluminium layer **68** are removed, again with the aid of a photographic mask, so that conductive layers **69** and **70** remain which contact the base region **65** and the emitter region **67**. Current-supply conductors **71** and **72** may be secured to the said conductive layers by so-called "thermo-compression bonding" (FIGURE 15).

The maximum potential which is permissible between the conductive layers **69** and **70** on the one hand and the collector region on the other is again determined substantially by the properties of junction layer **75** between the base and emitter regions, and this potential may be a multiple of the maximum potential to be applied across an oxide layer.

It is to be noted that, in the present example, the window above the base region may, without objection, be made much larger so that the conductive layer which contacts the base region comes to lie only within this window and not on the insulating layer **66**. This conductive layer is indicated by **76** in FIGURE 16.

The connection to the collector region may be made in the usual manner beside the emitter and base connections in a window, or at the lower side of the disc **61**.

As shown in FIGURE 17, a more practicable embodiment of a transistor according to the invention has an emitter window **81** which lies between two base windows **82**. Conductive layers **83** and **84** in the windows contact an emitter region **85** and a base region **86** respectively. The lines along which the junctions between the various regions intersect the semiconductor surface are indicated by the numerals **87** and **88** in FIGURE 18.

It will be evident that the use of the invention is not confined to the geometries above described, which are intended only by way of example. The invention is applicable more particularly to interdigital and similar geometries.

What is claimed is:

1. A transistor comprising a semiconductor body having a collector region of one type conductivity, a base region of the opposite type conductivity inset in the collector region forming a collector p-n junction extending to a major planar surface of the body, and a tiny emitter region of the one type conductivity inset in the base region forming an emitter p-n junction extending to said major planar surface, the collector, base and emitter regions all having substantial surface areas accessible at said major planar surface, a thin insulating layer on said major planar surface and covering the areas at which the p-n junctions intersect the said major planar surface, a base window opening in said insulating layer over the base region surface area, a base conductive contact in the base window and on the surface of said base region, a base supply conductor bonded to said base contact, a tiny emitter window opening in said insulating layer over the emitter region surface area, an emitter conductive contact on the insulating layer and extending through the emitter window into contact with the emitter region, the lateral extent of said emitter contact being substantially larger than that of the emitter window and being limited to an area located wholly within that encompassed by the collector junction and over the base and emitter regions and laterally spaced from the collector surface area, and an emitter supply conductor bonded to the emitter contact at an area spaced from the emitter window and overlying the base region and laterally spaced from the collector surface area, said emitter supply conductor being too large to fit within the emitter window.

2. A transistor as set forth in claim **1** wherein the base conductive contact comprises a conductive layer on the insulator and extending through the base window into contact with the base region, said base conductive layer being located wholly above the base region.

3. A transistor as set forth in claim **1** wherein the base conductive contact lies completely within the base window.

4. An amplifying circuit including a transistor as set forth in claim **1** and comprising an input circuit coupled to the emitter supply conductor, and an output circuit coupled to the collector region, said base supply condutor being connected in common to the input and output circuits.

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JAMES D. KALLAM, Primary Examiner

R. F. POLISSACK, Assistant Examiner

U.S. Cl. X.R.

317—235

PO-1050
(5/69)

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,482,150 Dated December 2, 1969

Inventor(s) G. C. M. E. WOLFRUM ET AL

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 1, Author's name, "Theodor" read --Theodoor--;

Col. 3, line 63, "be seen from" read --seen from--.

Signed and sealed this 14th day of July , 19 70 .

(SEAL)
Attest:

Edward M. Fletcher, Jr.
Attesting Officer

WILLIAM E. SCHUYLER, JR.
Commissioner of Patents