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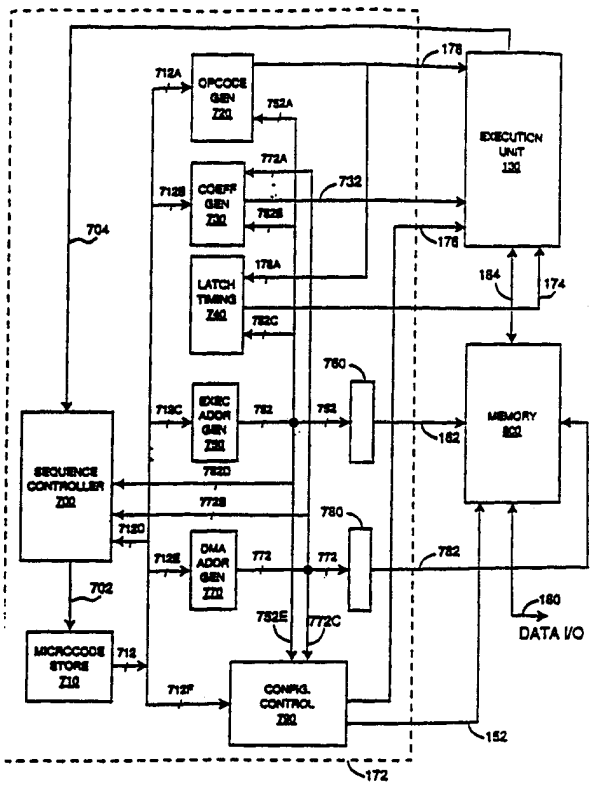
12 August 1999 (12.08.99)

(54) Title: PROCESSOR INTERFACING TO MEMORY MAPPED COMPUTING ENGINE

(57) Abstract

A method of interfacing a processor bus to a computation engine having a microprogrammable memory-centric controller and an array of memory, comprising the steps of providing a predetermined series of microcode instructions for execution by the MCC; selecting a start address within the series of microcode instructions for carrying out a corresponding operation; and executing the series of microcode instruction in the MCC beginning at the selected start address so as to carry out the corresponding operation in the engine. The present invention is useful in a wide variety of signal processing applications including programmable MPEG encode and decode, graphics, speech processing, image processing, array processors, etc. In telecommunications, the invention can be used, for example, for switching applications in which multiple I/O channels are operated simultaneously.



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INTERNATIONAL SEARCH REPORT

Inte. .ional Application No
PCT/US 98/10549

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F9/38 G06F9/24 G06F13/16 G11C7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ERTEM M C: "A RECONFIGURABLE CO-PROCESSOR FOR MICROPROCESSOR SYSTEMS" PROCEEDINGS OF THE SOUTHEAST CONFERENCE, TAMPA, APRIL 5 - 8, 1987, vol. 1, 5 April 1987, pages 225-228, XP000212298 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS	1,2,4-7, 16
Y	see the whole document	8-13, 17-20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 May 1999	26.05.99

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Daskalakis, T

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INTERNATIONAL SEARCH REPORT

Inter. ..ional Application No
PCT/US 98/10549

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	A. C. DAVIES ET AL.: "Interfacing a Hardware Multiplier to a General-purpose Microprocessor" MICROPROCESSORS AND MICROSYSTEMS., vol. 1, no. 7, October 1977, pages 425-431, XP000212024 LONDON GB see page 427	8,11-13
Y	PATENT ABSTRACTS OF JAPAN vol. 097, no. 006, 30 June 1997 & JP 09 034783 A (MITSUBISHI ELECTRIC CORP), 7 February 1997 see abstract	9,10, 17-20
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X	US 4 862 407 A (FETTE BRUCE A ET AL) 29 August 1989 see the whole document	1,2,4-7
A	US 5 230 042 A (MASAKI YASUO ET AL) 20 July 1993 see the whole document	1,16
A	WO 94 12929 A (S MOS SYSTEMS INC) 9 June 1994 see the whole document	3,4
A	US 5 448 715 A (LELM CHARLES A ET AL) 5 September 1995 see the whole document	9,10, 17-20
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A	DE 44 32 217 A (MITSUBISHI ELECTRIC CORP) 16 March 1995 see column 7, line 52 - column 9, line 50; figure 2	9,10, 17-20
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A	US 5 396 634 A (ZAIDI SYED A A ET AL) 7 March 1995 see column 4, line 1 - column 5, line 11	14,15

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 98/10549

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-7, 16

   A computation engine comprising memory, execution unit, controller and bus interface, and a method of interfacing a processor to a computation engine comprising the step of providing a series of microcode instructions in a non-volatile memory accessible to said computation engine by downloading the said series of microcode instructions under processor control.

2. Claims: 8 and 11-15

   A method of interfacing a processor to a memory mapped computation engine

3. Claims: 9, 10 and 17-20

   A computation engine comprising in tandem an SRAM buffer and a DRAM memory array to store data transferred from a processor, and a method of interfacing said processor to said computation engine.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte. ..tional Application No
PCT/US 98/10549

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