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(54) Title: METHOD FOR PRODUCING TWO N-TYPE BURIED LAYERS IN AN INTEGRATED CIRCUIT

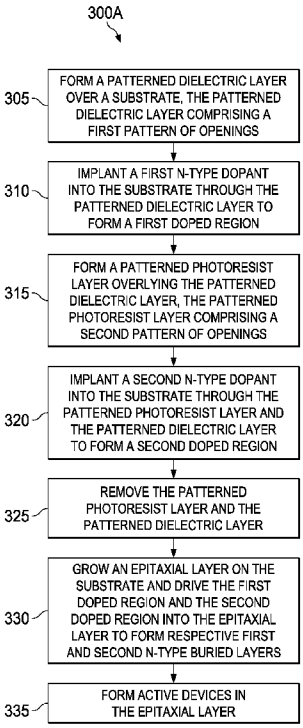

FIG. 3A

(57) Abstract: A method (300 A) of fabricating an integrated circuit includes forming (305) a patterned dielectric layer, which includes a first pattern of openings, over a substrate and implanting (310) a first n-type dopant into the substrate through the patterned dielectric layer to form a first doped region. The method continues with forming (315) a patterned photoresist layer overlying the patterned dielectric layer, which includes a second pattern of openings and implanting (320) a second n-type dopant into the substrate through the patterned photoresist layer and patterned dielectric layer to form a second doped region. The patterned photoresist layer and patterned dielectric layer are removed (325). An epitaxial layer is grown (330) on the substrate, and the first doped region and second doped region are driven (330) into the epitaxial layer to form respective first and second n-type buried layers, and then active devices are formed (335) in the epitaxial layer.

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[Continued on next page]

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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METHOD FOR PRODUCING TWO N-TYPE BURIED LAYERS IN AN INTEGRATED CIRCUIT

[0001] This relates generally to manufacturing semiconductor devices, and more particularly to producing two n-type buried layers in an integrated circuit.

BACKGROUND

[0002] Semiconductor manufacturing requires highly controlled processing in an ultra-clean environment and can be a very expensive process. Manufacturers are constantly looking for ways to improve the flow, shorten the processing time and/or lower the costs of production for a given process, such as implanting two different buried layers on a single chip.

SUMMARY

[0003] In described examples of a method of forming two n-type regions in a substrate, the method includes: implanting a first n-type dopant into the substrate through openings in a dielectric layer that is patterned for a first region; forming a first photoresist layer overlying the dielectric layer, the first photoresist layer being patterned for a second region; and implanting a second n-type dopant into the substrate through openings in the first photoresist layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIGS. 1A-H depict various stages in the process of forming n-type buried regions in an integrated circuit chip according to an embodiment.

[0005] FIG. 2 depicts a graphic comparison of the simulated concentration of phosphorus in the deep n-type buried layer using the conventional process and using an example embodiment.

[0006] FIG. 3A depicts a flowchart of a method of fabricating an integrated circuit.

[0007] FIG. 3B depicts a flowchart of a method of forming two n-type buried regions in an integrated circuit chip.

[0008] FIG. 3C depicts a flowchart of a method of forming two n-type regions in an integrated circuit chip according to an embodiment.

[0009] FIGS. 4A-D depict various stages in the process of forming two buried layers in a semiconductor substrate according to the prior art.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0010] In the drawings, like references indicate similar elements. In this description, different references to "an" or "one" embodiment are not necessarily to the same embodiment, and such references may mean at least one. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, such feature, structure or characteristic may be effected in connection with other embodiments, irrespective of whether explicitly described.

[0011] Example embodiments include a method of producing dual buried layers in a semiconductor chip that eliminates a number of steps from a prior process to accomplish the same result. The described embodiments decrease the time necessary to produce the end product and consequently lowers the cost of production.

[0012] FIGS. 4A-D show a conventional process of forming dual n-type buried layers in a semiconductor substrate. In the process shown, an n-type buried layer (NBL) region 405 is formed on the right side of the figure, a deep n-type buried layer (DNBL) region 401 is formed on the left side and a region with overlapping sections of both implants 403 is shown in the middle of the figure. Not all of these regions are necessarily included in a single layout; instead, these are all shown for the purpose of illustration. The process begins with a semiconductor substrate 402, which in one embodiment is a silicon wafer. At the point shown as 400A, a first oxidation layer 404, i.e., silicon dioxide, has been grown on the top surface of substrate 402. Usually, this oxidation layer is 7500Å thick in order that the oxidation layer can act as a hardmask for the implantation process. Oxidation layer 404 has been patterned using a photoresist (not specifically shown), which has then been removed. A thin pad oxide layer 406, e.g. 200Å thick, is grown to protect the surface of the substrate during the implantation process. In the example process, phosphorus (P) is implanted into substrate 402 at a dosage of $1.5x10^{13}/cm^2$ and an energy level of 150KV. This process is then followed by a DNBL drive to form DNBL 408. The DNBL drive is generally performed at 1200°C for 30 minutes.

[0013] After the DNBL drive is completed, oxidation layer 404 is stripped off and a second oxidation layer 410, also 7500Å thick, is grown on substrate 402. This stage of the process is shown as 400B. At the stage shown at stage 400C, oxidation layer 410 has been patterned using a photoresist layer (not specifically shown), which is then removed. A second implantation is performed through the patterned opening in oxidation layer 410 to form NBL implant 412. In at least one embodiment, the second implantation process implants antimony at a dosage of

$2x10^{15}/cm^2$ at an energy of 60KV.

[0014] After the implantation is completed, a diffusion-under-field (DUF) drive is performed to drive the two implants further into the substrate, creating the regions shown as 400D. As the DUF drive is performed, pad oxide 414 grows on the exposed silicon overlying NBL implant 412. This completes the prior process of forming the dual buried layers. The process illustrated in FIGS. 4A-D works well. However, by modifying the process, the same doping profiles can be reproduced using several days' less time and thus saving on the costs of manufacturing chips which use the described process.

[0015] The modified process is described herein with reference to FIGS. 1A-F. This process is described in terms of DNBL 101, NBL 105 and overlapping NBL+DNBL region 103, as were shown in the prior art, but the described process can be used with implanting two n-type dopants for other types of regions. At stage 100A, oxidation layer 104 has been grown on the surface of substrate 102. In at least one embodiment, oxidation layer 104 again has a thickness of 7500Å. At stage 100B, photoresist 106 has been deposited over oxidation layer 104 and a pattern that was created in photoresist 106 has been etched into oxidation layer 104 to expose the substrate in areas where an n-type buried layer is desired. In at least one embodiment, photoresist 106 is 1 micron thick.

[0016] As shown at 100C, photoresist 106 is removed before implanting antimony in a blanket implant process to create NBL 108. In one embodiment, the implantation process to create NBL 108 is performed at 60KV and implants antimony at a dosage of $2x10^{15}/cm^2$. The DUF drive that previously followed the implantation of NBL 108 is not performed at this point, although it will be performed at a later time. As shown at stage 100D, a new oxidation layer is not created between the two implantation processes; rather photoresist layer 110 simply covers both oxidation layer 104 and exposed regions of substrate 102. Because photoresist 110 is a conformal layer, the topography of the photoresist 110 is not entirely smooth.

[0017] In the described process, the DNBL implantation takes place through oxide layer 104 and thus requires higher energy to perform. In one embodiment, the thickness of photoresist 110 is increased to 1.5 microns. As shown at 100E, photoresist 110 has been patterned, although the underlying oxidation layer 104 has not been disturbed. The substrate is already exposed in the region where the DNBL and NBL overlap. A close examination reveals that the opening through which DNBL 112 will be formed is somewhat larger than the opening used in the

conventional process; this adjustment compensates for the fact that no DNBL drive is performed in the described process. One advantage of the described process is that whenever a thermal process is performed on the substrate, e.g., the conventional re-growing of 7500Å of oxide, outgassing of the dopant can occur through exposed regions and may contaminate other regions. In example embodiments, no thick growth of oxide is performed after the implant, so little or no outgassing or cross contamination by the phosphorus occurs.

[0018] In one embodiment, the blanket implantation of phosphorus is a chain implant, with one segment implanting $1.0x10^{13}/cm^2$ at 90Kev and a second segment implanting $1.5x10^{13}/cm^2$ at 1.3MeV. The first, low energy implant will be blocked by the thick oxide layer over the DNBL region 101, but will penetrate in the overlapping region 103. The second, high energy implant will penetrate the thick oxide overlying region 101 and will penetrate deeply into the substrate in region 103. In the steps illustrated in 100F, photoresist 110 was ashed and substrate 102 was subjected to the DUF drive that was not previously performed. The DUF drive will enlarge both NBL 108 and DNBL 112 by driving each further into the substrate. During this process, a thin layer of silicon dioxide 114 is also formed.

[0019] This completes the process of implanting two n-type dopants into a substrate, although this process is part of a larger process that includes forming two n-type buried layers and forming the rest of the circuit, e.g., active devices. As shown at 100G, the oxidation layers and any other dielectric remaining on the surface of substrate 102 has been removed and an epitaxial layer 116 has been grown. As the epitaxial layer is grown, the buried implants are driven into epitaxial layer 116 to form an n-type buried layer 108 and a deep n-type buried layer 112. Depending on the specific circuit in which the described dual n-type layers is being used, further processing can take many forms.

[0020] FIG. 1H illustrates an example of an integrated circuit 100H that uses the described dual n-type buried layers. This example is a cross section of a portion of a power NMOS device and depicts active devices that have been formed in the epitaxial layer. Integrated circuit 100H includes deep n-type buried layer (DNBL) 112 and n-type buried layer (NBL) 108, which have been implanted into substrate 102 and driven into epitaxial layer 116 as this layer was grown. The circuit also includes a deep p-type buried layer (DNBL) 120 and both n-type wells 122 and p-type well 124, and high-voltage p-well implant (HVPW) 126 and n-channel voltage adjust implant (VTN) 128. N-type contact areas 134 and P-type contact areas 136 are also shown.

Accordingly, other specific active devices can also be formed over the described buried layers. Oxide layer 130 and an inter-level dielectric 132 complete this circuit.

[0021] The process is described herein for two buried layers grown in the substrate of a silicon wafer. However, other semiconductor materials, such as germanium and selenium, can also be used in conjunction with the described method. Further, this method can also be used after an epitaxial layer has been formed. Therefore, for the purposes of this application, reference to actions performed on a substrate can also be interpreted to include actions performed on an epitaxial layer. Additionally, when the described implantations are performed after the epitaxial layer is formed, regions other than buried layers can be created using the described process.

[0022] It is possible to use the described process, while reversing the order of the implantations, so the process can implant dopants for the DNBL through openings in a photoresist layer before implanting dopants for the NBL through openings in the dielectric layer. However, it is important that patterns are aligned to each other, so that the relationship between different regions is maintained. Because the dielectric layer is not itself patterned when implanting the DNBL region, performing the DNBL implant first would require additional actions to form alignment marks that can be used when patterning the NBL layer. By implanting NBL first, alignment marks can be formed in the dielectric layer when the pattern etch for the NBL layer is performed, such that no additional actions are needed.

[0023] Table 1 below shows a comparison of the actions performed in the conventional method and those performed in the described procedures.

Table 1

PRIOR ART	*DESCRIBED PROCESS*
1ST OXIDATION	1ST OXIDATION (7500A)
DNBL PATTERN	Moved
DNBL ETCH	Removed
DNBL ETCH CLEAN	Removed
DNBL PAD OX	Removed
DNBL IMPLANT	Moved
DNBL DRIVE	Removed
2ND OXIDATION	Removed
N+ BL PATTERN (Aligned to	N+ BL PATTERN

DNBL)	
N+ BL ETCH	N+ BL ETCH
N+ BL CLEAN	N+ BL CLEAN
NBL IMPLANT	NBL IMPLANT
	DNBL PATTERN (Aligned to NBL; Upsized opening compensates for no DNBL Drive)
	DNBL IMPLANT (Chain implant; at least one segment is a high energy implant >1MeV to penetrate 7500A Oxide)
DUF DRIVE	DUF DRIVE

[0024] As shown in the comparison of this table, the changes made by the described process eliminate the need for a number of actions, such as etching the oxide before implanting the DNBL and cleaning up after the etch is completed. There is also no need to grow a pad oxide, as a much thicker oxide already exists on top of the substrate where the DNBL is to be implanted. Additionally, the DNBL drive is removed from the process. Finally, because the first oxidation layer is not removed in the second process, there is no need to grow a second oxidation layer in preparation for the DNBL implantation. In one embodiment, the time saved in removing all of these actions amounts to approximately three days, which over the lifetime of the process can potentially save millions of dollars.

[0025] Although the process is described herein using phosphorus for the DNBL and antimony for the NBL, other n-type dopants can be used. The most commonly used n-type dopants are phosphorus, arsenic and antimony, which have atomic mass units (AMU) of 31, 75 and 121 respectively. Any of these dopants or other less commonly used n-type dopants can be used for the NBL layer, which is implanted directly into the substrate. Implanting dopants through the dielectric layer requires using high implant energy, with higher AMU species requiring higher implant energies to penetrate through the dielectric. Arsenic can be implanted in the example DNBL through the dielectric; in one embodiment using arsenic, the oxidation layer is reduced to below 5000Å. Antimony would not generally be used to implant through the oxidation layer due to its large AMU. All of these variations fall within the scope of this description.

[0026] FIG. 2 illustrates a comparison between the simulated concentration of phosphorus for both the conventional process and for an example embodiment. The dotted lines show the prior art after the second oxidation process and also show an example embodiment as implanted, while

the solid lines show both the prior art and an example embodiment after respective NBL drives. The distribution of the phosphorus as implanted in the new process (labeled NBL First) is concentrated at depths between 0.5μm and 2.5μm, with a peak at 1.7μm, while the conventional process is heaviest near the surface of the chip and gradually lessens to around 5.25μm. However, the NBL drive causes the phosphorus to be redistributed through the substrate so that the two profiles after the NBL drive is quite similar.

[0027] FIGS. 3A-C each disclose a method that includes implanting two n-type dopants into an IC chip as described herein, each including different levels of additional processing on the chip. FIG. 3A depicts a method 300A of fabricating an integrated circuit. As expressed in flowchart 300A, the method begins with forming (305) a patterned dielectric layer over a substrate, where the patterned dielectric layer includes a first pattern of openings. In one embodiment, the substrate is a silicon wafer and the dielectric layer is silicon dioxide. This can include forming the dielectric layer, patterning the dielectric and performing any clean-up necessary to present a clean, prepared surface for implantation. The method continues with implanting (310) a first n-type dopant into the substrate through the patterned dielectric layer to form a first doped region. Next a patterned photoresist layer is formed (315) overlying the patterned dielectric layer, where the patterned photoresist layer includes a second pattern of openings, followed by implanting (320) a second n-type dopant into the substrate through the patterned photoresist layer to form a second doped region. The method removes (325) the patterned photoresist layer and the patterned dielectric layer, then grows (330) an epitaxial layer on the substrate and drives the first doped region and the second doped region into the epitaxial layer to form respective first and second n-type buried layers. Finally, the method forms (335) active devices in the epitaxial layer.

[0028] FIG. 3B depicts a method 300B of forming two n-type buried regions in an integrated circuit chip. This method implants (350) a first n-type dopant into a substrate through openings in a dielectric layer that is patterned with a first pattern of openings and forms (355) a first photoresist layer overlying the dielectric layer, where the first photoresist layer is patterned with a second pattern of openings. The method continues to implant (360) a second n-type dopant into the substrate through the second pattern of openings, then removes (365) the first photoresist layer and the dielectric layer, and finishes by growing (370) an epitaxial layer on the substrate and driving the first implanted n-type dopant and the second implanted n-type dopant into the

epitaxial layer to form respective first and second n-type buried layers.

[0029] FIG. 3C depicts a third method (300C) of forming two n-type regions in an integrated circuit chip. This method implants (385) a first n-type dopant into the IC chip through openings in a dielectric layer that is patterned with a first pattern of openings, forms (390) a photoresist layer overlying the dielectric layer, where the photoresist layer is patterned with a second pattern of openings and implants (395) a second n-type dopant into the IC chip through openings in the photoresist layer.

[0030] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit, the method comprising:

forming a patterned dielectric layer over a substrate, the patterned dielectric layer comprising a first pattern of openings;

implanting a first n-type dopant into the substrate through the patterned dielectric layer to form a first doped region;

forming a patterned photoresist layer overlying the patterned dielectric layer, the patterned photoresist layer comprising a second pattern of openings;

implanting a second n-type dopant into the substrate through the patterned photoresist layer and the patterned dielectric layer to form a second doped region;

removing the patterned photoresist layer and the patterned dielectric layer;

growing an epitaxial layer on the substrate and driving the first doped region and the second doped region into the epitaxial layer to form respective first and second n-type buried layers; and

forming active devices in the epitaxial layer.

2. The method of claim 1, further comprising performing a thermal drive operation only after implanting both the first n-type dopant and the second n-type dopant.

3. The method of claim 2, wherein implanting the second n-type dopant comprises using a MeV ion implanter to form the second doped region.

4. The method of claim 2, wherein the patterned dielectric layer comprises approximately 7500Å of silicon dioxide.

5. The method of claim 2, wherein the patterned dielectric layer is approximately 5000Å of silicon dioxide.

6. The method of claim 2, wherein the first n-type dopant comprises antimony and the second n-type dopant comprises phosphorus.

7. The method of claim 2, wherein at least a portion of the first pattern of openings and the second pattern of openings overlap.

8. The method of claim 2, wherein no portion of the first pattern of openings and the second pattern of openings overlap.

9. A method of forming two n-type buried regions in an integrated circuit chip (IC), the method comprising:

implanting a first n-type dopant into a substrate through openings in a dielectric layer that is patterned with a first pattern of openings;

forming a first photoresist layer overlying the dielectric layer, the first photoresist layer being patterned with a second pattern of openings;

implanting a second n-type dopant into the substrate through the second pattern of openings;

removing the first photoresist layer and the dielectric layer;

growing an epitaxial layer on the substrate and driving the first implanted n-type dopant and the second implanted n-type dopant into the epitaxial layer to form respective first and second n-type buried layers.

10. The method of claim 9, wherein implanting the second n-type dopant comprises using a MeV ion implanter.

11. The method of claim 10, further comprising performing a thermal drive operation only after implanting both the first n-type dopant and the second n-type dopant.

12. The method of claim 11, further comprising:

depositing the dielectric layer;

patterning the dielectric layer using a second photoresist layer and the first pattern of openings; and

removing the second photoresist layer.

13. The method of claim 12, wherein the patterned dielectric layer comprises approximately 7500Å of silicon dioxide.

14. The method of claim 12, wherein the patterned dielectric layer is approximately 5000Å of silicon dioxide.

15. The method of claim 8, wherein the first n-type dopant comprises antimony and the second n-type dopant comprises arsenic.

16. The method of claim 11, wherein at least a portion of the first pattern of openings and the second pattern of openings overlap.

17. The method of claim 11, wherein no portion of the first pattern of openings and the second pattern of openings overlap.

18. A method of forming two n-type regions in an integrated circuit (IC) chip, the method comprising:

implanting a first n-type dopant into the IC chip through openings in a dielectric layer that is patterned with a first pattern of openings;

forming a photoresist layer overlying the dielectric layer, the photoresist layer being patterned with a second pattern of openings; and

implanting a second n-type dopant into the IC chip through openings in the photoresist layer.

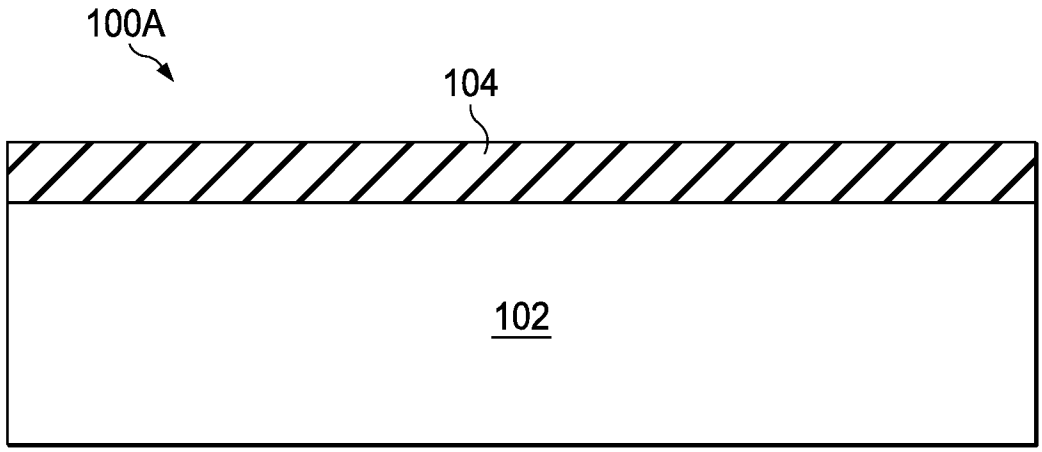


FIG. 1A

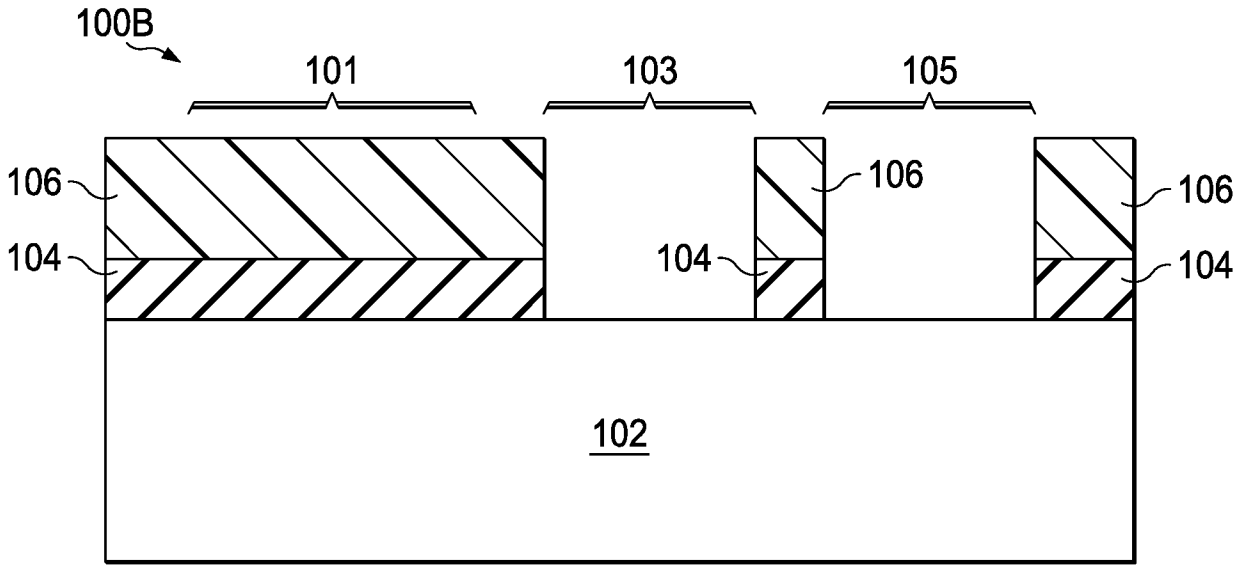


FIG. 1B

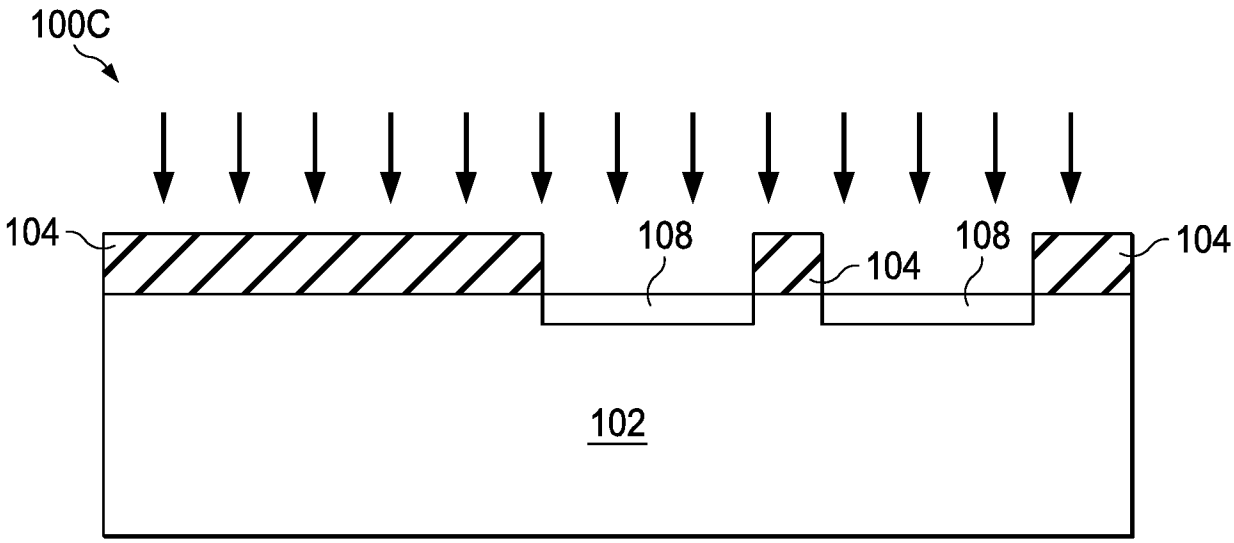


FIG. 1C

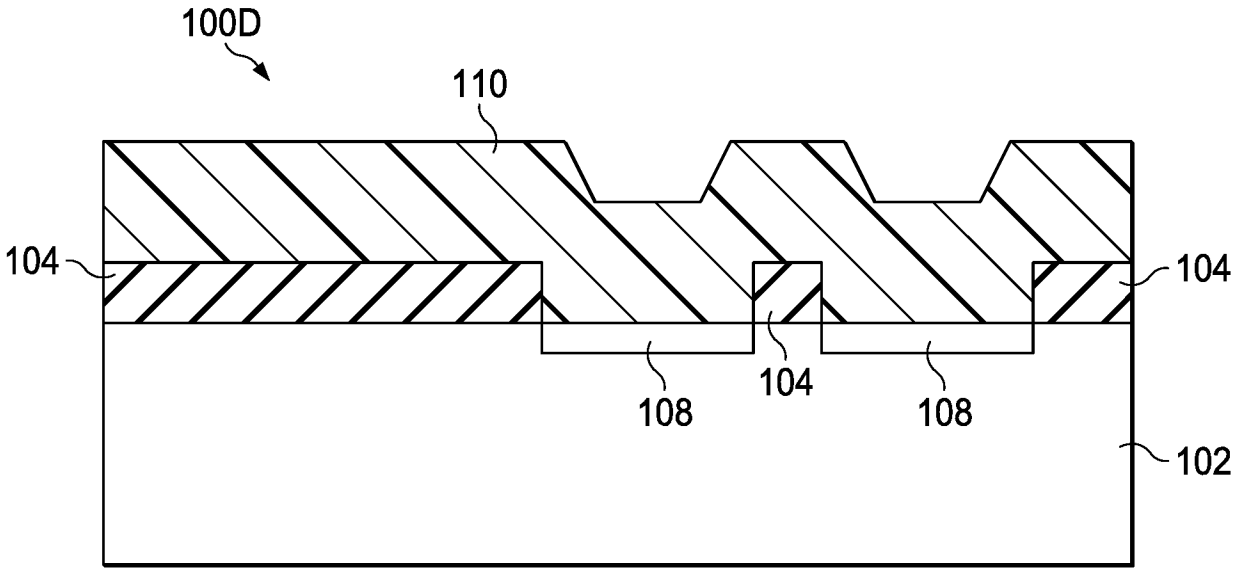
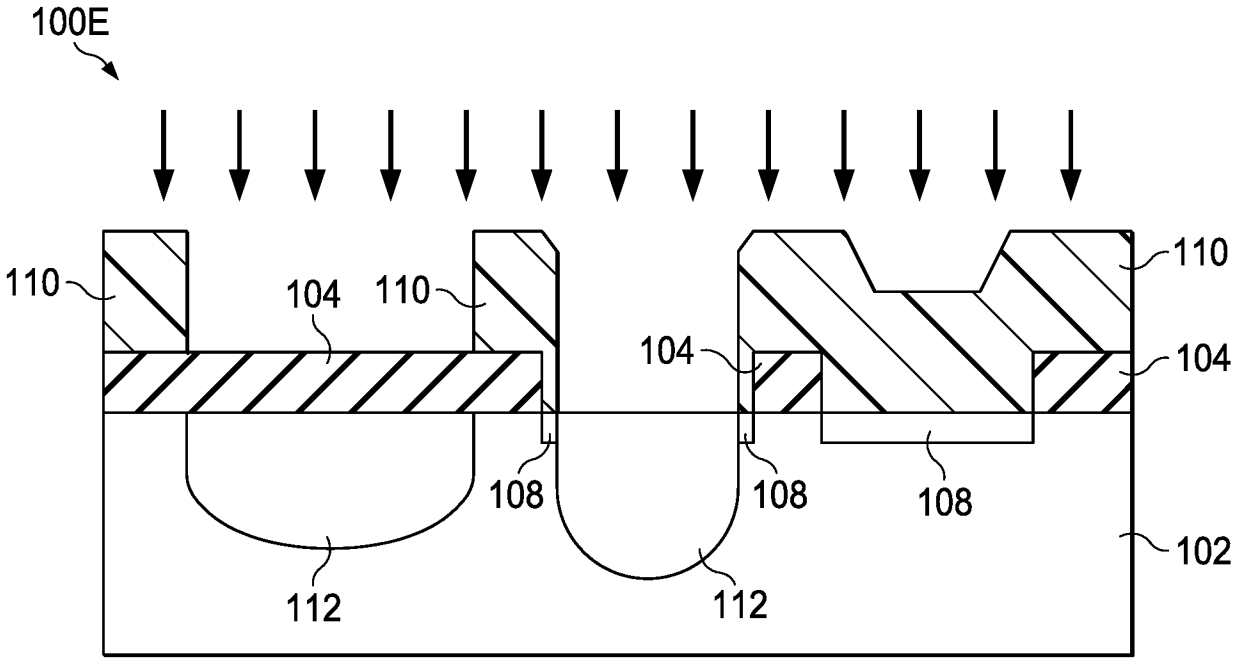


FIG. 1D


100E
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112
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FIG. 1E

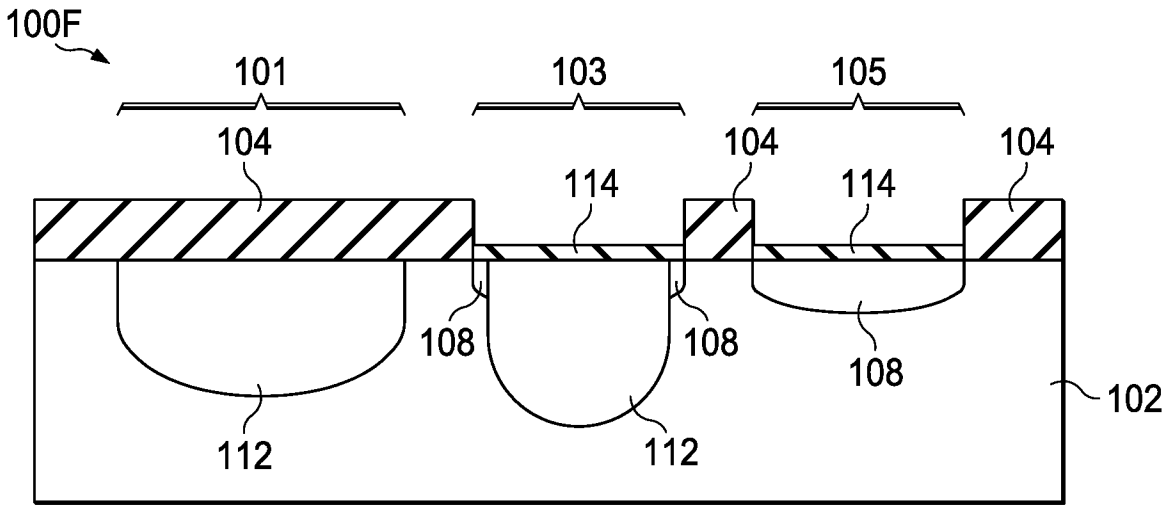
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FIG. 1F

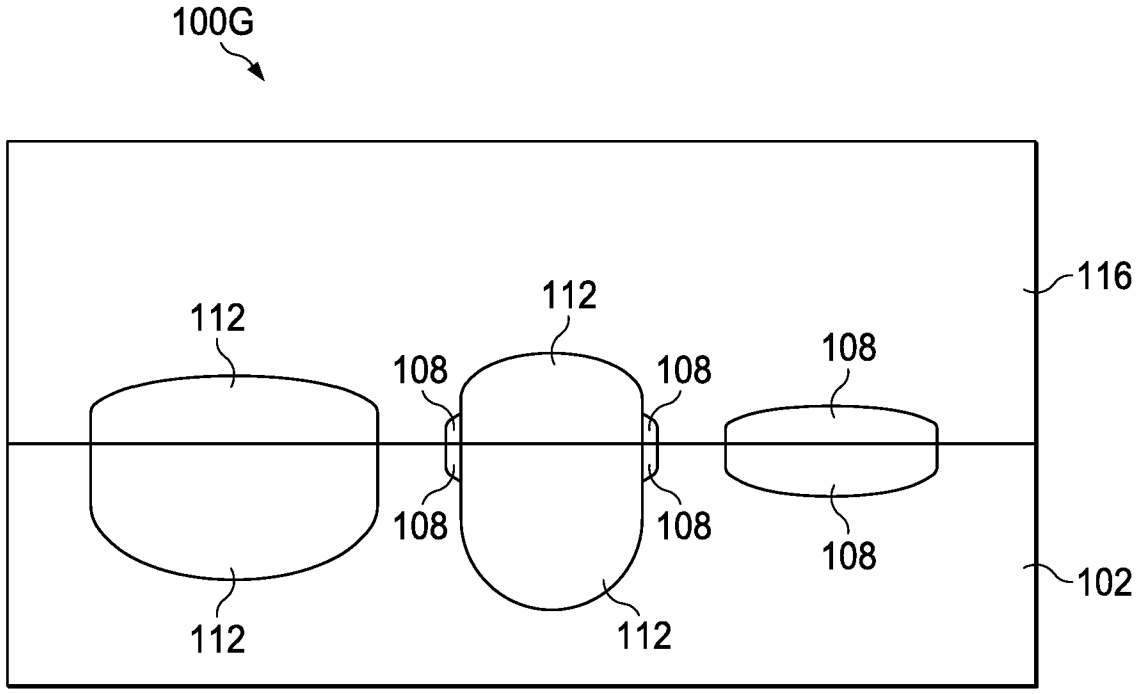
100G
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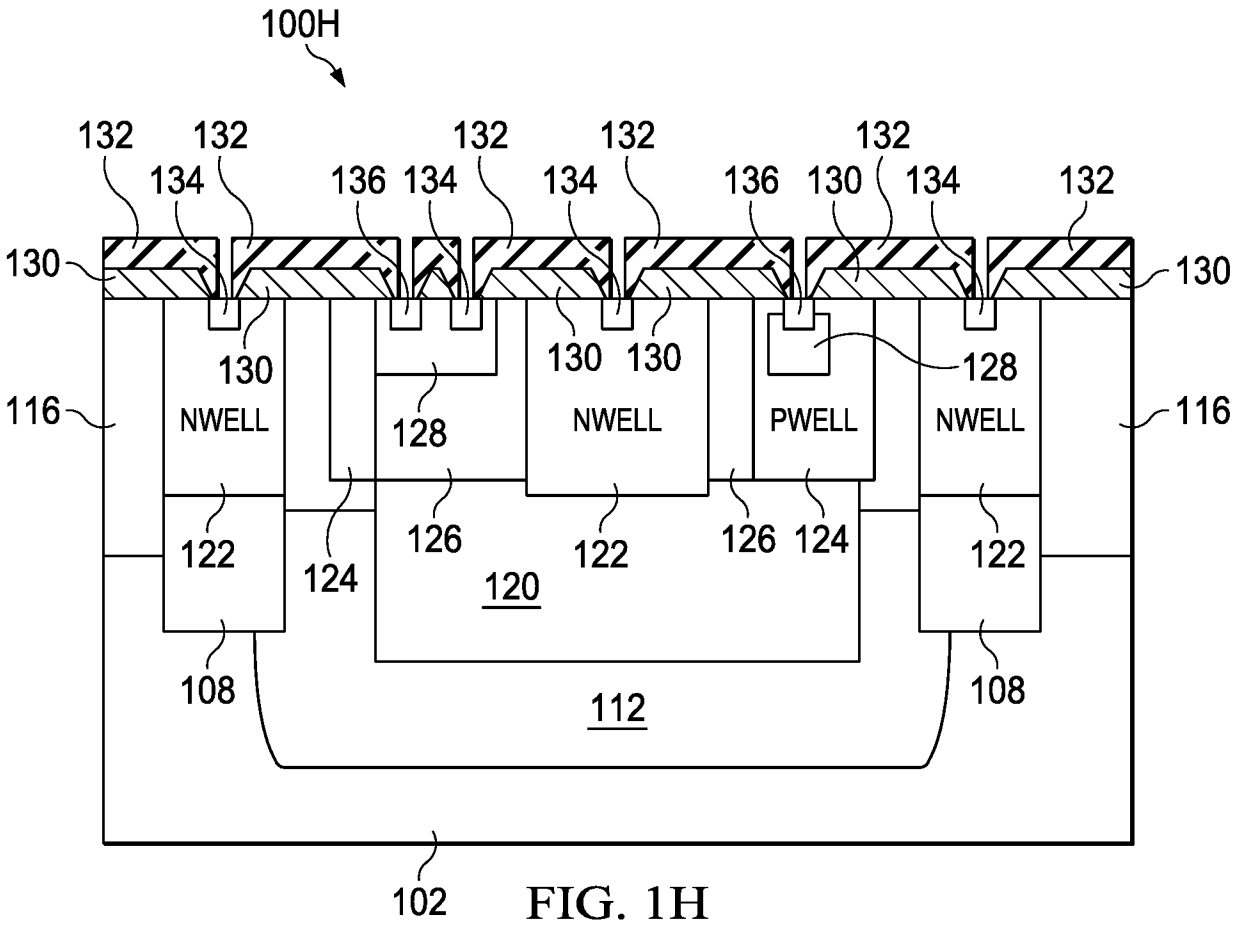
FIG. 1G


100H
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NWELL
128
NWELL
PWELL
NWELL
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126
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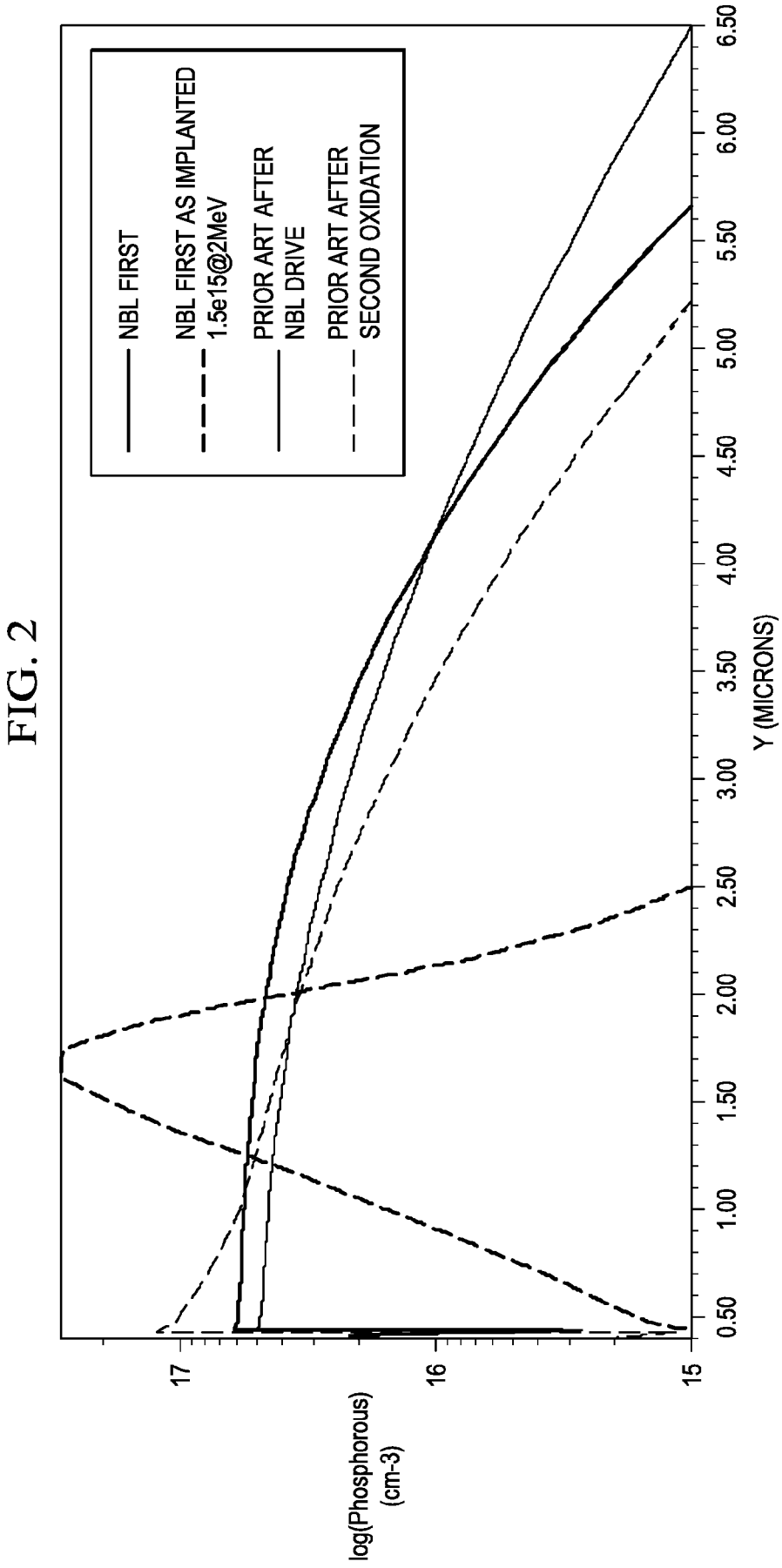
108
112
108
102

FIG. 1H

FIG. 2


NBL FIRST
NBL FIRST AS IMPLANTED 1.5e15@2MeV
PRIOR ART AFTER NBL DRIVE
PRIOR ART AFTER SECOND OXIDATION
log(Phosphorous) (cm-3)
17
16
15
Y (MICRONS)
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
5.50
6.00
6.50

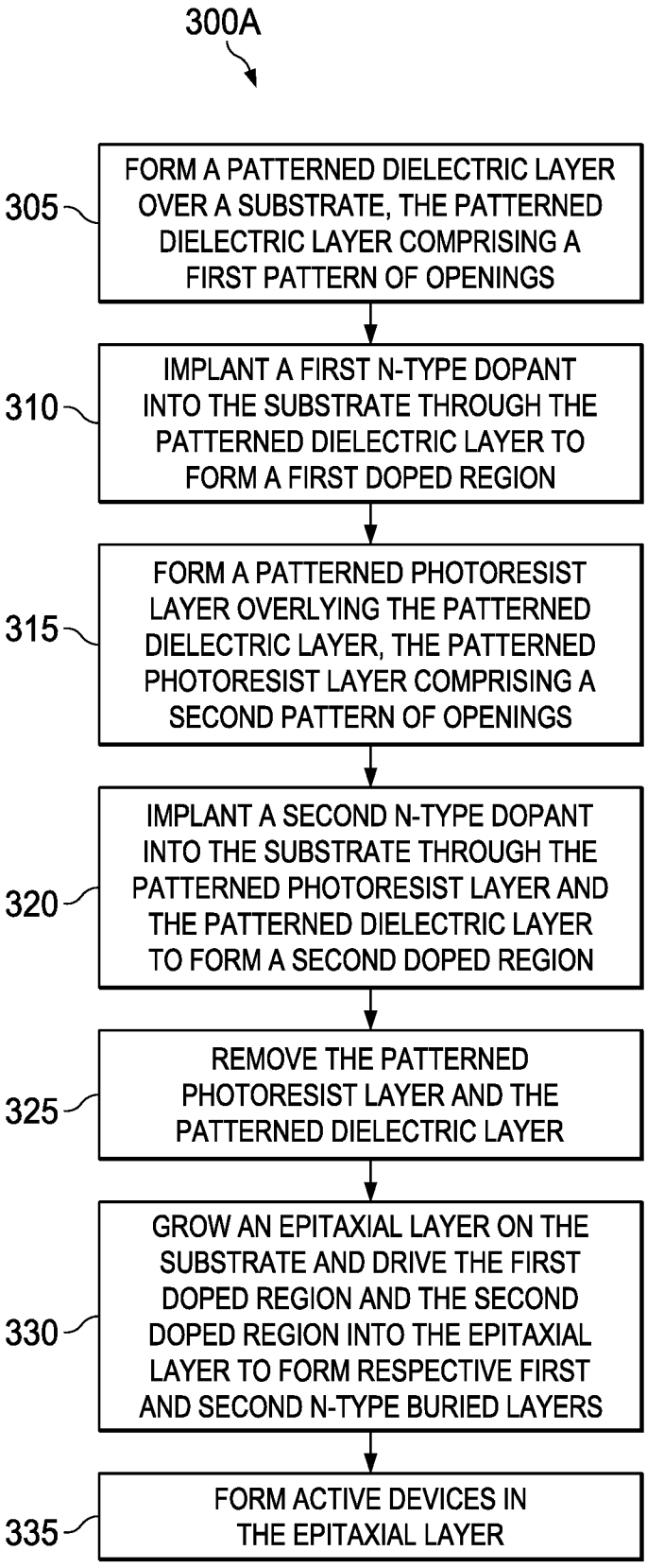

300A
305
FORM A PATTERNED DIELECTRIC LAYER OVER A SUBSTRATE, THE PATTERNED DIELECTRIC LAYER COMPRISING A FIRST PATTERN OF OPENINGS
310
IMPLANT A FIRST N-TYPE DOPANT INTO THE SUBSTRATE THROUGH THE PATTERNED DIELECTRIC LAYER TO FORM A FIRST DOPED REGION
315
FORM A PATTERNED PHOTORESIST LAYER OVERLYING THE PATTERNED DIELECTRIC LAYER, THE PATTERNED PHOTORESIST LAYER COMPRISING A SECOND PATTERN OF OPENINGS
320
IMPLANT A SECOND N-TYPE DOPANT INTO THE SUBSTRATE THROUGH THE PATTERNED PHOTORESIST LAYER AND THE PATTERNED DIELECTRIC LAYER TO FORM A SECOND DOPED REGION
325
REMOVE THE PATTERNED PHOTORESIST LAYER AND THE PATTERNED DIELECTRIC LAYER
330
GROW AN EPITAXIAL LAYER ON THE SUBSTRATE AND DRIVE THE FIRST DOPED REGION AND THE SECOND DOPED REGION INTO THE EPITAXIAL LAYER TO FORM RESPECTIVE FIRST AND SECOND N-TYPE BURIED LAYERS
335
FORM ACTIVE DEVICES IN THE EPITAXIAL LAYER

FIG. 3A

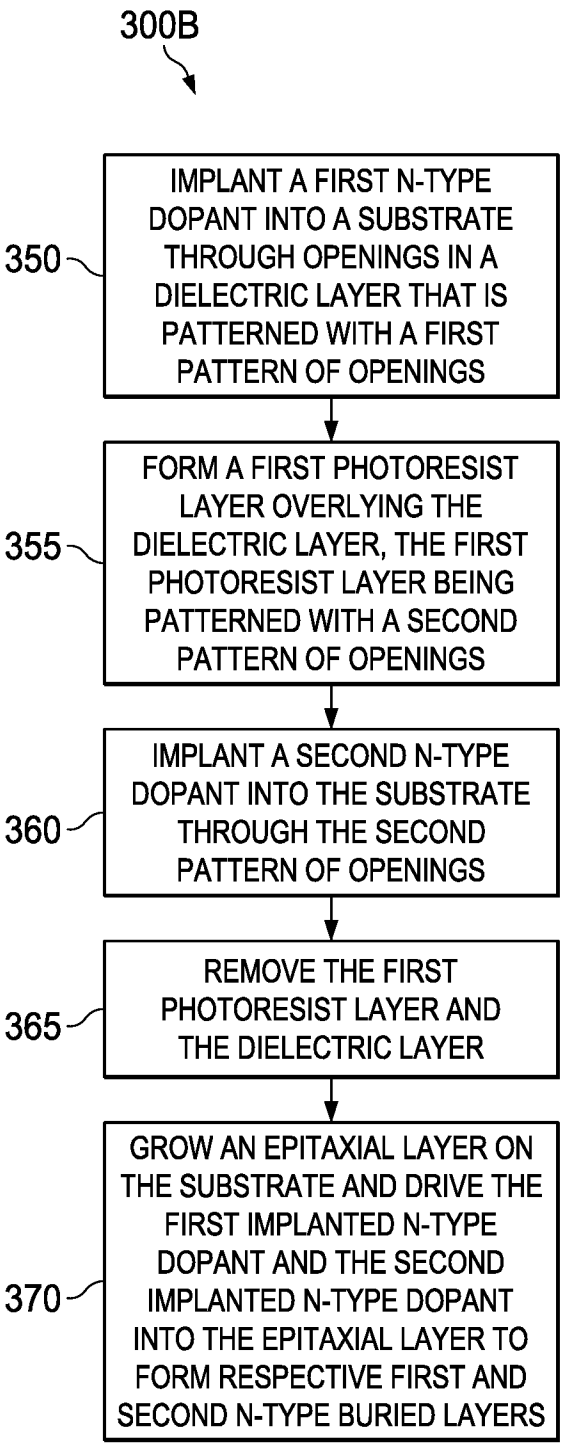

300B
IMPLANT A FIRST N-TYPE DOPANT INTO A SUBSTRATE THROUGH OPENINGS IN A DIELECTRIC LAYER THAT IS PATTERNED WITH A FIRST PATTERN OF OPENINGS
350
FORM A FIRST PHOTORESIST LAYER OVERLYING THE DIELECTRIC LAYER, THE FIRST PHOTORESIST LAYER BEING PATTERNED WITH A SECOND PATTERN OF OPENINGS
355
IMPLANT A SECOND N-TYPE DOPANT INTO THE SUBSTRATE THROUGH THE SECOND PATTERN OF OPENINGS
360
REMOVE THE FIRST PHOTORESIST LAYER AND THE DIELECTRIC LAYER
365
GROW AN EPITAXIAL LAYER ON THE SUBSTRATE AND DRIVE THE FIRST IMPLANTED N-TYPE DOPANT AND THE SECOND IMPLANTED N-TYPE DOPANT INTO THE EPITAXIAL LAYER TO FORM RESPECTIVE FIRST AND SECOND N-TYPE BURIED LAYERS
370

FIG. 3B

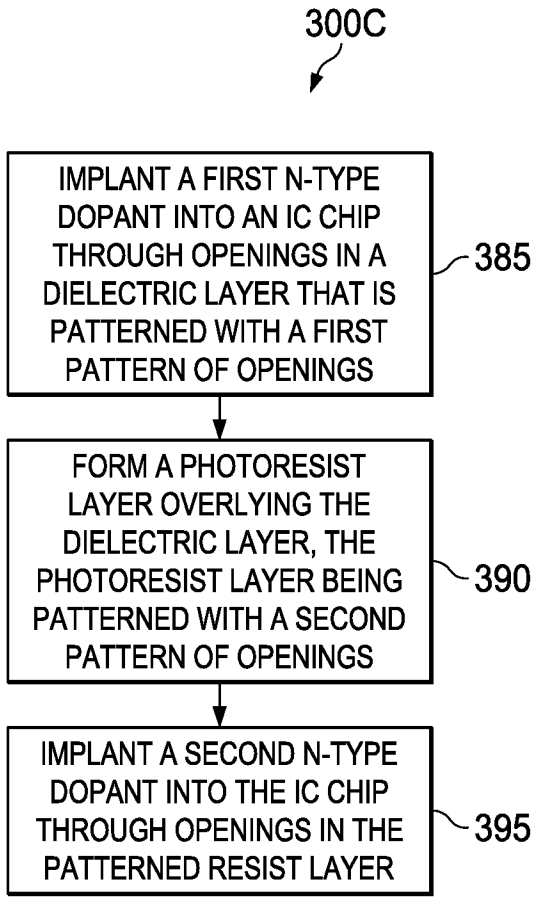

300C
IMPLANT A FIRST N-TYPE DOPANT INTO AN IC CHIP THROUGH OPENINGS IN A DIELECTRIC LAYER THAT IS PATTERNED WITH A FIRST PATTERN OF OPENINGS
385
FORM A PHOTORESIST LAYER OVERLYING THE DIELECTRIC LAYER, THE PHOTORESIST LAYER BEING PATTERNED WITH A SECOND PATTERN OF OPENINGS
390
IMPLANT A SECOND N-TYPE DOPANT INTO THE IC CHIP THROUGH OPENINGS IN THE PATTERNED RESIST LAYER
395

FIG. 3C

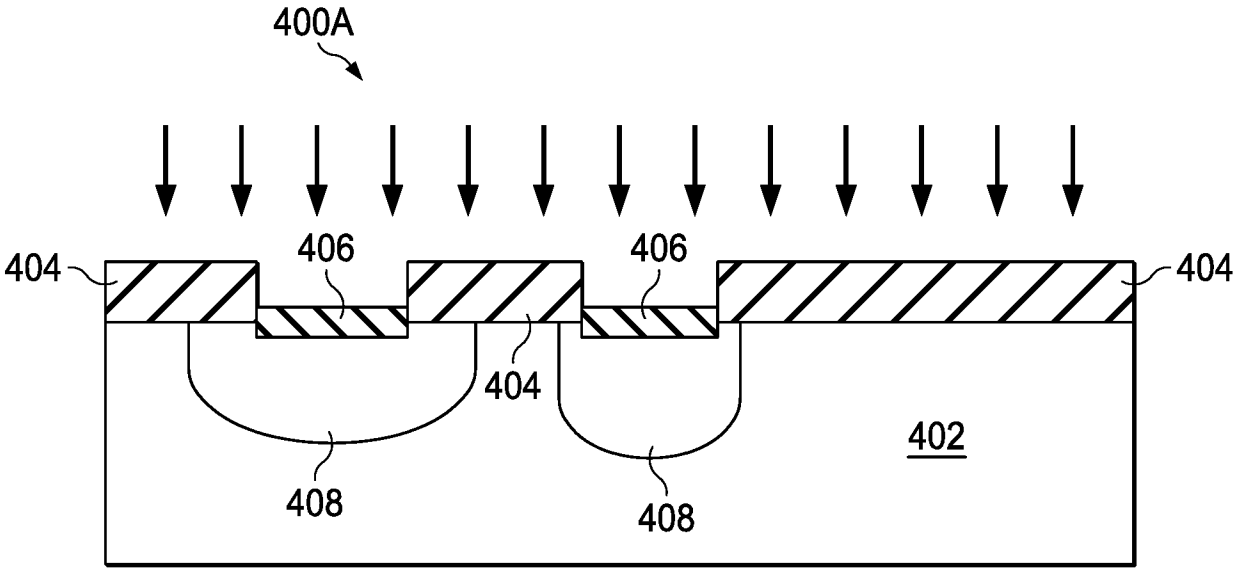


FIG. 4A
(PRIOR ART)

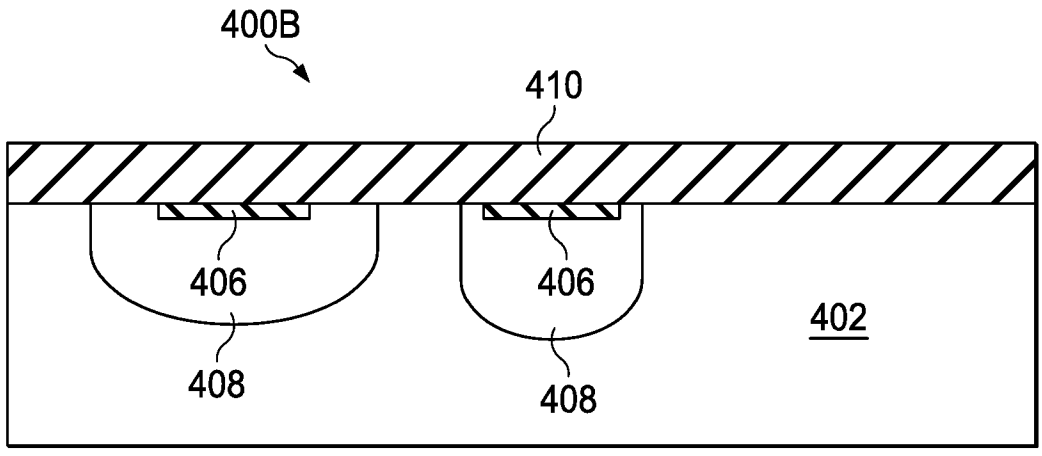


FIG. 4B
(PRIOR ART)

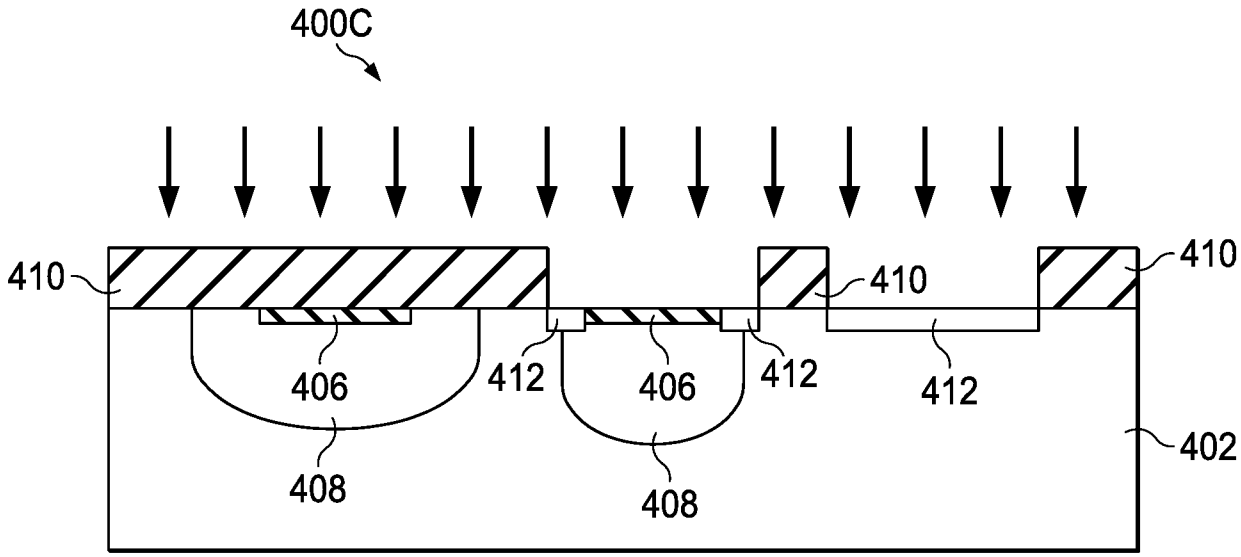


FIG. 4C
(PRIOR ART)

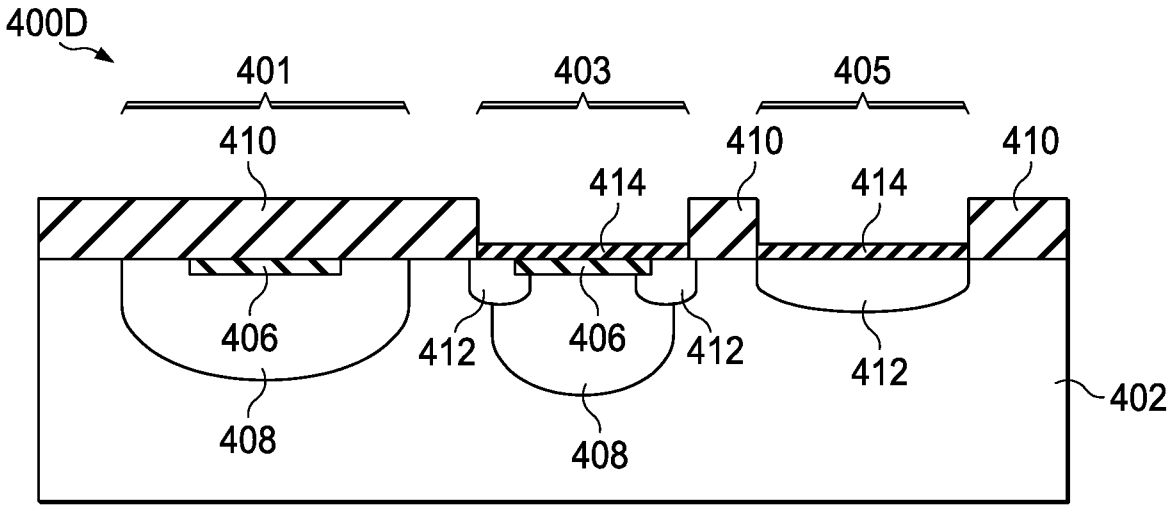


FIG. 4D
(PRIOR ART)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2017/050981

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/82 *(2006.01)*
H01L 21/265 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/82, 21/22, 21/265

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/0278200 A1 (SANYO ELECTRIC CO., LTD) 12.11.2009, fig.1-4, [0020]-[0034]	1-18
X	US 2004/0248389 A1 (AKIO IWABUCHI) 09.12.2004, fig.3-8, [0042]-[0058]	1-3, 6-12, 15-18
X	US 5331198 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 19.07.1994, fig.1-3, col.4-5	1-3, 6-12, 15-18
A	US 9105712 B1 (TOWER SEMICONDUCTOR LTD.) 11.08.2015	1-18
A	US 5336920 A (SGS-THOMSON MICROELECTRONICS S.A.) 09.08.1994	1-18

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 December 2017 (13.12.2017)	28 December 2017 (28.12.2017)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2017/050981

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0851487 A1 (SANKEN ELECTRIC CO., LTD.) 01.07.1998	1-18