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LINE GENERATING MEANS AND METHOD

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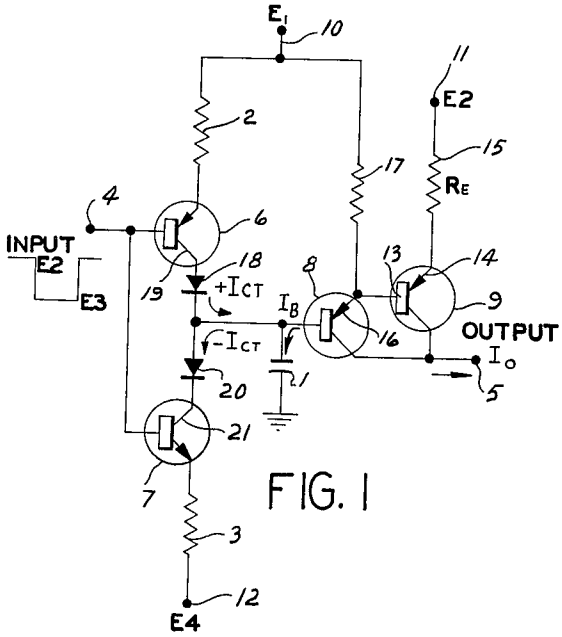


FIG. 1

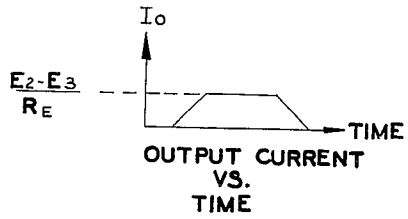


FIG. 2

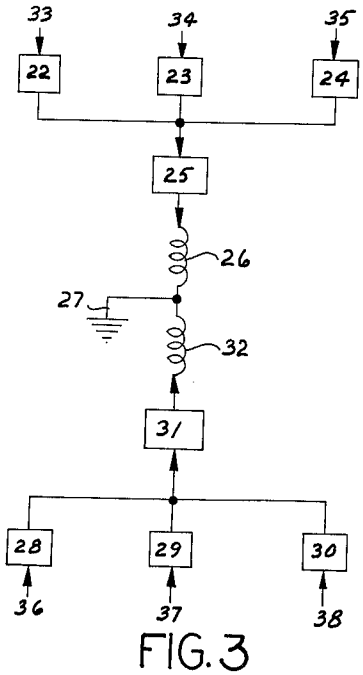


FIG. 3

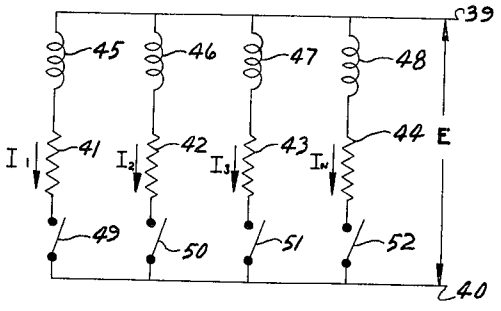


FIG. 4

INVENTOR.
DANIEL J. GRIFFIN

BY

R. E. Beaugne

ATTORNEY

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LINE GENERATING MEANS AND METHOD

Daniel J. Griffin, La Puente, Calif., assignor to The Marquardt Corporation, Van Nuys, Calif., a corporation of California

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This invention relates to a novel method of generating straight line traces between any two selected points on the screen of a cathode ray tube, and to novel and improved apparatus suitable for implementing the method of the invention.

There have been proposed heretofore a number of ramp generators which are suitable for generating deflection voltages or deflection currents for tracing line segments on a cathode ray tube screen. Generally, these prior devices have been variations of the well-known saw-tooth generator.

Saw-tooth waveforms are suitable for horizontal or vertical sweeps, and are frequently used in cathode ray tube devices. Also, it has been proposed heretofore to combine suitably phased pairs of sinusoidal waveforms of equal amplitudes to result in Lissajous figure having the form of a straight line deflection on the cathode ray tube screen. However, these methods are not particularly suitable for selectively generating straight line traces between any two points on the cathode ray tube screen, such as along non-orthogonal axes.

To overcome these shortcomings of the prior art, the the present invention is directed to readily adjustable means for providing arbitrarily oriented straight line traces.

The method of the present invention resides in the generation of a linear deflection signal for the horizontal axis which has a time duration equal to the time duration of a linearly generated vertical axis signal, the voltage or current amplitude of the two signals being independently variable. That is, the duration of the horizontal signal is made to equal the duration of the vertical signal or conversely without regard to the amplitude of either signal. Since the two signals are of the same duration, they may be applied concurrently to their respective deflection systems of the cathode ray tube to provide a line trace passing through selected loci.

Various circuit means have been contemplated to accomplish this function, each of which must provide means for selecting the slope of the deflection signal (viz., the starting and final amplitude) and independent means for selecting the time interval required for the deflection signal to change from the starting value to the final value, so that it will equal the time interval of a similar circuit for the alternate axis of the deflection system. The deflection signals may be provided by either a voltage ramp generator or a current ramp generator, provided only that the specified range of selectable amplitudes may be varied while maintaining a fixed duration of the ramp time base.

While various circuit means may be employed to result in the deflection signals necessary to accomplish the novel method of the invention, certain preferred circuits are contemplated. Two embodiments of apparatus suitable for implementing the novel method of the invention will be shown and described hereinafter. One embodiment employs a ramp deflection generator circuit having series L and R elements in which the inductive element tends to linearize the current flow through the purely resistive element. The alternate embodiment employs R and C elements in which the capacitive element comprises a timing capacitor which controls the time duration of the ramp.

It is therefore a principal object of the invention to provide an improved method of generating linear signals which may be applied to the deflection system of a cathode ray tube for tracing a straight line between any two selected points on the screen of the tube.

Another object of the invention is to provide novel apparatus for providing ramp signals in which the ramp slope and the ramp time base may be independently varied.

Still another object of the invention is to provide a novel ramp generator circuit capable of providing linear ramp current signals of selectably variable slope and duration.

Still another object of the invention is to provide a novel ramp generator circuit capable of providing linear voltage signals in which the ramp slope and the ramp duration may be linearly varied over a selectable range.

These and other objects of the invention will be better understood with reference to the accompanying description and the following drawings in which:

FIGURE 1 is a schematic diagram of a first embodiment of a ramp generator circuit suitable for implementing the method of the invention.

FIGURE 2 graphically illustrates the output current from the circuit of FIGURE 1, as a function of time, in response to specified operating conditions.

FIGURE 3 diagrammatically illustrates the method of utilizing the apparatus of FIGURE 1 in the deflection system of a cathode ray tube.

FIGURE 4 is a simplified schematic diagram illustrating the circuit operating principles of an alternate embodiment of a ramp generator apparatus suitable for use in the invention.

There is shown in FIGURE 1 a current ramp generator circuit which employs all solid-state components and which will generate an output current having a wave form of the type shown in FIGURE 2.

The circuit of FIGURE 1 operates to convert a square wave input signal to a linear current ramp signal. Timing capacitor **1** is the timing capacitance which controls the time duration of the ramp. Resistors **2** and **3** comprise the timing resistance and may be identical in value for a symmetrical output signal and may be selected to have differing resistance values should it be desired to provide an asymmetrical ramp. The input square wave is applied to input terminal **4**; this signal swings between the voltage levels identified as E_2 and E_3.

To achieve linearity of the output ramp signal, which appears at output terminal **5**, the charging or discharging of capacitor **1** must be accomplished with essentially constant currents. This charging is accomplished via transistors **6** and **7**. Current amplification is provided by cascaded transistors **8** and **9**.

Operating potentials E_1, E_2, and E_4 are supplied to terminals **10**, **11**, and **12**, respectively. Emitter **14** of transistor **9** is connected to the supply voltage terminal **11** via emitter resistor R_E identified as **15**. The current amplification provided keeps the current I_B small with respect to the charging current $\pm I_{CT}$. Since both transistors **6** and **7** are always on, the voltage level E_2 or E_3 on timing capacitor **1** can be maintained indefinitely.

Current will flow in transistor **9** only when its base **13** is less positive than E_2. Hence, if base **13** is driven to

E_2 volts, transistor **9** will be cut off. Now if the base **13** voltage of transistor **9** is lowered in a linear manner to the signal voltage level E_3, the emitter **14** voltage of transistor **9** will also decrease in a linear manner to the signal voltage level E_3. As can be seen, the current will increase in a linear manner in transistor **9** from essentially zero current to a final value proportional to

$$\frac{E_2-E_3}{R_E}$$

Likewise, as transistor **9** is cut off in a linear manner by the signal voltage on capacitor **1**, the current through transistor **9** will decrease linearly to zero.

Emitter **16** is directly coupled to base **13** and is referenced to supply potential E_1 via emitter resistor **17**.

The positive charge current $+I_{CT}$ flows through diode **18** from collector **19**; conversely, negative charge current $-I_{CT}$ flows through diode **20** to collector **21**. Note that the polarity of transistor **7** has complementary symmetry to that of transistor **6**. The input signal is applied simultaneously to bases **22** and **23** with the positive-going and negative-going portions of the signal being routed through an appropriate one of diodes **18** and **20**.

The ramp amplitude may be selectively controlled by varying R_E; this may be done independently of the ramp duration, the latter being selectively controlled by the value of timing resistances **2** and **3**.

There is shown in FIGURE 2 the wave form of the output appearing at terminal **5**. The output current I_o may be caused to first rise to a selected level

$$\frac{E_2-E_3}{R_E}$$

and thereafter linearly decrease to zero. While the particular wave form shown in FIGURE 2 is very nearly symmetrical, it should be understood that the timing resistance and the timing capacitance may be varied independently to create asymmetrical up-ramp and down-ramp wave shapes.

In order to utilize the ramp generator circuit of FIGURE 1 in the deflection system of a magnetically deflected cathode ray tube, a plurality of ramp generators may have their outputs summed and amplified; an arrangement for accomplishing this is shown in black diagram form in FIGURE 3. There is shown three separate ramp generators **22**, **23**, and **24** having their outputs combined and supplied to the inputs of current amplifier **25**. A resistance network may be used to sum the outputs of generators **22–24** in a manner well known to those skilled in the art. Amplifier **25** may, for example, be of the emitter follower type. The output of amplifier **25** is supplied to one terminal of horizontal deflection coil **26** of the cathode ray tube; the other terminal is referenced to ground **27**. Similarly, the outputs of ramp generators **28**, **29**, and **30** may be summed and amplified through emitter follower **31** and supplied to vertical deflection coil **32**. Input control signals in the form of square waves are applied to input terminals **33–38**. There will result a one-to-one time correspondence between the interval or duration of the horizontal and vertical deflection currents. Each trace on the cathode ray tube screen is of constant time duration and ultimately results in proportionately equal deflection increments.

If it is desired to employ electrostatic deflection, rather than magnetic deflection, the output of amplifiers **25** and **31**, each can be made to drive a resistor across which would appear a voltage proportional to the sum of the several current inputs, as will be obvious to those skilled in the art.

Referring now to FIGURE 4, there is shown an alternative circuit for implementing the method of the invention whereby deflection currents (both horizontal and vertical) are controlled so that any change in the currents will occur in the same time interval, independently of

the magnitude of the current change. The circuit comprises several parallel branches each connected between common busses **39** and **40**. Each branch comprises a resistor R (identified as **41–44**), an inductor L (identified as **45–48**), and a switch (**49–52**). A supply voltage E, applied to busses **39** and **40**, is maintained across the branch networks, and hence the current flow I_t is proportional to the supply voltage E divided by the parallel sum of the resistors (i.e. **41–44**) that are connected in the circuit.

To show that the time required for the current (I) to reach its final value is a constant, assume the following:

$$R>>R_1 \left\{\begin{array}{l}\text{The resistance of the}\\ \text{inductor is small with}\\ \text{respect to R}\end{array}\right.$$

$$L_2=\frac{L_1}{2} \qquad R_2=\frac{R_1}{2}$$

$$L_3=\frac{L_1}{4} \qquad R_3=\frac{R_1}{4}$$

$$L_n=\frac{L_1}{(2^{n-1})} \qquad R_n=\frac{R_1}{(2^{n-1})}$$

The current through any branch circuit is given by

$$i=\frac{E}{R}\left(1-e^{\frac{-R_t}{L}}\right)$$

By direct substitution in the equation for *i*, it can be shown that the time constant of the branch is a constant.

$$i_1=\frac{E}{R_1}\left(1-e^{\frac{-R_1 t}{L_1}}\right)$$

$$\tau=\frac{L}{R}\rightarrow=\tau_1=\frac{L_1}{R_1}$$

$$\tau_2=\frac{L_2}{R_2}=\frac{\frac{L_1}{2}}{\frac{R_1}{2}}=\frac{L_1}{R_1}$$

$$\tau_n=\frac{L_n}{R_n}=\frac{\frac{L_1}{2^{n-1}}}{\frac{R_1}{2^{n-1}}}=\frac{L_1}{R_1}$$

There have been thus disclosed two embodiments of a circuit for producing a linear ramp signal in which the time duration and the maximum signal amplitude may be selectively and independently varied. It will be apparent that the embodiments shown are only exemplary and that various changes and modifications may be made, by those skilled in the art, without departing from the invention as described in the appended claims.

What is claimed is:

1. In a cathode ray tube deflection system, a ramp signal generator comprising a timing capacitor, a source of operating potential, first and second charging circuits for said capacitor, each of said charging circuits comprising a transistor and a diode, each of said transistors having a first control electrode connected to said source of operating potential and a second control electrode connected to an electrode of its corresponding diode, the other electrode of each diode being connected to a common point, said timing capacitor being connected between ground and said common point, a common junction for a third control electrode of each of said transistors, means for applying an input control signal to said common junction, said control signal varying between a first level and a second level such as to positively charge said capacitor through said first charging circuit and to negatively charge said capacitor through said second charging circuit, and an output terminal connected to said common point from which the generated ramp signal may be obtained.

2. In a linear current ramp generator for generating

ramp signals having selectively variable slopes and fixed time bases, a source of operating potential, a plurality of branch circuits adapted to be selectively connected in parallel across said source of operating potential and thereby select said slopes, each of said branch circuits comprising an inductance, a resistance, and a switch connected in series, said switches selectively closing said series branch circuits to place said circuits across said source of operating potential, and said series inductances linearizing the current flow through the resistances which are coupled across the source of operating potential.

3. A linear wave generator comprising, in combination, charge storage means, a source of direct potential, first and second charging circuits for said charge storage means, each of said charging circuits comprising a transistor and a diode, each of said transistors having a first control electrode connected to said source of direct potential and a second electrode connected to an electrode of its corresponding diode, the other electrode of each diode being connected to a common point, said charge storage means being connected between ground and said common point, a common junction for a third control electrode of each of said transistors, means for selectively supplying a signal voltage to said common junction, said first charging circuit being responsive to said signal voltage to apply a positive charging current to said charge storage means and said second charging circuit being responsive to a change in sign of said signal voltage to apply a negative charging current to said charge storage means, and a current amplifier connected to said common point.

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DAVID G. REDINBAUGH, *Primary Examiner.*

RALPH NILSON, ROBERT SEGAL, *Examiners.*

D. E. SRAGOW, J. E. BECK, *Assistant Examiners.*