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(54) Title: METHOD FOR STACKING SEMICONDUCTOR CHIPS

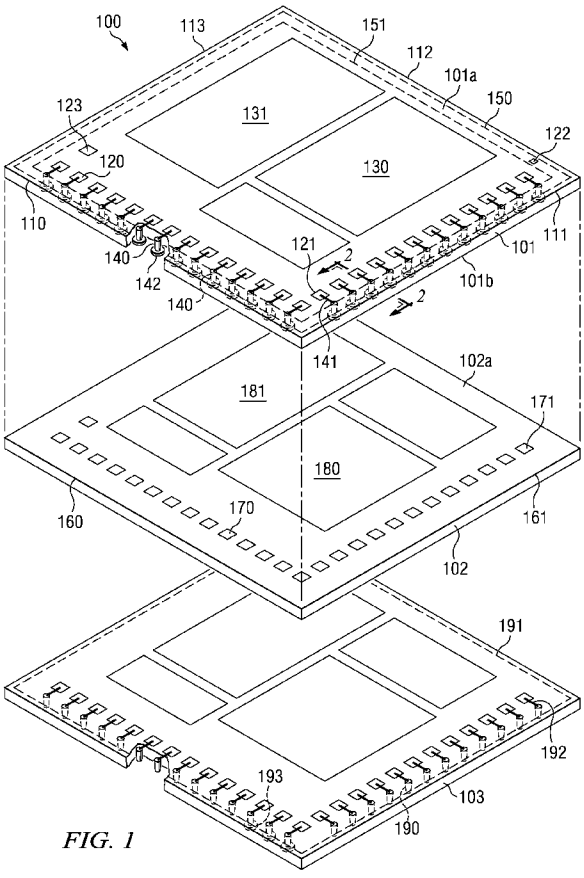

FIG. 1

(57) Abstract: In a semiconductor system (100) including a chip (101) and a workpiece (102), the chip has metal-filled vias (140) positioned between contact pads (120) and the respective edges (110). In addition, seals against microcracks (150) and thermo-mechanical stress (151) are located between the vias and the active components, and sometimes also between the vias and the respective nearest edge. Workpiece may be another semiconductor chip or a substrate; it has contact pads (170) matching the locations of the vias. The chip is vertically stacked on the workpiece so that each contact pad is aligned and in electrical contact with the corresponding via.

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC8 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS (KIPO internal) and keywords "vias, crack, microcrack, seal, metal, insulator, trench, thermo, stress, and similar terms"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005-0104181 A1 (Kang-Wook Lee et al.) 19 May 2005 See abstract, Figures 1-9 and claims 1-34	1-16
A	US 2007-0176295 A1 (IBM CORPORATION) 21 August 2007 See abstract, Figures 1-30 and claims 1-6	1-16
A	KR 10-0753415 B1 (HYNIX SEMICONDUCTOR INC.) 23 August 2007 See abstract, Figures 1-3 and claims 1-4	1-16

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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KR 10-0753415 B1	23.08.2007	JP 2007-251145 A US 2007-222050 A1	27.09.2007 27.09.2007