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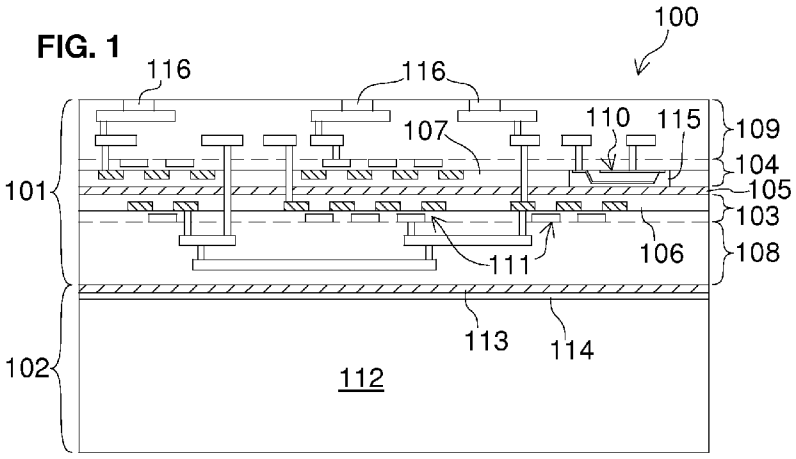
(54) Title: SEMICONDUCTOR STRUCTURE WITH MULTIPLE ACTIVE LAYERS IN AN SOI WAFER

FIG. 1



(57) Abstract: An semiconductor on insulator wafer has an insulator layer between a substrate layer and a semiconductor layer. A first active layer is formed in and on the semiconductor layer. A second active layer is formed in and on the substrate layer. In some embodiments, a handle wafer is bonded to the semiconductor on insulator wafer, and the substrate layer is thinned before forming the second active layer. In some embodiments, a third active layer may be formed in the substrate of the handle wafer. In some embodiments, the first and second active layers include a MEMS device in one of these layers and a CMOS device in the other.

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Semiconductor Structure with Multiple Active Layers in an SOI Wafer

Background of the Invention

[0001] This application claims priority to U.S. Non-Provisional Patent Application No. 14/454,262, filed on August 7, 2014 and entitled "Semiconductor Structure with Multiple Active Layers in an SOI Wafer", which is hereby incorporated by reference for all purposes.

Background of the Invention

[0002] Integrated circuits (ICs) vertical integration techniques utilize multiple active/device layers on a single die. These techniques allows for a significant increase in the number of components per IC without increasing the required die area. The die thickness may be increased, but it is the die area that is usually more of a limiting design consideration, and the overall result can be a reduced total die volume and IC package weight. The development of vertical integration techniques is, thus, of paramount importance for technologies in which electronic devices must be relatively small and lightweight, e.g. cell/smart phones, notebook/tablet PCs, etc.

Summary

[0003] Embodiments of the present invention involve a semiconductor structure with multiple active layers formed from an SOI wafer. The typical SOI wafer has an insulator layer (e.g. a buried oxide) between a substrate layer and a semiconductor layer. A first active layer is formed in and on the semiconductor layer. A second active layer is formed in and on the substrate layer. In some embodiments, a handle wafer is bonded to the SOI wafer, and the substrate layer is thinned before forming the second active layer. In some embodiments, a third active layer may be formed in the substrate of the handle wafer. In some embodiments, the first and second active layers include a MEMS device in one of these layers and a CMOS device in the other.

[0004] A more complete appreciation of the present disclosure and its scope, and the manner in which it achieves the above noted improvements, can be obtained by

reference to the following detailed description of presently preferred embodiments taken in connection with the accompanying drawings, which are briefly summarized below, and the appended claims.

Brief Description of the Drawings

[0005] Fig. 1 is a simplified cross-section of a semiconductor structure incorporating an embodiment of the present invention.

[0006] Figs. 2-5 are simplified cross-sections of semiconductor structures at intermediate stages in the fabrication of the semiconductor structure shown in Fig. 1 in accordance with embodiments of the present invention.

[0007] Fig. 6 is a simplified cross-section of an alternative semiconductor structure incorporating an embodiment of the present invention.

Detailed Description of the Invention

[0008] According to some embodiments, the present invention achieves vertical integration of active layers in a monolithically formed IC semiconductor structure (e.g. semiconductor structure 100 of Fig. 1) using a semiconductor-on-insulator (SOI) wafer. In general, after a first active layer is formed in and on the SOI wafer, the SOI wafer is inverted, and a second active layer is formed in and on the underlying substrate, as described in more detail below. This technique generally enables a relatively compact vertical integration of a variety of types of active layers with a significant reduction of die area and an increase in die per wafer. Additionally, in some embodiments, the multiple active layers may enable the integration of CMOS devices in the same monolithic semiconductor structure with other types of devices, such as film bulk acoustic resonators, surface acoustic wave devices, film plate acoustic resonators (FPAR), acoustic filters, RF switches, passive components, and other microelectromechanical systems (MEMS) devices.

[0009] In the example shown in Fig. 1, the semiconductor structure 100 generally has an inverted SOI wafer 101 bonded with a handle wafer 102. The SOI wafer 101 generally has two active layers 103 and 104 on both opposite sides (i.e. top/bottom or upper/lower) of an insulator layer 105 (e.g. a buried oxide). The first active layer 103 is formed in and on the conventional semiconductor layer 106 of the SOI wafer 101. The second active layer 104 is formed in and on the underlying conventional

substrate layer 107 of the SOI wafer 101, or the portion that remains after thinning the original substrate layer 107. The components that are shown within the active layers 103 and 104 are provided for illustrative purposes only and do not necessarily depict limitations on the present invention.

[0010] Additionally, the SOI wafer 101 generally includes interconnect layers 108 and 109, through which electrical connections may be made between the various components of the active layers 103 and 104. The components that are shown within the interconnect layers 108 and 109 are provided for illustrative purposes only and do not necessarily depict limitations on the present invention. In some embodiments, for example, one of the active layers (e.g. 104) may include an RF/MEMS device 110 (among other components), and the other active layer (e.g. 103) may include CMOS devices 111 (among other components) for circuitry that controls operation of the MEMS device 110.

[0011] The handle wafer 102 generally includes a handle substrate layer 112, a bonding layer 113, and an optional trap rich layer (TRL) 114. The handle wafer 102 is bonded to a top surface of the SOI wafer 101 (inverted as shown) after the formation of the first active layer 103 and the first interconnect layer 108. The handle wafer 102 is generally used to provide structural stability for the semiconductor structure 100 while processing the substrate layer 107 of the SOI wafer 101 and the formation of the second active layer 104 and second interconnect layer 109. In some embodiments, the structural stability aspect enables the substrate layer 107 of the SOI wafer 101 to be thinned before formation of the second active layer 104.

[0012] The first and second active layers 103 and 104 and the first and second interconnect layers 108 and 109 are described herein as being built up both into and onto the semiconductor layer 106 and substrate layer 107, respectively. This type of fabrication technique is known as a “monolithic” style of fabrication. A different technique of active layer fabrication is known as a “layer transfer” style, which involves the formation of the active layers in and on multiple separate wafers, followed by transferring one of the active layers onto the wafer of the other. There are various advantages and disadvantages for both of these techniques. The monolithic style, for example, generally requires serial processing for each of the manufacturing steps; whereas, the layer transfer style allows for parallel processing of the multiple wafers, thereby potentially reducing the overall time to manufacture the final semiconductor structure. However, the monolithic style generally does not

require the expense of multiple substrates, does not require wafer bonding or wafer cleavage steps, does not require significant grinding or etching back steps, does not require precision wafer-aligning for bonding, and does not require a capital investment for fabrication machines that can perform the wafer-bonding-related steps. Some general exceptions to these advantages may occur in some situations, such as the wafer bonding of the handle wafer 102. However, since the handle wafer 102 does not have additional circuitry prior to bonding, there is no need for a high-precision alignment of the wafers 101 and 102. Thus, the bonding step for the handle wafer 102 can be relatively simple and cheap compared to approaches where multiple active layers on multiple wafers are integrated via a layer transfer process.

[0013] A simplified example manufacturing process, according to some embodiments for forming the semiconductor structure 100 of Fig. 1, is shown by Figs. 2-5. The process generally starts with the SOI wafer 101 having the insulator layer 105 (e.g. a buried oxide) between the semiconductor layer 106 and substrate layer 107 as shown in Fig. 2. The first active layer 103 is then formed into and onto the "top" or "upper" surface of the semiconductor layer 106 using mostly conventional process steps. In situations where the active devices in active layer 103 are CMOS transistors, these process steps are those typically associated with single wafer monolithic CMOS manufacturing. Additionally, instead of or in addition to the TRL 114 in the handle wafer 102, the SOI wafer 101 may include a TRL formed as disclosed in U.S. Pat. App. __/___,___ filed on the same day as the present application with attorney docket number IOSEP009CIP4. The disclosure of which is incorporated by reference herein in its entirety.

[0014] The first interconnect layer 108 is then formed on the "top" or "upper" surface of the first active layer 103. Since the SOI wafer 101 is subsequently inverted from the orientation shown in Fig. 2, for the benefit of consistency in description, the portion of the SOI wafer 101 referred to as the "top" (or "upper" or "front") with respect to Fig. 2 will continue to be referred to herein as the "top" (or "upper" or "front"), and the portion of the SOI wafer 101 referred to as the "bottom" (or "lower" or "back") will continue to be referred to herein as the "bottom" (or "lower" or "back"), even after the SOI wafer 101 has been inverted. Therefore, in Fig. 1, the "top" of the overall semiconductor structure 100 is considered the same as the "bottom" of the SOI wafer 101. Also, when the top of the overall semiconductor

structure 100 is being processed, it is considered "back side" processing for the SOI wafer 101.

[0015] Additionally, for purposes of description herein, when material or layers are added to a wafer, the added material or layers are considered to become part of the wafer. Also, when material or layers are removed from the wafer, the removed material or layers are no longer considered to be part of the wafer. Therefore, for example, the element designated as the SOI wafer 101 or the handle wafer 102 in the Figs. may increase or decrease in size or thickness as it is being processed.

[0016] Also, for purposes of description herein, a surface referred to as the "top surface" or "bottom surface" of a wafer may change during processing when material or layers are added to or removed from the wafer. For example, the first active layer 103 is formed by front side processing in and on the top surface of the SOI wafer 101, but the material that is placed on the SOI wafer 101 creates a new top surface. Thus, the first interconnect layer 108 is formed on the new top surface. Then when the handle wafer 102 is bonded to the SOI wafer 101, it is bonded to yet another new top surface thereof.

[0017] Furthermore, various layers of materials are described herein. However, there is not necessarily a distinct demarcation line between some of the layers. For example, some materials formed during fabrication of the interconnect layers 108 or 109 may extend into other layers. Through semiconductor vias (TSVs), for example, may be formed through the active layers 103 or 104 and the insulator layer 105. Other examples of overlapping layers may also become apparent.

[0018] The simplified example manufacturing process, according to some embodiments for forming the semiconductor structure 100 of Fig. 1, continues with the formation of the handle wafer 102 as shown in Fig. 3. The bonding layer 113, and the TRL 114 are formed on the handle substrate layer 112. The handle substrate layer 112 is generally thick enough to provide structural stability or strength to the semiconductor structure 100. The TRL 114 is formed by any appropriate technique, e.g. implanting ions of high energy particles (e.g. a noble gas, Silicon, Oxygen, Carbon, Germanium, etc.), irradiating the handle wafer 102, depositing high resistivity material, damaging the exposed surfaces of the handle substrate layer 112, etc. In some embodiments, the TRL 114 is formed as disclosed in U.S. Pat. App. __/___,___ filed on the same day as the present application with attorney docket number IOSEP009CIP4. The disclosure of which is incorporated by reference

herein in its entirety. The bonding layer 113 may be any appropriate material that can be bonded to the material at the top surface of the SOI wafer 101. Other bonding techniques for other embodiments with or without the bonding layer 113 may also be used. In some embodiments, the bonding layer 113 may be combined with the TRL 114. In some embodiments, the entire handle wafer 102 will be the TRL 114.

[0019] As shown in Fig. 4, SOI wafer 101 of Fig. 2 is bonded to the handle wafer 102 of Fig. 3. The SOI wafer 101 is inverted in Fig. 4 relative to its orientation in Fig. 2. The surface of the SOI wafer 101 to which the handle wafer 102 is bonded is the top surface, which is opposite the insulator layer from the substrate layer 107. This step leaves the bottom or back side of the SOI wafer 101 exposed for processing. The handle wafer 102 provides structural stability during this processing.

[0020] A portion of the substrate layer 107 is removed, thereby thinning the substrate layer 107, as shown in Fig. 5. The remaining portion of the substrate layer 107 is sufficiently thick to be used as a new semiconductor layer for the formation of a second active layer, such as the second active layer 104 in Fig. 1.

[0021] In some embodiments, since the MEMS device 110 is to be formed in the second active layer 104, a cavity 115 may be formed in the substrate layer 107. The cavity 115 at least partly surrounds the MEMS device 110. The cavity 115 may be formed by any appropriate technique, e.g. orientation dependent etch, anisotropic etch, isotropic etch, etc. The cavity 115 provides isolation, improved thermal performance and/or a material for release of the MEMS device 110. A fill material is then placed inside the cavity 115 and planarized, e.g. by CMP. The fill material may be selective to the material that forms second active layer 104, so the fill material can be removed later to release the MEMS device 110. In some embodiments, the cavity 115 may extend into the insulator layer 105, so the fill material may have to be selective to the insulator material.

[0022] The second active layer 104 is then formed in and on the remaining portion of the substrate layer 107. In some embodiments, fabrication of the MEMS device 110 within the second active layer 104 is done in reverse order from the conventional process. This reverse process may aid in simplifying the bonding and interconnection for low temperatures (e.g. less than 200℃).

[0023] The second interconnect layer 109 is then formed on the second active layer 104 (and through the two active layers 103 and 104) to produce the semiconductor structure 100 shown in Fig. 1. In some embodiments, some of the electrical connections between the two active layers 103 and 104 may be formed with a buried contact, e.g. forming TSVs early in the overall fabrication process. Electrical connection pads 116 and a redistribution layer (not shown) may also be formed for external electrical connections. Electrical interconnects, e.g. TSVs, that pass through more than one layer may provide electrical connections between any two or more components in the two interconnect layers 108 and 109 and the active layers 103 and 104, e.g. a TSV interconnect between metallization in the interconnect layers 108 and 109, or a TSV interconnect between metallization in one of the interconnect layers 108 or 109 and an active device (e.g. source, drain or gate region) in one of the active layers 108 or 109.

[0024] An alternative semiconductor structure 200 incorporating an alternative embodiment of the present invention is shown in Fig. 6. In this case, many of the elements are similar to those of the embodiment shown in Fig. 1, because this embodiment may be built up from the semiconductor structure 100. However, a portion of the handle substrate layer 112 is removed, thereby thinning the handle substrate layer 112. The remaining portion of the handle substrate layer 112 is sufficiently thick to be used as a new semiconductor layer for the formation of a third active layer 201, thereby monolithically forming yet another active layer. In some embodiments, another handle wafer (not shown) may be bonded to the semiconductor structure 100 to provide structural stability during subsequent processing if the existing thickness of the semiconductor structure 100 does not provide sufficient structural stability.

[0025] In some embodiments, a MEMS device 202 is formed in the third active layer 201, such thata cavity 203 may need to be formed in the handle substrate layer 112. The cavity 203 may be formed by any appropriate technique, e.g. orientation dependent etch, anisotropic etch, isotropic etch, etc. The cavity 203 provides isolation, improved thermal performance and/or a material for release of the MEMS device 202. A fill material is then placed inside the cavity 203 and planarized, e.g. by CMP. The fill material may be selective to the material of third active layer 201, so the fill material can be removed later to release the MEMS device 202.

[0026] The third active layer 201 is then formed in and on the remaining portion of the handle substrate layer 112.

[0027] A third interconnect layer 204 is then formed on the third active layer 201 (and through to the first active layer 103) to produce the semiconductor structure 200 shown in Fig. 6. In some embodiments, some of the electrical connections between the first and third active layers 103 and 201 may be formed with a buried contact, e.g. forming TSVs early in the overall fabrication process. The third active layer 201 may also be connected to the second active layer 104 via contacts between those layers and a common circuit node in interconnect layer 108. Electrical connection pads (not shown) and a redistribution layer (not shown) may also be formed for external electrical connections on the bottom side of the alternative semiconductor structure 200. Alternatively or in combination, electrical connection pads 116 and a redistribution layer (not shown) may also be formed for external electrical connections to the bottom side of the alternative semiconductor structure 200.

[0028] Although embodiments of the present invention have been discussed primarily with respect to specific embodiments thereof, other variations are possible. Various configurations of the described system may be used in place of, or in addition to, the configurations presented herein. For example, additional components may be included where appropriate. As another example, configurations were described with general reference to certain types and combinations of semiconductor components, but other types and/or combinations of semiconductor components could be used in addition to or in the place of those described.

[0029] Those skilled in the art will appreciate that the foregoing description is by way of example only, and is not intended to limit the present invention. Nothing in the disclosure should indicate that the present invention is limited to systems that have the specific type of semiconductor components shown and described, unless otherwise indicated in the claims. Nothing in the disclosure should indicate that the present invention is limited to systems that require a particular form of semiconductor processing or integrated circuits, unless otherwise indicated in the claims. In general, any diagrams presented are only intended to indicate one possible configuration, and many variations are possible. Those skilled in the art will also appreciate that methods and systems consistent with the present invention are suitable for use in a wide range of applications.

[0030] While the specification has been described in detail with respect to specific embodiments of the present invention, it will be appreciated that those skilled in the art, upon attaining an understanding of the foregoing, may readily conceive of alterations to, variations of, and equivalents to these embodiments. These and other modifications and variations to the present invention may be practiced by those skilled in the art, without departing from the spirit and scope of the present invention, which is more particularly set forth in the appended claims.

Claims

What is claimed is:

1. A method comprising:

providing an semiconductor on insulator wafer having an insulator layer between a substrate layer and a semiconductor layer;

forming a first active layer in and on the semiconductor layer; and

forming a second active layer in and on the substrate layer.

2. The method of claim 1, further comprising:

removing a first portion of the substrate layer; and

forming the second active layer in and on a second portion of the substrate layer.

3. The method of claim 2, further comprising:

before the removing of the first portion of the substrate layer, bonding a handle wafer to a first surface of the semiconductor on insulator wafer; and

removing the first portion of the substrate layer from a second surface of the semiconductor on insulator wafer.

4. The method of claim 3, further comprising:

providing a trap rich layer in the handle wafer.

5. The method of claim 1, further comprising:

bonding a handle wafer to a surface of the semiconductor on insulator wafer, the surface of the semiconductor on insulator wafer being opposite the insulator layer from the substrate layer, and the handle wafer having a handle substrate layer; and

forming a third active layer in and on the handle substrate layer.

6. The method of claim 5, further comprising:

removing a first portion of the handle substrate layer; and

forming the third active layer in and on a second portion of the handle substrate layer.

7. The method of claim 1, further comprising:

forming an interconnect layer on the second active layer; and

forming electrical connections between the interconnect layer and the first and second active layers.

8. The method of claim 1, further comprising:

forming a MEMS device in and on the substrate layer.

9. The method of claim 8, further comprising:

forming a cavity for the MEMS device in at least one of: the substrate layer and the insulator layer.

10. The method of claim 8, wherein:

the forming of the first active layer further comprises forming a CMOS device; and

the method further comprises forming an electrical connection between the CMOS device and the MEMS device, the CMOS device providing a control signal for the MEMS device through the electrical connection.

11. A semiconductor structure comprising:

an semiconductor on insulator wafer having an insulator layer between a semiconductor layer and a substrate layer;

a first active layer formed in and on the semiconductor layer; and

a second active layer formed in and on the substrate layer.

12. The semiconductor structure of claim 11, wherein:

the second active layer is formed in and on a remaining portion of the substrate layer after the substrate layer has been thinned.

13. The semiconductor structure of claim 12, further comprising:

a handle wafer bonded to a surface of the semiconductor on insulator wafer

opposite the insulator layer from the substrate layer.

14. The semiconductor structure of claim 13, wherein:
the handle wafer has a trap rich layer.

15. The semiconductor structure of claim 11, further comprising:
a handle wafer bonded to a surface of the semiconductor on insulator wafer, the surface of the semiconductor on insulator wafer being opposite the insulator layer from the substrate layer, the handle wafer having a handle substrate layer; and
a third active layer formed in and on the handle substrate layer.

16. The semiconductor structure of claim 15, wherein:
the third active layer is formed in and on a remaining portion of the handle substrate layer after the handle substrate layer has been thinned.

17. The semiconductor structure of claim 11, further comprising:
an interconnect layer formed on the second active layer; and
electrical connections between the interconnect layer and the first and second active layers.

18. The semiconductor structure of claim 11, further comprising:
a MEMS device formed in and on the substrate layer.

19. The semiconductor structure of claim 18, further comprising:
a cavity surrounding at least part of the MEMS device, the cavity being formed in at least one of: the substrate layer and the insulator layer.

20. The semiconductor structure of claim 18, wherein:
the first active layer includes a CMOS device; and
the CMOS device provides a control signal for the MEMS device.

FIG. 1

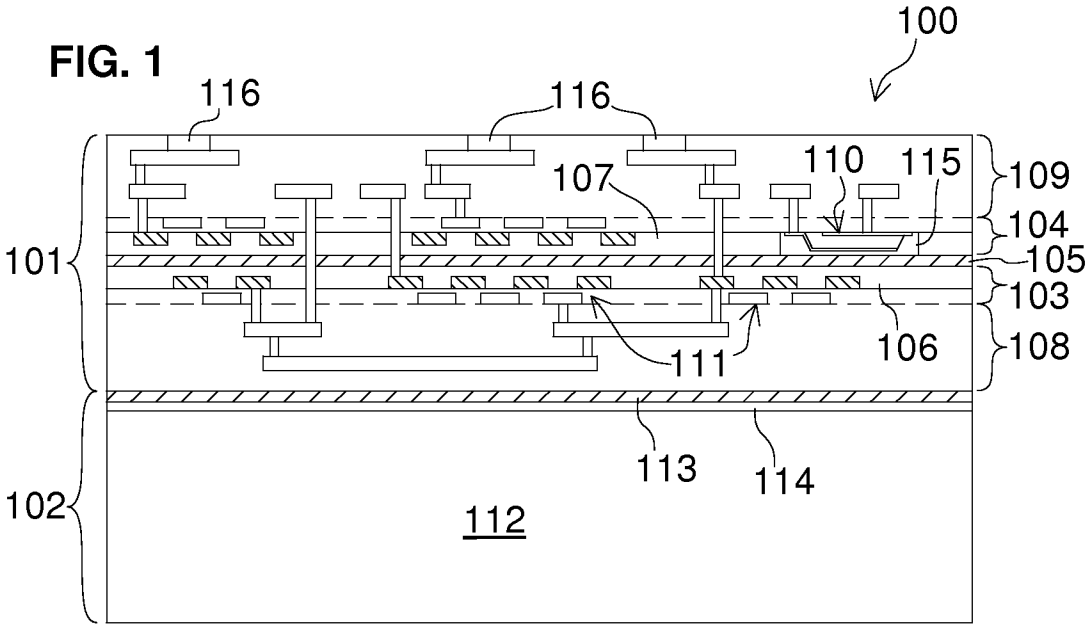

FIG. 2

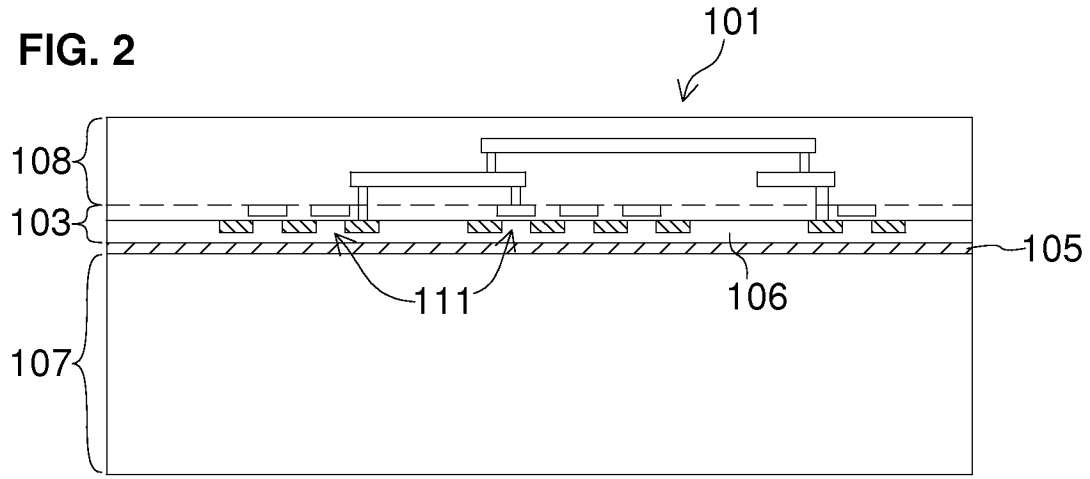

FIG. 3

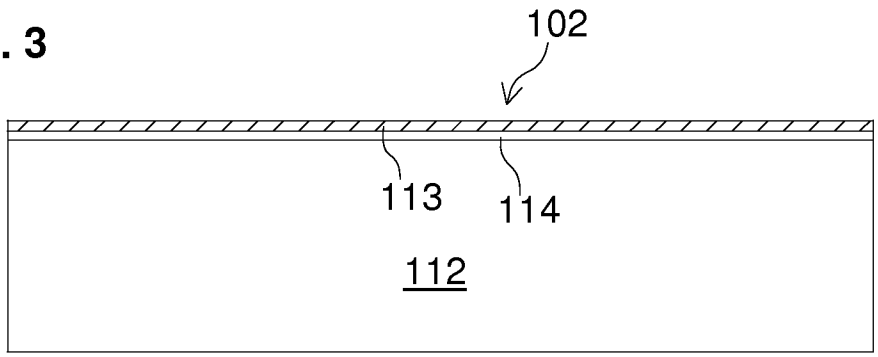

FIG. 4

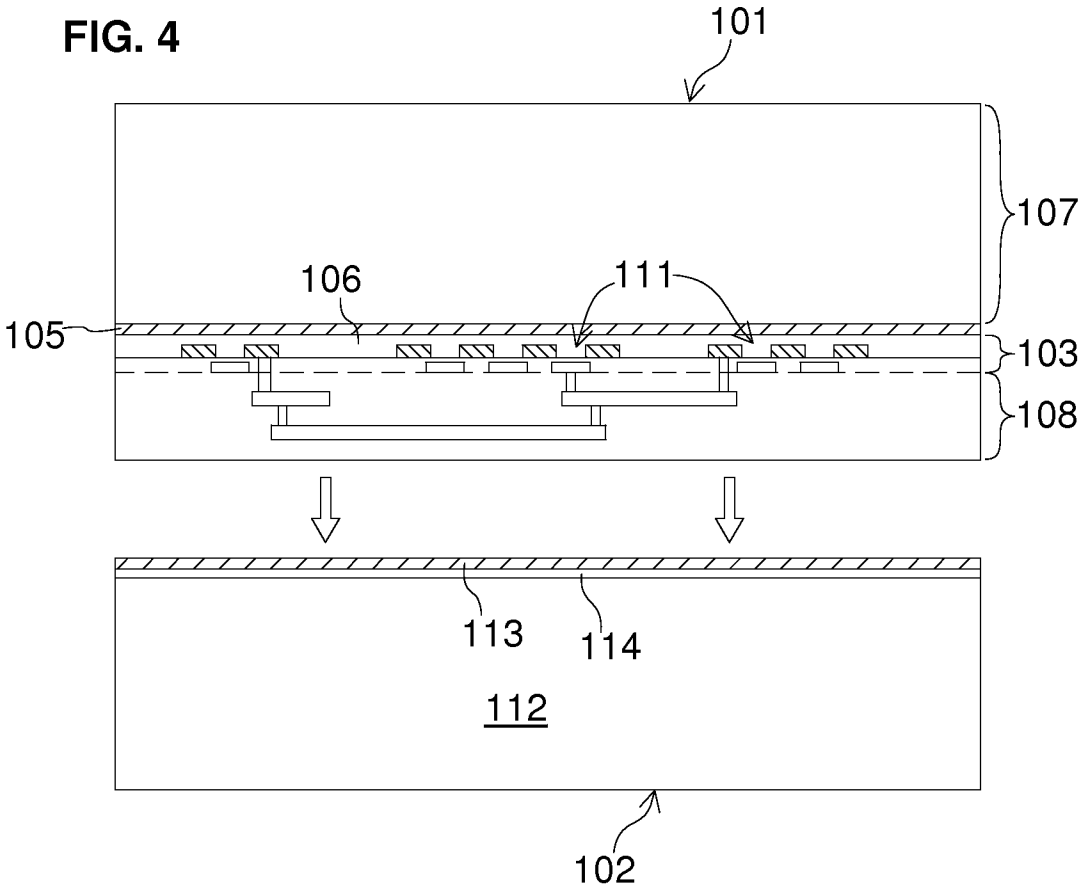
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FIG. 5

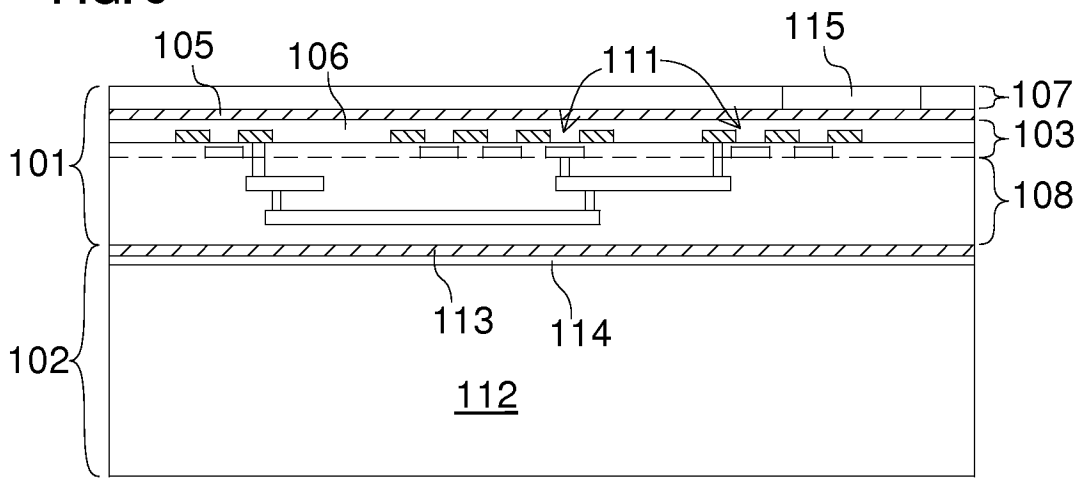
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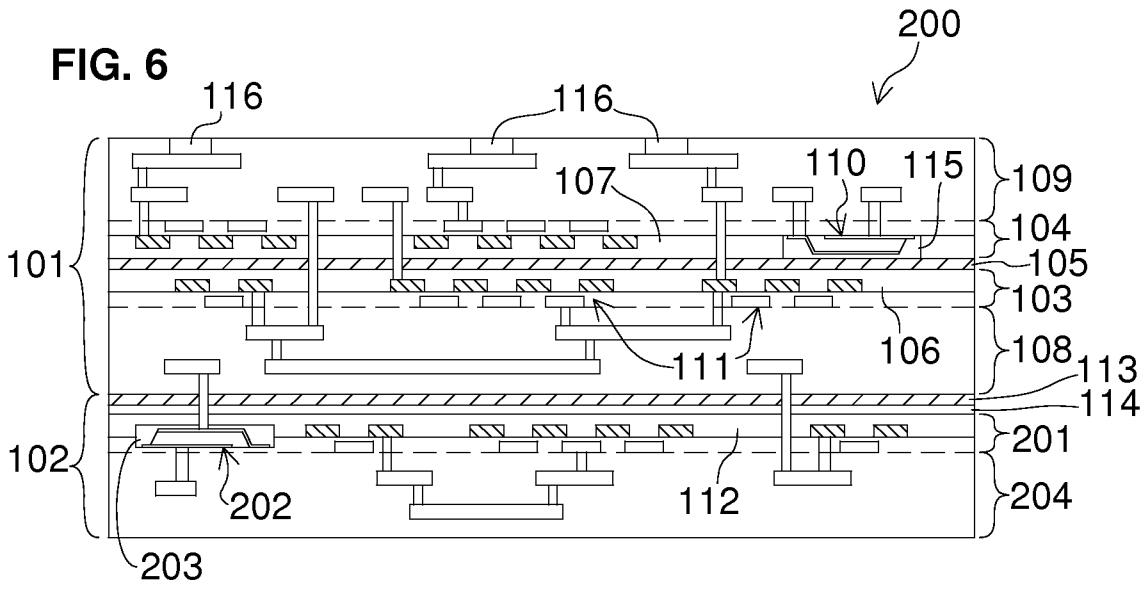
FIG. 6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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US15/41769

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/762, 21/8238, 23/485 (2015.01)
CPC - H01L 21/762, 21/8238, 23/485
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): H01L 21/762, 21/8238, 23/485 (2015.01)
CPC: H01L 21/762, 21/8238, 23/485,.2221/68368; USPC: 438/479

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC); Google Patent; Google; Google Scholar; ProQuest; Semiconductor, insulator, SOI, wafer, active, substrate, layer, handle, trap, CMOS, MEMS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2008/0179678 A1 (DYER, TW et al.) 31 July 2008; figures 1-3, 5-7, 9-13; paragraphs [0006], [0009], [0041]-[0053], [0056], [0061]-[0066]	1-3, 7-9, 11-13, 17-19 ---------- 4-6, 10, 14-16, 20
Y	US 8,466,036 B2 (BRINDLE, C et al.) 18 June 2013; figure 3; column 9, lines 45-67; column 10, lines 6-41	4-6, 14-16
Y	US 8,334,729 B1 (KHLAT, N) 18 December 2012; figure 2; column 9, lines 9-13, 61-67; column 10, lines 1-2	10, 20
P, Y	US 2015/0179505 A1 (SILANNA SEMICONDUCTOR USA, INC.) 25 June 2015; entire document	1-20
A	US 8,368,143 B2 (BEDELL, SW et al.) 05 February 2013; entire document	1-20
A	US 6,297,090 B1 (KIM, KN) 2 October 2001; entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 September 2015 (30.09.2015)	28 OCT 2015
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