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ASCEND

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SECTION



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July 9, 1968

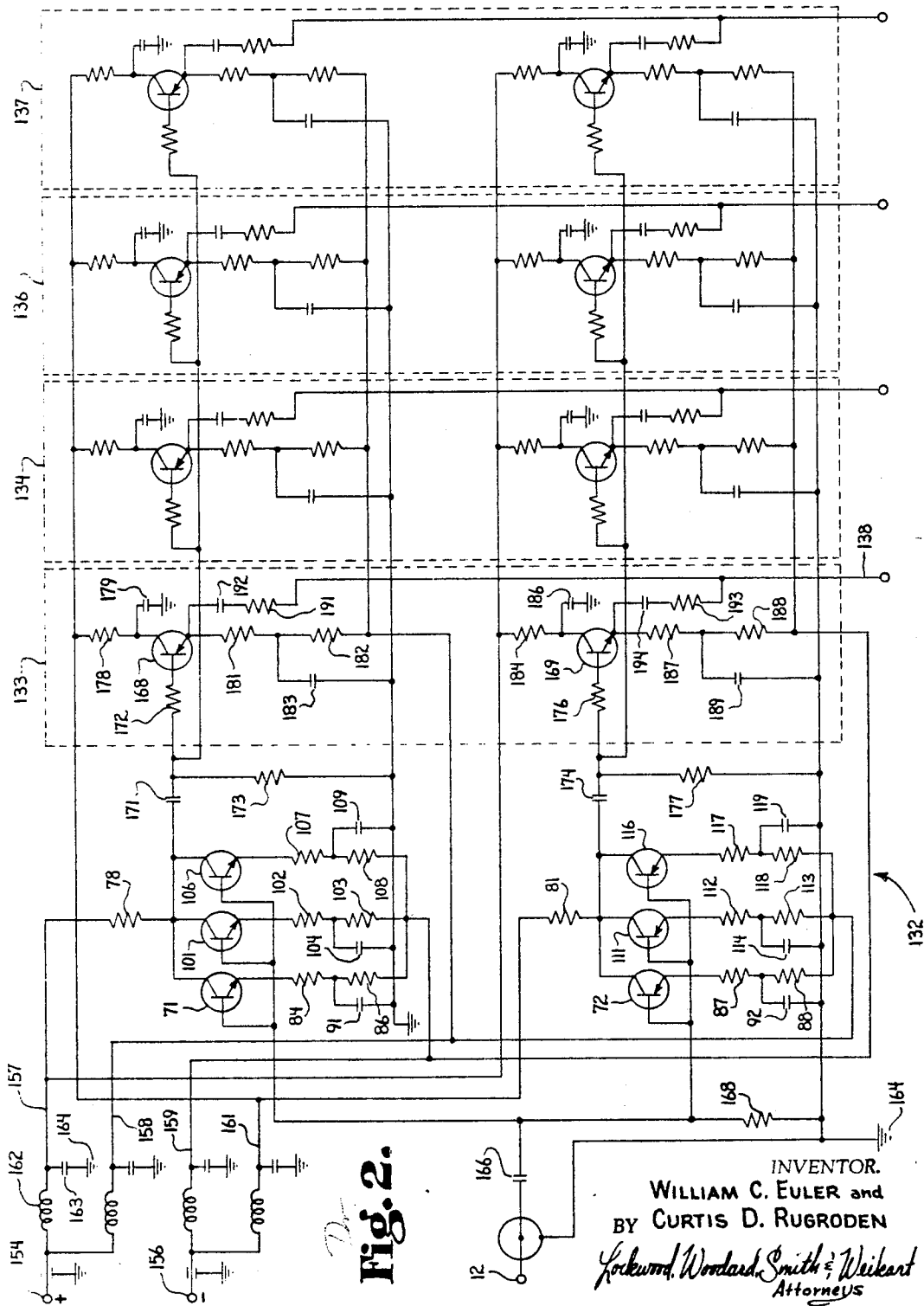
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ANTENNA MULTICOUPLER

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Fig. 4.

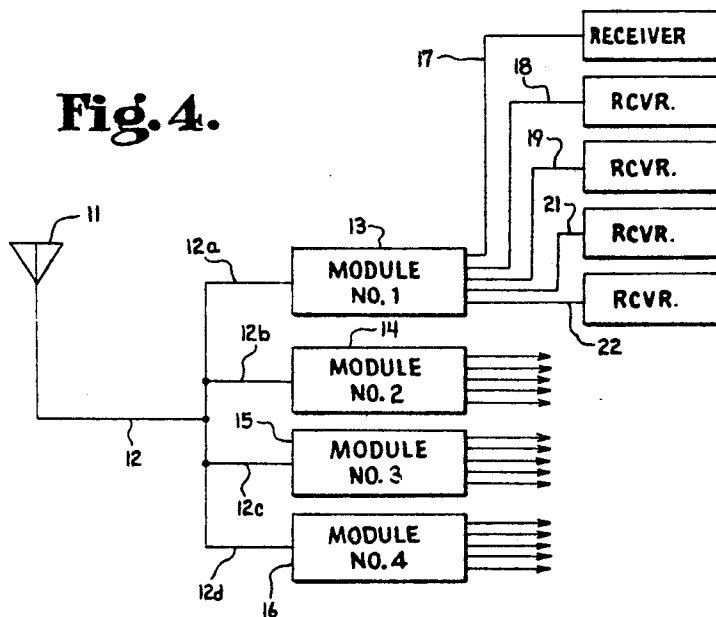
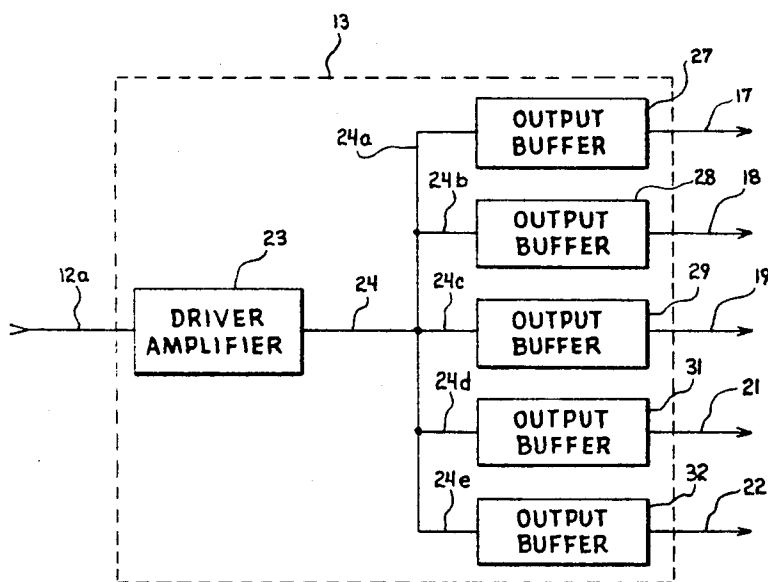


Fig. 5.

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4 Sheets-Sheet 4

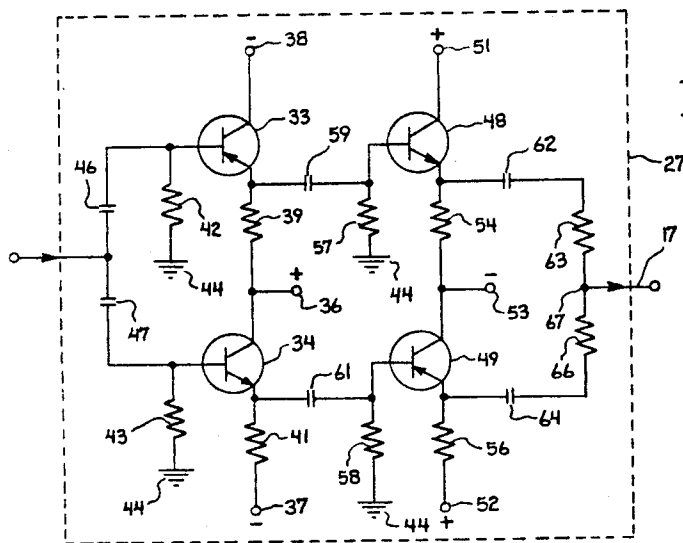


Fig. 6.

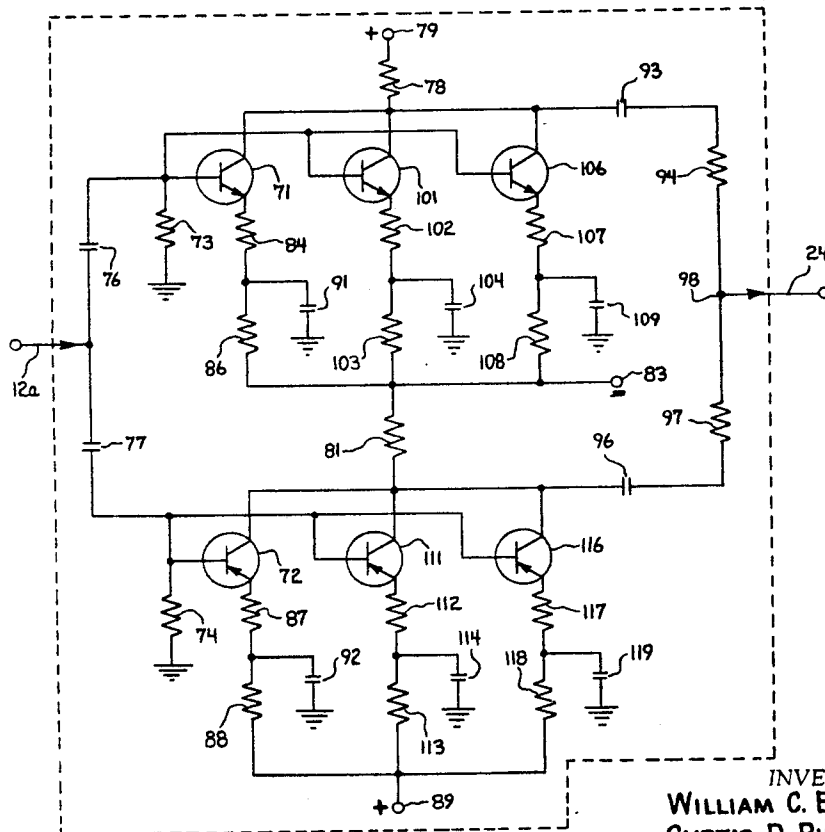


Fig. 7.

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ANTENNA MULTICOUPLER

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This invention relates generally to antenna multicouplers and more particularly to a compact multicoupler capable of coupling many receivers to a single antenna and capable of handling wide bands at high frequencies.

For many years, devices have been needed which are capable of providing optimum coupling between several receivers and a single antenna. Many devices have been built to satisfy this need, and resistive and transformer networks have been used with reasonable success when very few outputs are needed. Where more outputs were needed, vacuum tube versions have been employed.

As communication links in general and receiving sites in particular have become more complex, the number of terminal equipments requiring an antenna input increased beyond the practical limits of most of the available multicouplers. This generally required cascading multicouplers or building more antennas. Cascading multicouplers, in addition to increasing the noise level, added much heat, cost and bulk to the basic installation. Building more antennas is also expensive and requires hard-to-get landscape.

It is, therefore, a general object of the present invention to provide an improved antenna multicoupler.

A further object is to provide a multicoupler occupying very little space, weighing less than 20 pounds, and consuming less than 30 watts of power.

A further object is to provide a multicoupler capable of handling frequencies in the range between 0.1 megacycle and 60 megacycles.

A further object is to provide an antenna multicoupler having an intermodulation distortion of less than -60 decibels (with two 0.25 volt input signals) and having interchannel crosstalk of less than 40 decibels at 60 megacycles.

A further object is to provide an antenna multicoupler of a type whose input and output impedance can be readily matched to antenna and receiving equipment.

A further object is to provide a multicoupler achieving the foregoing objects and well suited to module construction having expandable available outputs of 5, 10, 15 or 20, for example.

A further object is to provide a multicoupler requiring no transformers or L-C coupling devices or tuned circuits therein.

Described briefly, a typical embodiment of the present invention incorporates in a single module a complementary amplifier driving four complementary emitter followers. Each emitter follower drives a set of five channel buffers all of which may be grouped in another module. Each of the channel buffers furnishes an output for a receiver. The driver amplifier and emitter followers are operated Class A and transistors are paralleled in the driver amplifier.

Input and output impedances of the multicoupler are established by selection of resistors, and they are practically unaffected by change of signal frequency. No transformers, L-C coupling devices or tuned circuits are employed.

The full nature of the invention will be understood from the following description and claims and the accompanying drawings wherein:

FIG. 1 is a block diagram of a multicoupler applica-

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tion according to a preferred embodiment of the invention.

FIG. 2 is a schematic diagram of the driver section of the preferred embodiment.

FIG. 3 is a schematic diagram of the channel buffer employed in the preferred embodiment.

FIG. 4 is a block diagram of an early embodiment.

FIG. 5 is a block diagram of one module thereof incorporating features of the invention.

FIG. 6 is a schematic diagram of the output buffer thereof.

FIG. 7 is a schematic diagram of the driver amplifier thereof.

Referring first to the early embodiment shown in FIGS. 4 through 7, antenna 11 (FIG. 4) provides an input to each of four modules 13, 14, 15, and 16, all of which are connected in parallel to the antenna input line 12. Each of the four modules has five outputs. The four modules are identical so the module 13 will be described in detail. Five outputs 17, 18, 19, 21 and 22 are provided from module 13. The input to module 13 is provided by the line 12a whereas inputs to the modules 14, 15 and 16 are provided on the lines 12b, 12c and 12d respectively.

Referring now to FIG. 5, the input 12a and the five output lines are shown. The input is fed to a driver amplifier 23 whose output line 24 is connected in parallel to the inputs 24a, 24b, 24c, 24d, and 24e of output buffers 27, 28, 29, 31 and 32.

All of the output buffers of FIG. 5 are identical and a schematic diagram of buffer 27 is shown in FIG. 6. The output buffer of FIG. 6 includes two Class A complementary emitter follower stages. The first stage includes the PNP transistor 33 and the NPN transistor 34 arranged in complementary symmetry with a positive direct current potential being applied at terminal 36 and negative direct current potential being applied at terminals 37 and 38. Resistor 39 is connected in series between terminal 36 and the emitter-collector path of transistor 33. Similarly resistor 41 is connected between terminal 37 and the emitter-collector path of transistor 34. Resistors 42 and 43 are connected between a point of intermediate potential or ground 44 and the base electrodes of transistors 33 and 34 respectively. D.C. isolation is provided by capacitors 46 and 47.

The second emitter follower stage includes NPN transistor 48 and PNP transistor 49 in complementary symmetry arrangement with positive direct current potential being provided at terminals 51 and 52 and negative direct current potential being provided at terminal 53. Positive terminals 51 and 52 may be tied to the positive terminal 36 and negative terminals 53, 37, and 38 may be tied together, the potentials supplied to the three positive terminals being the same and the potentials supplied to the three negative terminals being the same. A resistor 54 is connected between negative supply terminal 53 and the emitter-collector path of transistor 48 whereas resistor 56 is connected in series between the positive supply terminal 52 and the emitter-collector path of transistor 49. Suitable conventional isolation from the power supply is normally desirable. To simplify the drawing, though, it is not shown.

Resistor 57 is connected between ground and the base of transistor 48 and resistor 58 is connected between ground and the base of transistor 49.

The signal input to transistor 48 is supplied through DC blocking capacitor 59 connected from the emitter of transistor 33 to the base of transistor 48. Similarly, the signal input to transistor 49 is provided by the capacitor 61 connected between the emitter of transistor 34 and the base of transistor 49.

A capacitor 62 is provided between the emitter of transistor 48 and the upper end of resistor 63. The capac-

itor 64 is provided between the emitter of transistor 49 and the lower end of resistor 66. The output line 17 is connected to the junction 67 of resistors 63 and 66.

Transistors 33 and 34 are complementary pairs having reasonably matched characteristics. An example of such a matched pair is a 2N2411 or 2N1143 for transistor 33 and 2N744 for transistor 34. The values of the capacitors 46 and 47 are chosen to provide sufficient coupling at the low frequency extreme of the desired frequency band while maintaining DC isolation. The values of the resistors 42 and 43 should be chosen as low as is compatible with the input requirements, so that the input impedance will tend to be constant with the frequency. Otherwise, transistor beta changes caused by frequency may affect the input impedance of the transistors and affect the circuit input impedance. By keeping resistors 42 and 43 at as low a value as possible, this effect of frequency on beta characteristics will be minimized.

The choice of values of resistances 39 and 41 depends upon the choice of transistors 33 and 34 and upon the output impedance requirements. These resistors set the quiescent current to the transistors. The quiescent current is a compromise between the most linear operation of the individual transistor and the current drive required by the load.

The same parameters affect the selection of components for the second stage. The resistors 63 and 66 establish the output impedance of the circuit. Capacitors 62 and 64 provide DC isolation between the output and the second stage whereas the capacitors 59 and 61 provide DC isolation between the first and second stages while functioning also as signal couplers. By combining signals at the junction of resistors 63 and 66, distortion effects are reduced through cancellation.

By thus employing the transistors in complementary relationship, harmonic distortions are essentially cancelled and, therefore, there is very little intermodulation. The use of high frequency silicon and germanium transistors minimizes noise because of the excellent low noise characteristics of these types of transistors. Because of the cancellation of harmonic distortion, large signals can be handled without intermodulation distortion. On the other hand, conventional transistor techniques fail due to non-linear beta versus current characteristics and the inherently low input impedance.

Referring now to FIG. 7, which is a schematic diagram of the novel driver amplifier employed in the module of FIG. 5, three complementary pairs of transistors are shown. In the first pair, there is employed an NPN transistor 71 and a PNP transistor 72. Resistors 73 and 74 are chosen as described above for the complementary emitter followers, to establish an input impedance which is as nearly independent of input frequency as possible. The input impedance is selected to match that of the antenna with which the multicoupler is to be employed. Capacitors 76 and 77, of course, provide the antenna signal coupling to transistors 71 and 72 respectively and provide DC isolation thereof.

The collector of transistor 71 is connected through a resistance 78 to a source of positive DC potential at terminal 79. The collector of transistor 72 is connected through resistor 81 to a source of negative direct current potential at terminal 83. These resistors are the collector load resistors and should be chosen low enough to provide the required output impedance while being compatible with high frequency performance.

Resistors 84 and 86 are connected in series between the emitter of transistor 71 and the negative terminal 83. Similarly, resistors 87 and 88 are connected in series between the emitter of transistor 72 and the positive input terminal 89. Resistors 84 and 86 establish the quiescent current for transistor 71 whereas resistors 87 and 88 establish the quiescent current for transistor 72. The sum of the values of resistors 84 and 86 should be such that the quiescent current needed for linear operation flows

through transistor 71, and resistors 87 and 88 should be selected so that the sum of their values provides the desired quiescent current in transistor 72. The values of resistors 84 and 87 and those of corresponding resistors for corresponding transistors should be selected to provide input circuit impedance for the transistors which is high compared to the desired multicoupler input impedance, so that decreases of transistor input impedance which may occur at increased input signal frequencies do not significantly affect the multicoupler input impedance. The currents in these transistors must be compromises considering the most linear operational region of the transistor, the collector resistance, and the current required by the output load.

A capacitor 91 is connected between ground and the junction of resistors 84 and 86. Similarly, a capacitor 92 is connected between ground and the junction of resistors 87 and 88. These capacitors are used to decouple the current biasing resistors, capacitor 91 decoupling resistor 86 and the capacitor 92 decoupling resistor 88. The capacitors should be chosen to provide adequate decoupling at the low frequency extreme but not exhibit parallel resonance before the upper extreme.

In what may be called the upper amplifier, an NPN transistor 101 with series connected resistors 102 and 103 is connected between the resistor 78 and the terminal 83. A capacitor 104 is connected between ground and the junction of resistors 102 and 103. Likewise, an NPN transistor 106 whose collector is connected to the collector of transistor 71, has its emitter in series with resistors 107 and 108, the latter mentioned resistor being connected to terminal 83. The capacitor 109 is connected between ground and the junction of resistors 107 and 108. The base electrodes of the three transistors 71, 101 and 106 are connected in common to the upper end of resistor 73. It is apparent, therefore, that these three transistors are parallel in the upper amplifier.

Similarly, in the lower amplifier, PNP transistor 111 has its collector connected to the collector of transistor 72, and has its emitter connected in series with resistances 112 and 113 with the latter being connected to the terminal 89. A capacitor 114 is connected between ground and the junction of resistors 112 and 113. Another PNP transistor 116 is connected in series with resistors 117 and 118, with a capacitor 119 being connected between ground and the junction of resistors 117 and 118.

For each of the transistors, in each of the parallel arrangements, the gain will be the approximate ratio of the collector load resistor divided by the emitter resistor. For example, the gain for transistor 71 will be the approximate ratio of the resistance of resistor 78 divided by the resistance of resistor 84. For transistor 72, the gain will be the approximate ratio of the resistance of resistor 81 divided by the resistance of resistor 87. By providing the three transistors in parallel in each portion of the complementary amplifier, sufficient gain can be obtained to overcome the matching loss on the receivers together with the inherent loss to the emitter followers. By providing each transistor with its own biasing network, any temperature effects are minimized. Furthermore, if the transistors are not quite matched, the biasing resistors may be changed in value in order to effectively eliminate any distortion which might otherwise occur with inadequately matched transistors.

Capacitor 93 provides signal coupling from the collectors of transistors 71, 101, and 106 to the resistor 94 which is connected to the output line 24. Similarly, capacitor 96 couples the collectors of transistors 72, 111, and 116 to the resistor 97 which is connected to the output line 24. These capacitors provide DC isolation between the driver amplifier and the output buffers. The combining of the signals at the junction 98 between resistors 94 and 97 again provides a minimizing effect to distortion products. These resistors 94 and 97 are relatively small compared to resistors 78 and 81 and are

chosen to balance the gain through the upper and lower sections of the amplifier to obtain maximum cancellation of distortion products.

The high input impedance of the two complementary emitter followers in the output buffers allows paralleling of the five output channels to the driver amplifier. The output impedance is matched to the required 75 ohms load. The matching of a PNP transistor with an NPN transistor gives an additional advantage in distortion cancellation.

The grouping of the circuits for a single five channel module as shown in FIG. 5 can be accomplished by containing the six individual circuits in a honeycombed chassis that provides interchannel isolation and a very rugged construction. The module input impedance is approximately 300 ohms and each channel has a nominal 75 ohm output impedance.

As shown in FIG. 4, four of the modules can be combined to make up a 20 channel multicoupler. A terminating resistor at the input provides the required nominal 75 ohms input impedance if less than four modules are used in the multicoupler. This can be accomplished by connecting a 300 ohm resistor between ground and the input line 12d, for example, if module 16 were not included. However, because this may be inconvenient and because it can be inconvenient to parallel coaxial cable from the antenna into four driver amplifiers, there is a preferred embodiment of the invention, which will now be described.

The preferred embodiment is shown in FIGS. 1, 2, and 3. Referring particularly to FIG. 1, the high frequency input signals are derived from the antenna 11 which is coupled to a driver section which may be conveniently incorporated in a single module 131. In the driver section is a driver amplifier 132 whose input is received directly from the antenna 11 although input band pass filters may be employed if desired. Four complementary emitter followers 133, 134, 136 and 137 have inputs coupled to the driver amplifier.

The output of each of the complementary emitter followers may be coupled to five output channel buffers in parallel, each of which has a receiver coupled to its output. The channel buffers and receivers are shown connected to only one of the complementary emitter followers, namely 133, in order to conserve space in the drawing. As illustrated, the output line 138 of the emitter follower 133 is connected to parallel inputs 139, 141, 142, 143, and 144 to the channel buffers 146, 147, 148, 149, and 151 respectively. It is quite convenient to include all five of these channel buffers in a single module 152. Each of the channel buffers thus provides an output to which a receiver can be connected, the receiver 153 being connected to the output of the channel buffer 146, for example. By coupling an identical channel buffer module to each of the remaining complementary emitter followers 134, 136, and 137, an additional fifteen receiver output channels can be readily provided.

Referring now to FIG. 2 which shows the driver section in schematic, and for which voltage and component values will be given for purposes of example, a 10 volt positive direct current supply potential is provided at terminal 154 and a negative 10 volt direct current supply potential is provided at terminal 156. Grounded shielding may be employed as indicated and suitable signal decoupling for the four supply lines 157, 158, 159, and 161 is provided by the use of inductors 162 in series and capacitors 163 connected to ground 164. All four lines 157, 158, 159, and 161 are provided with identical decoupling means.

The antenna signal input 12 is coupled through the capacitor 166 to the base electrodes of the complementary amplifier 132. This amplifier is quite similar in overall construction to that previously described with reference to FIG. 7, and corresponding parts have been given reference numerals identical to those used in FIG. 7.

The positive direct current supply to the collector load resistor 78 is obtained from the positive supply terminal 154 through the decoupling means and line 157. The positive direct current supply potential for the emitters of the transistors 72, 111, and 116 is also obtained from the terminal 154 through the decoupling network and line 158. The negative direct current potential supply to the emitters of transistors 71, 101, and 106 is obtained from the negative direct current supply terminal 156 through the decoupling network and line 159. The negative direct current supply potential for the collector load resistor 81 is obtained from the negative terminal 156 through the decoupling network and line 161.

In this embodiment, only one coupling capacitor 166 is provided between the input line 12 and the base electrodes of all six of the transistors. Also, only one terminating resistor, 168, is provided. Its value is selected according to the same novel concept as the selection of resistors 73 and 74 was made for the embodiment of FIG. 7 so that the input impedance of the complementary amplifier will be quite stable over the range of input operating frequencies. Thus, the frequency effects on transistors which might otherwise affect the input impedance can be practically eliminated.

The values of collector load resistors 78 and 81 are made low so that the distributed capacity of the circuit and transistors would not cause objectionable fall off of response at the higher frequencies approaching 60 mc.

As in the previously described complementary amplifier of FIG. 7, values of resistors 84 and 87 and the corresponding resistors for the parallel transistors are selected to provide a sufficient emitter degeneration to give a transistor signal input circuit impedance which is high as compared to the desired multicoupler input impedance. The latter is thereby established principally by resistor 168. By proper selection of resistors 86 and 88 along with 84 and 87, the desired quiescent currents are obtained. In this way, the desired dynamic range without distortion is obtained. For the transistors used, 150 ohm values for resistors 84 and 87 provide this.

The three transistors in parallel in the upper and lower amplifier portions provide the desired 9 db unloaded gain for the amplifier. They also provide a good noise figure.

Four complementary emitter followers are coupled to the complementary amplifier. However, in contrast to the coupling previously described with reference to the earlier embodiment, the outputs of the upper and lower portions of the complementary amplifier in this preferred embodiment are not connected together before coupling to the emitter followers. For example, in the complementary emitter follower stage 133, we have transistors 168 and 169 in complementary symmetry. The collector output signal from transistors 71, 101, and 106 of the complementary amplifier 132 is coupled through the capacitor 171 and resistor 172 to the base electrode of transistor 168. A resistor 173 is coupled between ground and the junction of the capacitor 171 and resistor 172.

Similarly, the collectors of transistors 72, 111, and 116 of the complementary amplifier are coupled through the capacitor 174 and resistor 176 to the base electrode of transistor 169. A resistor 177 is coupled between ground and the junction of capacitor 174 and resistor 176. The selection of the resistors 173 and 177 is such that the value thereof is high enough not to affect the gain of the complementary amplifier. The capacitors 171 and 174 provide the necessary signal coupling while providing direct current isolation. The resistors 172 and 176 are provided to avoid parasitic oscillations. Similar resistors are provided for all of the emitter followers in the driver section 131.

Referring more specifically to the emitter follower 133, the decoupling resistor 178 is connected to the negative direct current supply line 161. A capacitor 179 is provided between ground and the junction of the said resistor 178 and the collector of transistor 168.

Resistors 181 and 182 are connected in series between

the emitter electrode and the positive supply line 158. The bypass capacitor 183 is connected between ground and the junction between resistors 181 and 182.

Similarly, the decoupling resistor 184 of transistor 169 is connected to the positive supply line 157. The capacitor 186 is connected between ground and the collector of transistor 169. Resistors 187 and 188 are connected in series between the emitter of transistor 169 and the negative supply line 159. A bypass capacitor 189 is connected between ground and the junction between resistors 187 and 188.

The single output line 138 from the complementary emitter follower 133 is coupled to the emitter of transistor 168 through the resistor 191 and DC blocking capacitor 192. Similarly, this single output line 138 is coupled to the emitter of transistor 169 through the resistance 193 and DC blocking capacitor 194. Accordingly, at the output 138, we are able to provide cancellation of distortion products. The remaining three emitter followers stages are identical to stage 133 and have parallel inputs. The selection of the resistors 187 and 188 in the emitters of these emitter followers can be made without attention to output impedance requirements of the multicoupler.

Referring now to FIG. 3, which is a schematic diagram of the channel buffers used throughout the preferred embodiment of the multicoupler, it will be considered for purposes of example that this is the channel buffer 146 of FIG. 1 having the input 139 which is coupled to the output 138 of the emitter follower 133. This channel buffer includes three NPN transistors 196, 197, and 198 employed in emitter follower arrangement. A 10 volt positive direct current potential may be supplied at the terminal 154 which may be the same supply as that for the complementary amplifier. Similarly, the negative 10 volt direct current supply is provided at terminal 156. Decoupling is provided by the inductors 162 and capacitors 163, with the latter being connected to ground in the same manner as was employed in the complementary amplifier.

The collector of the transistor 196 is coupled through the resistor 199 to the positive direct current supply while the emitter is coupled through the resistors 201 and 202 in series to the negative supply. A bypass capacitor 203 is connected between ground and the junction of resistors 201 and 202. Resistor 206 is connected between the signal input line 141 and the base electrode of transistor 196. Resistor 207 is connected between ground and the input line 141.

The emitter output of transistor 196 is coupled through resistor 208 to the base electrode of the transistor 197. It is also coupled through resistor 209 to the base electrode of transistor 198. The collector electrode of transistor 197 is coupled through resistor 211 to the terminal 154 while the emitter electrode is coupled through resistance 212 to the negative supply at terminal 156.

The collector electrode of transistor 198 is coupled through resistor 213 to the positive direct current supply whereas the emitter electrode is coupled through resistor 214 to the negative direct current supply. A capacitor 216 is coupled between ground and the collector of transistor 197 whereas a capacitor 217 is connected between ground and the collector of transistor 198.

The output from the emitter follower transistor 197 is coupled through capacitor 218 and resistor 219 to the junction 221. The output from the emitter of transistor 198 is coupled through capacitor 222 and resistor 223 also to the junction 221. The junction 221 feeds a single output 224 providing the input to the receiver 153 of the FIG. 1. The necessary output impedance for matching to the receiver is provided by suitable selection of the resistors 219 and 223. One percent resistors are preferable in these locations. The emitter resistors 212 and 214 for transistors 197 and 198 are selected to establish the necessary combination of AC load current requirement and

operating range in the channel buffer. This channel buffer has extreme linearity.

This preferred embodiment of the invention represents an improvement over the previously described embodiment in several respects. It eliminates any necessity for paralleling antenna inputs to driver amplifiers. Addition or subtraction of groups of five buffers will not affect those which are already connected. Therefore, by using the appropriate number of channel buffers, it is possible to employ practically any number of receivers up to twenty with the single driver amplifier and four complementary emitter followers without necessity of variation in component values to compensate for the variation in number of receivers. Furthermore, the inclusion of the four emitter followers and driver amplifier in one module and five channel buffers in a separate module, facilitates the addition of receivers five at a time, if desired, still without affecting the first module. Finally, the use of only one driver section and only three NPN transistors in each channel buffer results in a cost saving in the type and number of transistors used.

Examples of component values for the preferred embodiment are as follows, the reference numerals being used in most instances to identify the components:

25	PNP transistors -----	2N1143
	NPN transistors 196, 197, 198 -----	2N706
	NPN transistors—all except 196, 197, 198 ----	2N744
	All capacitors -----microfarads--	0.1
	All inductors -----microhenries--	10
30	Resistor 168 -----ohms--	75
	Resistors 78, 81, 84, 87, 102, 107, 112, 117, 178, 184 -----do-----	150
	Resistors 86, 88, 103, 108, 113, 118 -----do-----	910
	Resistors 173, 177 -----do-----	2000
35	Resistors 172, 176, 191, 193 -----do-----	39
	Resistors 181, 187 -----do-----	560
	Resistor 207 -----do-----	750
	Resistor 206 -----do-----	47
40	Resistors 208, 209 -----do-----	75
	Resistors 201, 212, 214 -----do-----	430
	Resistor 202 -----do-----	620
	Resistor 199 -----do-----	390
	Resistors 211, 213 -----do-----	200
	Resistors 219, 223 -----do-----	140
45	Resistors 188, 182 -----do-----	100

Because of the small size, low weight, low power consumption, and versatility of the multicoupler of the present invention, it is ideal field equipment. It possesses electrical characteristics desired in multicouplers. It lends itself to a most convenient and versatile modular construction. Even with its minimal size, weight, and power consumption, it provides many available outputs to which receivers can be readily connected and disconnected without affecting other receivers attached to other outputs. More outputs can be added as the problem expands.

The multicoupler of the present invention can be constructed using transistors normally considered to be of the small signal type to handle a frequency range from 100 kc. to 60 mc. Moreover, while antenna input signals to a receiver are normally below the 10 millivolt level, they can be as strong as 0.25 volt where a frequency range from 100 kc. to 60 mc. is used. The present invention can handle antenna inputs at this level.

While the invention has been disclosed and described in some detail in the drawings and foregoing description, they are to be considered as illustrative and not restrictive in character, as other modifications may readily suggest themselves to persons skilled in this art and within the broad scope of the invention, reference being had to the appended claims.

The invention claimed is:

1. A combination comprising: antenna means; a plurality of radio frequency energy receivers; means coupling said antenna means to said receivers and including

a driver amplifier having an input coupled to said antenna means and having an output, and output buffers, each of said output buffers having an input coupled to said driver amplifier output and having an output coupled to one of said receivers; a source of direct current electrical energy provided at first, second and third terminals, with the relative potentials of said first, second and third terminals being positive, zero, and negative, respectively; said driver amplifier including a first transistor, said first transistor being an NPN transistor having a collector electrode connected through first resistance means to said positive terminal and having an emitter connected through second resistance means to said negative terminal, and a second transistor, said second transistor being a PNP transistor having a collector electrode connected through third resistance means to said negative terminal and having an emitter electrode connected through fourth resistance means to said positive terminal, the base electrodes of both of said transistors being coupled to said amplifier input, with a fifth resistance connected between said second terminal and said base electrodes and providing impedance matching substantially independent of frequency effects on said transistors over a wide range of frequencies at said amplifier input.

2. A combination comprising: antenna means; a plurality of radio frequency energy receivers; means coupling said antenna means to said receivers and including a driver amplifier having an input coupled to said antenna means and having an output, and output buffers, each of said output buffers having an input coupled to said driver amplifier output and having an output coupled to one of said receivers; a source of direct current electrical energy provided at first, second and third terminals, with the relative direct current potentials of said first, second and third terminals being positive, zero, and negative, respectively; said driver amplifier including a first transistor, said first transistor being an NPN transistor having a collector electrode connected through first resistance means to said positive terminal and having an emitter connected through second resistance means to said negative terminal, and a second transistor, said second transistor being a PNP transistor having a collector electrode connected through third resistance means to said negative terminal and having an emitter electrode connected through fourth resistance means to said positive terminal, the base electrodes of both of said transistors being coupled to said amplifier input, with a fifth resistance connected between said second terminal and said base electrodes and providing impedance matching substantially independent of frequency effects on said transistors over a wide range of frequencies at said amplifier input, and means including a sixth resistance coupling the collector electrode of said first transistor to said driver amplifier output means and including a seventh resistance coupling the collector electrode of said second transistor to said driver amplifier output means, the said sixth and seventh resistances being of values which are small compared to the said first and third resistances between said collector electrodes and said direct current potential terminals, and thereby balancing the gain through said transistors to obtain maximum cancellation of distortion products.

3. A high frequency band antenna multicoupler for providing signals for a plurality of receivers from a single

antenna and comprising: Class A complementary amplifier means having input means for coupling to an antenna, and having output means; Class A complementary emitter follower means having input means coupled to the output means of said amplifier means and having a single ended output; and output circuit means comprising a first emitter follower having a control electrode coupled to said single ended output and having an output, second and third emitter followers, each having a control electrode coupled to said output of said first emitter follower and each having an output, the signal outputs of said second and third emitter followers being resistively coupled together to provide a single ended output for connection to a receiver.

4. A combination comprising: an antenna; and a multicoupler having Class A complementary amplifier means with signal input means coupled to said antenna, said amplifier means having a number of parallel connected PNP transistors and a like number of parallel connected NPN transistors with the control electrodes of said transistors connected to said input means, said input means including resistance means establishing an amplifier input impedance matching the impedance of said antenna and substantially unaffected by input signal frequency changes, a plurality of Class A complementary emitter follower means having parallel connected input means coupled to the said transistors, each of said complementary emitter follower means having a single ended output, and a plurality of output circuit means coupled to each of said outputs, each of said output circuit means including a first emitter follower having a control electrode coupled to one of said single ended outputs, and each said output circuit means having second and third emitter followers with the control electrodes thereof coupled to said first emitter follower to receive signals therefrom, each of said second and third emitter followers having an output, and each of said output circuit means having a single ended output for a receiver and coupled through a first resistance means to the output of said second emitter follower and coupled through a second resistance means to the output of said third emitter follower.

5. In an antenna multicoupler, the combination comprising: a first emitter follower having a control electrode for signal input; second and third emitter followers having parallel signal inputs, each having a control electrode receiving a signal input from an emitter of said first emitter follower; a single ended output; a first resistance means coupled between said single ended output, and the emitter of said second emitter follower; and a second resistance means coupled between said single ended output and the emitter of said third emitter follower, said first and second resistance means establishing an output impedance to match the input impedance of a receiver to be coupled to said output.

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