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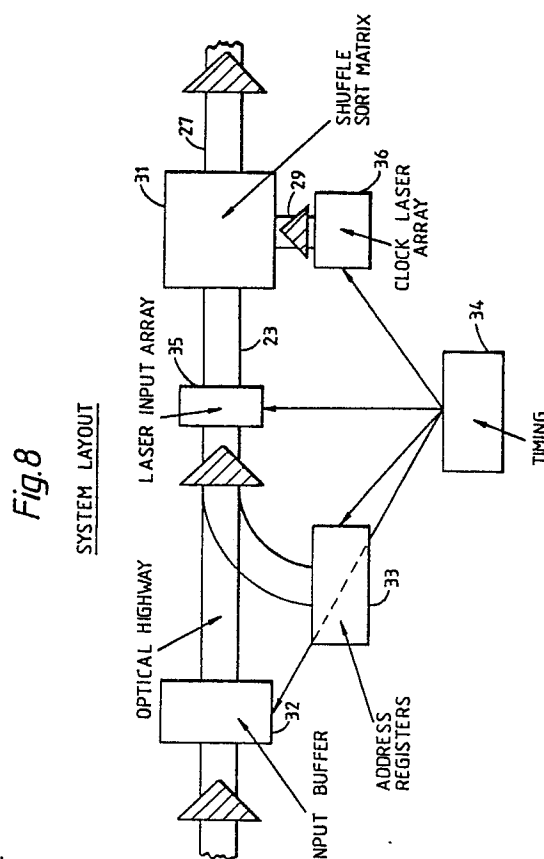
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54 Improvements relating to pipeline sort matrices.

57 A signal switching assembly comprises a pipeline sort matrix having a plurality (N) of input and output ports. A number of signal switching units are arranged in series between the input and output ports, the input ports being coupled with an upstream signal switching unit (7) and the output ports being coupled with a downstream signal switching unit. The switching units are coupled together so as to be able to perform a perfect shuffle algorithm or a group of output port addresses supplied to the input ports during a reset operation. The pipeline sort matrix is controlled by a control system (33,34,35,36) which generates selection signals which are supplied to each signal switching unit to reset the status of the signal switching unit so that after the status of each signal switching unit has been reset, selected input and output ports are coupled together. The control system is adapted to reset each signal switching unit in turn.



IMPROVEMENTS RELATING TO PIPELINE SORT MATRICES

The invention relates to pipeline sort matrices and signal switching assemblies incorporating such matrices.

Most proposals for optical switches to date have been based upon arrays of electrically controlled Exchange-Bypass Modules (EBM) optically wired to form some form of switching matrix. Such EBMs might be formed from Lithium Niobate Directional Couplers, active fibre couplers, mechanically operated fibre switches or a variety of other possibilities. Simple $N \times N$ cross points have been described and fabricated for small arrays, up to perhaps 16×16 , but the fabrication complexity escalates rapidly as the number of ports, N , increases. Such matrices have the attractive property that they are bi-directional and data transparent so that bidirectional communication can be carried on through them with arbitrary and variable bit-rate and data format. However, the problems of wiring large matrices to obtain low insertion loss and cross talk and the variability of insertion loss with path suggest that this is not a viable route for large switches. In addition, the bidirectional characteristics of such switches are of limited value in full $N \times N$ cross points since these are fundamentally two sided, implying the use of separate inward and outward channels.

The need to make large arrays has thus focussed some attention on the more efficient single sided networks (A.M.Hill, "One sided re-arrangeable optical switching networks", IEEE. Journal Lightwave Tech. Vol.LT-4, pp.785-789, (1986)) in which the number of cross points is greatly reduced in order to serve N ports and in which the bidirectional characteristics can be more fully exploited. Dramatic simplifications are possible in principle. However, these are gained at a price, notably that resetting any pair of input-output connections entails resetting many cross points, some of which will normally be actively carrying data. This poses its own special problems.

A new type of switching network has recently been proposed. This involves the use of a pipeline sort matrix of the kind having a plurality of input and output ports, and a number of signal switching units arranged in series between the input and output ports, the input ports being coupled with an upstream signal switching unit and the output ports being coupled with a downstream signal switching unit, whereby the status of each signal switching unit is reset by supplying selection signals to the signal switching units so that after the status of each signal switching unit has been selected, selected input and output ports are coupled together. Such matrices are hereinafter referred to as of the

kind described.

An example of a pipeline sort matrix of the kind described is described in "Light Electronics, Myth or Reality", IEE Proceedings Vol.132, Pt.J, pp.371-383, (1985). In this matrix, the signal switching units are coupled together using optics although in theory other forms of connection such as optical fibres could be used.

In this specification, the term "pipeline sort matrix", is taken to refer to any matrix which is configured to define a sort algorithm in a pipeline or staged format.

The need to reroute paths whilst data is being carried seems to imply one of two operating conditions. The paths must be completely reset in a time that is short compared to one bit interval and with a change in time delay that is equally short, or it must be reset synchronously in the inter-bit interval. For high speed data, it is very hard to see how the latter could be done at all with bidirectional communication since the optical path through the matrix is likely to take longer than one bit interval. Moreover, it also presupposes that the data lines are all synchronous and hence formatted to similar mean bit rate, even if that is only done by bit-padding. The former option seems to imply ultra-fast resetting, given again that we are only interested in handling high speed data.

In accordance with one aspect of the present invention, a method of resetting a pipeline sort matrix of the kind described comprises resetting each signal switching unit in turn.

In accordance with a second aspect of the present invention, a signal switching assembly comprises a pipeline sort matrix of the kind described; and control means for controlling operation of the pipeline sort matrix, the control means generating the selection signals which are supplied to each signal switching unit to reset the status of the signal switching unit, the control means being adapted to reset each signal switching unit in turn.

We have recognised that it is possible to reset a pipeline sort matrix in stages by resetting each signal switching unit in turn. This minimises the effect of the resetting procedure on the transmission of signals through the matrix and thus enables very high speed switching to be achieved.

Although the invention could be applied to a variety of different forms of signal, it is particularly applicable to optical pipeline sort matrices.

Typically, the matrix will have N input ports and N output ports, the signal switching units being capable of connecting the input and output ports in any configuration.

The invention is particularly suitable however,

to pipeline sort matrices which perform a perfect shuffle sort algorithm.

To reset the matrix, some form of reset signal might be injected to each signal switching unit. Preferably, however, since in general, pipeline sort matrices require clock signals to be supplied to each signal switching unit to control the passage of signals in a pipeline manner through the matrix, it is convenient to define the commencement of a reset period for each signal switching unit by suppressing the clock signal normally fed to that unit. Conveniently, during resetting of the upstream signal switching unit, the supply of signals to the input ports of the matrix is inhibited, the supply being restarted after resetting of the upstream signal switching unit is completed.

Although the status of each signal switching unit could be set by an external selection signal, it is preferable if the selection signals are fed to the input ports of each signal switching unit upstream of the signals to be switched. For example, the selection signals could be in the form of matrix output port addresses.

This latter technique is particularly suitable where the signal switching units comprise EBM's which respond to the address signals to cause subsequent signals to pass straight through the module (bypass) between the first input and output ports and the second input and output ports respectively or to switch (exchange).

An example of a signal switching assembly incorporating a pipeline sort matrix and a method of resetting the matrix in accordance with the present invention will now be described with reference to the accompanying drawings, in which:-

Figure 1 illustrates an example of an exchange-bypass module (EBM) and its truth table;

Figure 2 illustrates in diagrammatic form a generalised pipeline sort processor;

Figure 3a is a logical diagram for a self-setting EBM, and Figure 3b is the associated Truth Table;

Figure 4 illustrates the three types of EBM required to form a complete switching matrix;

Figure 5 illustrates the logical layout of EBM's for a perfect shuffle sort algorithm;

Figure 6 is a schematic diagram of a reflective, folded perfect shuffle processor;

Figures 7A, 7B, and 7C are a partial section, a perspective view, and a plan respectively of part of the input/output and control subsystem for the processor of Figure 6;

Figure 8 is a block diagram of the overall control system for the processor; and,

Figure 9 is a block diagram of an exchange/bypass module fabricated on a semiconductor chip.

The signal switching assembly or processor to

be described includes a pipeline sort matrix formed from a number of groups of exchange/bypass modules (EBM's). An example of the logical construction of an EBM is shown in Figure 1 and comprises four AND gates 1-4 whose outputs are coupled to respective inputs of a pair of OR gates 5, 6. The EBM has two input ports A, B connected to the AND gates 1, 2; 3,4 respectively and two output ports D, E connected to the OR gates 5, 6 respectively. The output ports of the AND gates 1, 3 are connected to the input ports of the OR gate 5 while the output ports of the AND gates 2, 4 are connected to the input ports of the OR gate 6.

The status of the EBM is set by a control signal C fed to the AND gates 1, 4 and its logical complement $\bar{C}$ fed to the AND gates 2,3.

As can be seen from the Truth Table in Figure 1, the EBM is set in its bypass state when the control signal C is logical 1 resulting in a signal on the input port A being passed to the output port D and a signal on the input port B being passed to the output port E. When the control signal C is logical zero, the EBM is in its exchange state in which the signal on input port A is coupled with the output port E and the signal on input port B is coupled with output port D.

Figure 2 illustrates a generalised sort processor having N input ports and N output ports. The input ports are connected in pairs to respective EBM's of a first group 7 whose output ports are connected to a redistribution network 8. The redistribution network has a fixed pattern and couples each input line with a respective output line. As can be seen in Figure 2, this generalised sort processor comprises a number of pairs of EBM groups and redistribution networks together with a final group of EBM's 9 connected to the output ports of the processor.

In this example, we propose that the redistribution networks should be arranged such that the matrix performs a perfect shuffle algorithm. This is particularly suitable for optical signal implementation since each redistribution network has an identical form and so can be fabricated by a common network.

The use of the perfect shuffle for sorting was first described many years ago. For a matrix having N input ports where $M = \log(N)$ and log is to base 2, a first cut design requires $M \times M$ rows each of N/2 EBM's between the N input and N output ports with perfect shuffle interconnects between each row. These involve three types of logical EBM shown in Figure 4. By the terminology "logical EBM", we imply a module that includes the logic to establish whether it should self set to the exchange or bypass state according to the address data presented to it through its input ports. The "0" module always bypasses whilst the "+" and "-" modules always route the larger of the two ad-

dresses (numbers) to the port marked "h". They are thus logically identical in structure but are mirror images in function.

Figure 5 shows the logical layout for a full 32×32 matrix using the perfect shuffle sort algorithm for its self addressing function. Here $N = 32$ and $M = 5$. The layout has been deliberately split into five groups of five rows, with each row containing 16 modules. The data lines emerging from each row of 16 EBM's are perfect shuffled before entering the next row. After the first five rows, (ie. at the output of row five), the input data has been sorted into 8 bitonic sequences, with the adjacent pairs of inputs reversed or not according to the address size and spatial position. After the succeeding groups of five rows, the addresses have been sorted into 4 bitonic sequences, 2, 1 and finally into a linearly ascending sequence at row 25.

The result of this wiring pattern is that after every block of M EBM's, the address data has been bitonically sorted, initially into $N/4$ sequences and then by factors of two into ever larger sequences. However, it also emerges that the first $M-1$ rows of "0" EBM's can be completely discarded without altering the overall operation of the matrix. Accordingly, we only need $M(M-1)+1$ rows of EBM's to implement the matrix. Moreover, of these, $1+2+\dots+(M-2) = (M-1)(M-2)/2$ are entirely composed of "0" EBM's and thus play no active role in the sort. Accordingly, we find the following results:-

Total number of EBM nodes = $(N/2) \cdot (M(M-1) + 1)$

Total number of shuffles = $M(M-1)$

Number of active EBM nodes = $(N/4)M(M-1)$

For the case of 128 input ports, $M=7$, and these evaluate to 2752, 42 and 1344 respectively.

The optical implementation of the perfect shuffle wiring between each row is described below.

It should be noted that a perfect shuffle of the numbers from 1 to N simply involves two operations. In the first, they are split into two equal sequences, 1 to $N/2$ and $N/2 + 1$ to N . Setting $N/2 = P$ for ease of writing, in the second operation these are interleaved to form the sequence:-

1, $P+1$, 2, $P+2$, 3, $P+3$, ..., $N/2, N$

The fact that this is readily done optically with zero time skew in two dimensions is a major attraction since it allows one to monolithically integrate all the logical EBM's onto a single chip and to use a single optical system to provide all the interconnects in parallel through space normal to the chip.

The setting of each EBM is determined by address data supplied to each input port of the matrix. This address data defines the matrix output port to which subsequent signals are to be switched. The use of logical EBM's is particularly advantageous in this connection since they re-

spond to the relative size of the two addresses arriving at each input port of the respective pair (see Truth Table of Figure 3B). The only action required on the EBM is always to deliver the larger number to the same defined (by position) exit port. Such a logical operation on binary MSB first addresses is trivial, since identical bits always pass directly through. The first pair of bits in the address to differ then define uniquely the larger of the two numbers.

Figure 3a illustrates the overall logical circuit for an EBM where I_1 , I_2 , O_1 , O_2 are the input ports and output ports respectively; R indicates a reset signal; and P , Q indicate control inputs and outputs for latching the EBM in one of its two states.

An example of the full Truth Table for the EBM of Figure 3a is shown in Figure 3b.

If the status of the EBM is set or selected then the reset signal R will be logical 1 and the signals P , Q will define whether the state is bypass, exchange, or not yet set. When $R=0$, the device is in reset mode, as illustrated in Figure 3b. Consider for example line 15 of the Truth Table where $Q(n-1) = 1$ and $P(n-1) = 0$. This corresponds to the exchange state and it will be seen that the signal on port I_1 has been switched to port O_2 and the signal received at port I_2 has been switched to port O_1 .

If the status of the EBM is to be reset, the reset signal is switched to zero causing $Q(n)$ and $P(n)$ to be zeroed thus implying that the EBM is thereafter not set and preparing the EBM to be set once the reset signal returns to logical 1. Upon this return, the EBM will treat the next data received on its input ports I_1 , I_2 as address or setting data. For example, consider line 13 in the Truth Table where $Q(n-1)$ and $P(n-1)$ are both zero implying that the EBM is not set. Since $R=1$, the data on input ports I_1 , I_2 is treated as setting data which in this case sets the EBM in the exchange mode and also exchanges that address data.

The reset operation will be explained in more detail in due course.

Figures 6 to 9 illustrate a practical implementation of a perfect shuffle sort matrix of the type shown in Figure 2.

Each group of EBM's is fabricated in a manner to be described below into a logic array 10 (Figure 6) comprising a number of rows of EBM's, each row corresponding to one group (such as the group 7 in Figure 2). In the case of the perfect shuffle algorithm, each redistribution network has an identical form and in this example is defined optically by a lens system 11. As in previous implementations, this shuffle optics relies upon the concept of magnifying an image laterally by a factor of 2, shearing the image into two, and overlaying the two halves to form a shuffled image. It also has some

additional advantages not previously achieved since it allows the whole optical system to be folded into a compact sub unit embracing the return data path to the array. It also brings together all the input/output and control channels in a single port 12 located opposite the logic array 10.

The logic array 10 is fabricated on a single chip of for example GaInAs/InP with a band gap in the 1300-1500 nm region. The array comprises a number of MQW electro-absorption modulators (EAM), two for each EBM, each of which can be addressed by an externally generated "read" laser beam.

An example of one EBM within the logic array is shown in Figure 9. This comprises a pair of photodetectors 13,14 formed, for example, from electro-absorption modulators. The electronic output signals from these photodetectors 13, 14 are fed to respective gain and thresholding circuits 15 whose outputs are fed to an EBM logic circuit 16. A photodetector 17 also formed from an electro-absorption modulator is responsive to a clock laser beam to provide clock signals to the EBM logic circuit 16. The electronic output signals from the EBM logic circuit 16 are fed to respective EAM drivers 18, 19 which drive respective electro-absorption modulators 20, 21. An external read beam is supplied to each EAM 20, 21 which modulates the beam to generate the required output signal.

The arrangement of Figure 9 is particularly useful for a number of reasons. Firstly, the optical source of the "read" beam can be located away from the active chip and can thus dissipate its heat elsewhere. This has a secondary, but important advantage, that this enables the beam also to be used for timing and control purposes. Secondly, by externally addressing the modulators, the exit beam direction can be derived from the input. This is highly desirable in order to implement the shuffle wiring scheme. Thirdly, EAMs are known to be inherently fast (sub 100 ps switching speed), are readily fabricated and lend themselves to monolithic integration. They are also (optically) non-resonant so that they are relatively insensitive to temperature and wavelength.

The input/output system positioned at the port 12 in Figure 6 is illustrated in detail in Figure 7. At the input port 12 is positioned a composite, layered I/O structure 22 shown in detail in Figure 7A. This comprises the output end of an input fibre array 23 composed of a number of optical fibres, one for each input port of the matrix, as a top layer followed by alternate layers of microlenses 24 and reflectors 25, there being one pair of layers 24, 25 corresponding to each row of EBMs, and terminating with the input end 26 of an output fibre array 27. In this example, there are 128 input ports and 128 output ports with 64 EBMs in each row.

In order for the EBMs to function, it is necessary to supply three pump laser beams to each EBM. These provide the two "read" beams to the EAMs 20, 21 and the clock beam supplied to the photodetector 17. Each set of three beams is provided in this example by a respective laser the power from which is fanned out into 3 N/2 spots (N is the number of EBMs) on the associated row position on the I/O element 22 to generate three beams to each EBM. These beams are fed via the microlenses 24 associated with the respective EBM row to the logic array 10. Each laser thus provides synchronisation and interrogation for all the EBMs in a single logical row of the pipeline. The laser will be clocked with the appropriate phasing for that row position. Since all the M(M-1)+1 clock lasers can be colocated in a linear array and will require identical delays between each, it is believed that very accurate clocking should be possible. In addition, the rows enjoy zero clock skew as a result of the optical delivery system.

To examine the operation of the whole matrix, we will follow a signal through from input to output, initially ignoring the control aspects and simply assume that each EBMs exchange or bypass status is already established. Data arrives at the input ports via the input fibre array 23 and passes through the I/O structure 22 at a transparent row space. The lower half of the optical system 11 then images the signals onto the first row of 128 input photodetectors 13, 14 associated with 64 EBMs. The photodetectors 13, 14 generate corresponding electrical signals which are applied to the gain/threshold circuits 15 and then fed to the EBM logic 16 which generates appropriate signals depending on the exchange or bypass state to the drivers 18, 19. These drivers 18, 19 then control the EAMs 20, 21.

In order to read the output signals, interrogation beams from the pump source previously described are injected via the first row of microlenses 24, the interrogation beams impinging onto the logic array at different angles which will be imposed upon them by means of prisms (solid or holographic) located at the I/O element 22. The prisms are indicated by reference numeral 30 (Figure 6). The reason for this is that it is desirable to spatially separate the optical beams emerging from the two halves (1 to P and P+1 to N) of the array in order to operate the shuffle optical system with minimum power loss.

The two read beams are reflected from the respective EAMs 20, 21 after modulation and are guided by the shuffle optics 11 to impinge upon the first reflector layer 25 of the I/O element 22 to form a shuffled array of outputs at the reflector and are then imaged back to the input photodetector array of the next row of EBMs.

This sequence is then repeated for each row of EBM's with the read beams from the final row of EAM's being guided to the output fibre array 26.

Figure 8 shows a block diagram of the complete processor. At the input to the switching matrix 31, having the Figure 6 structure, a storage register, 33 is positioned which notionally uses electronic logic. In the address register 33, N registers store the desired matrix output port address associated with each matrix input port. Thus if input port 23 is to be connected to output port 56, the number 56 is stored in the 23rd address register. Within the address register 33, the complete set of addresses from 1 to N is stored. If some channels are not active, then one of the unused exit port addresses is stored in its register.

An input buffer 32 is set in the data input line to store data during the reset intervals. This need not be very large, perhaps 20 to 30 bits per input line. The processor is controlled by timing electronics 34.

To establish a global reset of the matrix the clock signal (CK) generated by a clock laser array 36 as previously described is removed (turn off the appropriate clock laser) and the EBM logic is designed so that it falls back to the reset state in the absence of the clock. Any row of the matrix can now be reset at will.

Following the reset operation, the set of N output port addresses is injected via a fibre laser input array 35 and the data path 23 in MSB first format. The EBM examines addresses entering its input ports and as soon as two address bits differ, latches to the appropriate exchange or bypass state and remains there until reset. Immediately following the address bits (7 bits), the data from the buffer 32 follows. If no data is present on a line, then we may consider that channel as remaining idle. In practice it might be necessary to inject some dummy data to limit the signal disparity in the electronic EBM stages.

A further advantage of the linear clock laser array can now be understood. Assume that the EBM logic involves (of order) 10 clock pulses from input to output. Also assume that the round trip optical path through the shuffle optics is of order 50 cms. This will take about 2ns. At a data rate of 10Gbit/s, this corresponds to 20 bits. Accordingly, we have flow delay of about 30 bits per row and about 1200 bits per matrix or about 120ns.

It would be undesirable to close down the whole matrix for a block of this order every time reset was required. Using the discrete clocks, we need only adopt the following sequence. Stop clock, pause for reset, start clock and allow to synchronise, inject 7 bits address. We might postulate this taking 20 bit intervals. The next row can then be shut down and reset using the same se-

quence but starting 30 bit intervals later. Thus the first rows of the matrix can be reset while the tail of the previous data stream is still passing through the later rows of the matrix. It was for this reason that we suggested the clock laser array be driven in a linear sequence. For the example given above, we would introduce a 30 bit delay between each laser driver for obvious reasons, delaying in particular the control/set/reset signal. It also follows from these considerations that the input data flow in a circuit switched network need only be interrupted for 20-30 bits while reset occurs and this sets in turn the size required for the input buffers.

Clearly these operations need to be under the control of the central clock 34 as shown in Figure 8. Note that although the various modules requiring accurate synchronisation appear widely distributed physically, in reality they will be clustered together very intimately in the region of the I/O structure 22 of Figure 6. Thus, it is likely that they can be packaged in a single sub-assembly, optically connected via fibre highways to the I/O element and with very intimate connection to the single control sub-system.

Claims

1. A method of resetting a pipeline sort matrix having a plurality of input and output ports, and a number of signal switching units arranged in series between the input and output ports, the input ports being coupled with an upstream signal switching unit and the output ports being coupled with a downstream signal switching unit, whereby the status of each signal switching unit is reset by supplying selection signals to the signal switching units so that after the status of each signal switching unit has been selected, selected input and output ports are coupled together, the method comprising resetting each signal switching unit in turn.

2. A method according to claim 1, wherein clock signals are supplied to each signal switching unit to control the passage of signals in a pipeline manner through the matrix, each signal switching unit being prepared for resetting by suppressing the clock signal normally fed to that unit.

3. A method according to claim 1 or claim 2, wherein during resetting of the upstream signal switching unit, the supply of signals to the input ports of the matrix is inhibited, the supply being restarted after resetting of the upstream signal switching unit is completed.

4. A method according to any of the preceding claims, wherein the pipeline sort matrix is adapted to sort optical signals.

5. A method according to any of the preceding claims, wherein the pipeline sort matrix performs a perfect shuffle sort algorithm.

6. A method of resetting a pipeline sort matrix substantially as hereinbefore described with reference to the accompanying drawings.

7. A signal switching assembly comprising a pipeline sort matrix having a plurality of input and output ports; and a number of signal switching units arranged in series between the input and output ports, the input ports being coupled with an upstream signal switching unit and the output ports being coupled with a downstream signal switching unit; and control means for controlling operation of the pipeline sort matrix, the control means generating selection signals which are supplied to each signal switching unit to reset the status of the signal switching unit so that after the status of each signal switching unit has been reset, selected input and output ports are coupled together, the control means being adapted to reset each signal switching unit in turn.

8. An assembly according to claim 8, wherein each signal switching unit comprises at least one exchange-bypass module having first and second input ports and first and second output ports, the module status being selectable such that in a first state the first input and output ports and the second input and output ports are coupled together, and in a second state the first input port is connected to the second output port and the second input port is connected to the first output port.

9. An assembly according to claim 8, wherein each module is responsive, during resetting, to matrix output port address data supplied to its input ports to set its switching state.

10. An assembly according to any of claims 7 to 9, further comprising a buffer positioned upstream of the input ports of the pipeline sort matrix, the control means being adapted to cause incoming signals to be stored in the buffer while the upstream signal switching unit is reset, and to cause the stored signals to be supplied to the upstream signal switching unit after resetting of the upstream signal switching unit is completed.

11. An assembly according to any of claims 7 to 10, wherein the control means supplies clock signals to each signal switching unit to control the passage of signals in a pipeline manner through the matrix, the control means being adapted to prepare each signal switching unit for resetting by suppressing the clock signal normally fed to that unit.

12. An assembly according to any of claims 7 to 11, wherein the pipeline sort matrix is adapted to sort optical signals.

13. An assembly according to any of claims 7 to 12, wherein the pipeline sort matrix performs a perfect shuffle sort algorithm.

14. A switching assembly substantially as hereinbefore described with reference to the accompanying drawings.

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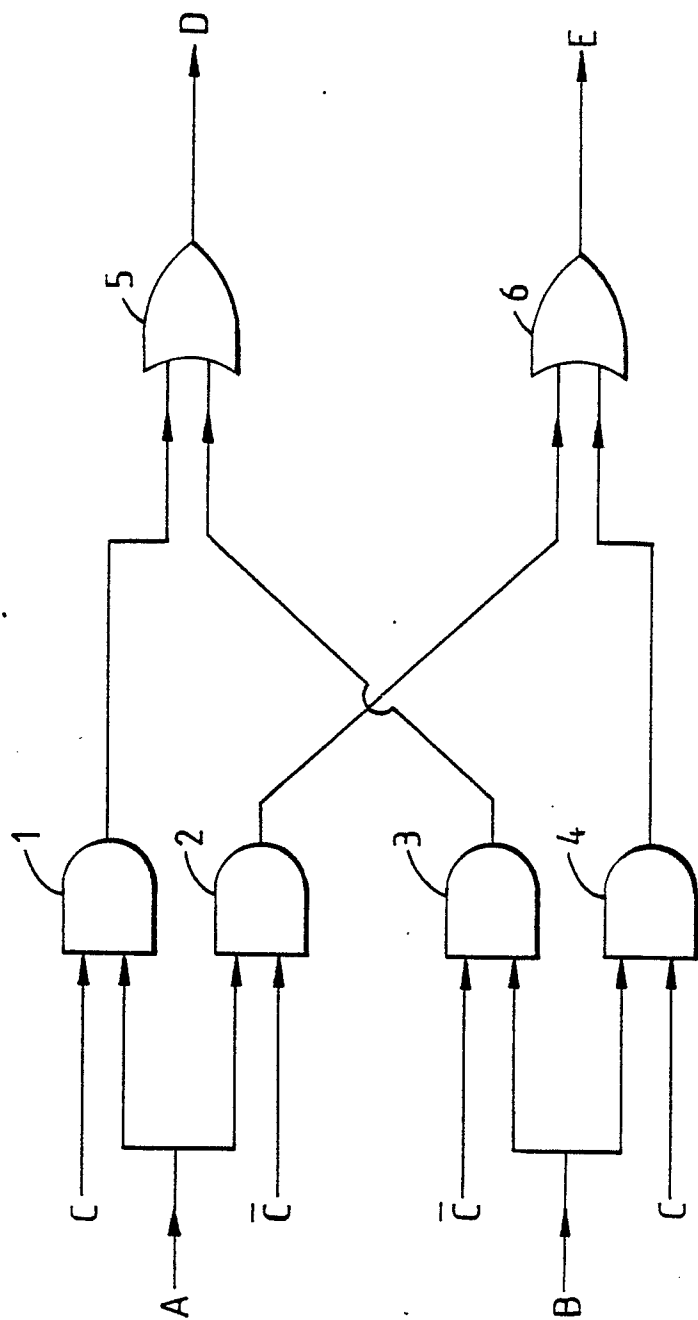
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LOGICAL EXCHANGE / BYPASS



C	$\bar{C}$	EXCHANGE	BYPASS
0	1	1	0
1	0	0	1

GAIN
UNIDIRECTIONAL
CLOCKED
(SYNCHRONOUS)

Fig.1

Fig. 2

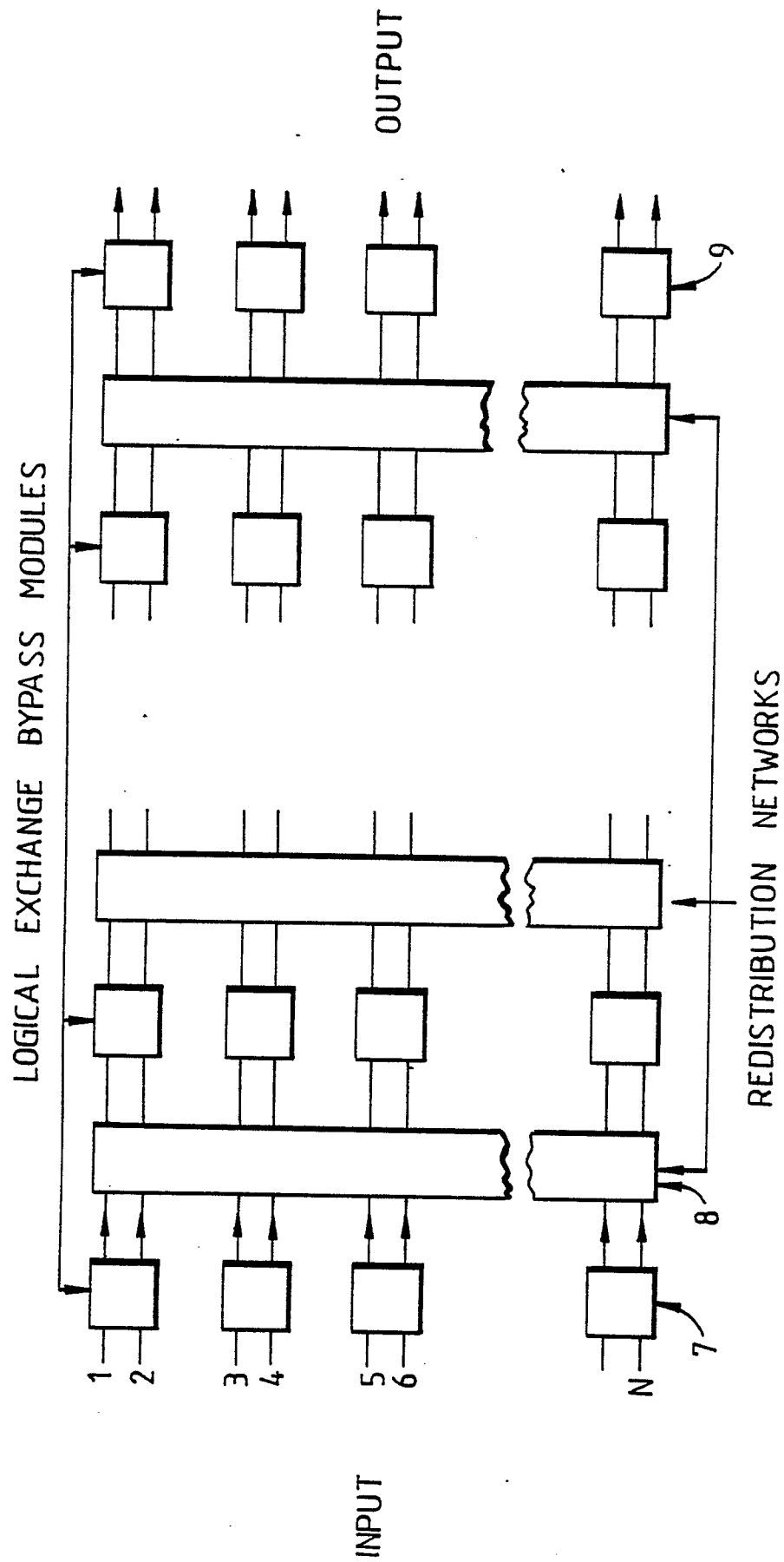


Fig. 3b

EXCHANGE-BYPASS MODULE
FULL TRUTH TABLE

I1	I2	R	Q(n-1)	P(n-1)	Q(n)	P(n)	01	02	COMMENT
0	0	0	0	0	0	0	x	x	
0	0	0	0	1	0	0	x	x	
0	0	0	1	0	0	0	x	x	
0	0	0	1	1	0	0	x	x	
0	0	1	0	0	0	0	0	0	DEFER SET, HOLD BP
0	0	1	0	1	0	1	0	0	HOLD BP
0	0	1	1	0	1	0	0	0	HOLD EX
0	0	1	1	1	0	0	0	0	DEFER SET, HOLD BP
0	1	0	0	0	0	0	x	x	
0	1	0	0	1	0	0	x	x	
0	1	0	1	0	0	0	x	x	
0	1	0	1	1	0	0	x	x	
0	1	1	0	0	1	0	1	0	SET EX
0	1	1	0	1	0	1	0	1	HOLD BP
0	1	1	1	0	1	0	1	0	HOLD EX
0	1	1	1	1	1	0	1	0	SET EX
1	0	0	0	0	0	0	x	x	
1	0	0	0	1	0	0	x	x	
1	0	0	1	0	0	0	x	x	
1	0	0	1	1	0	0	x	x	
1	0	1	0	0	0	1	1	0	SET BP
1	0	1	0	1	0	1	1	0	HOLD BP
1	0	1	1	0	1	0	0	1	HOLD EX
1	0	1	1	1	0	1	1	0	SET BP
1	1	0	0	0	0	0	x	x	
1	1	0	0	1	0	0	x	x	
1	1	0	1	0	0	0	x	x	
1	1	0	1	1	0	0	x	x	
1	1	1	0	0	0	0	1	1	DEFER SET, HOLD BP
1	1	1	0	1	0	1	1	1	HOLD BP
1	1	1	1	0	1	0	1	1	HOLD EX
1	1	1	1	1	0	0	1	1	DEFER SET, HOLD BP

NOTE - ENTRY OF "x" IMPLIES "DON'T CARE STATE"

P=Q IMPLIES NOT SET.

P=1, Q=0 IMPLIES BYPASS

P=0, Q=1 IMPLIES EXCHANGE

LOGICAL EXCHANGE - BYPASS MODULE

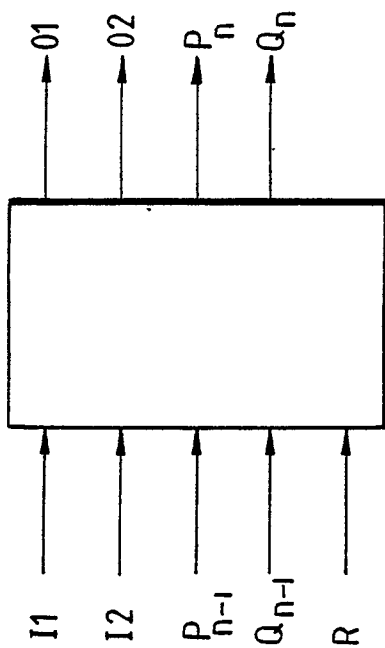


Fig. 3a

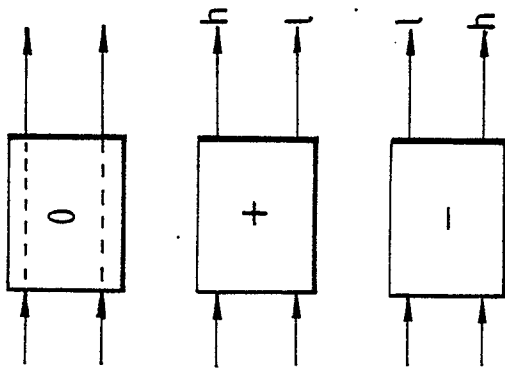


Fig. 4

IMAGE SHEARING PRISMS

Fig. 6

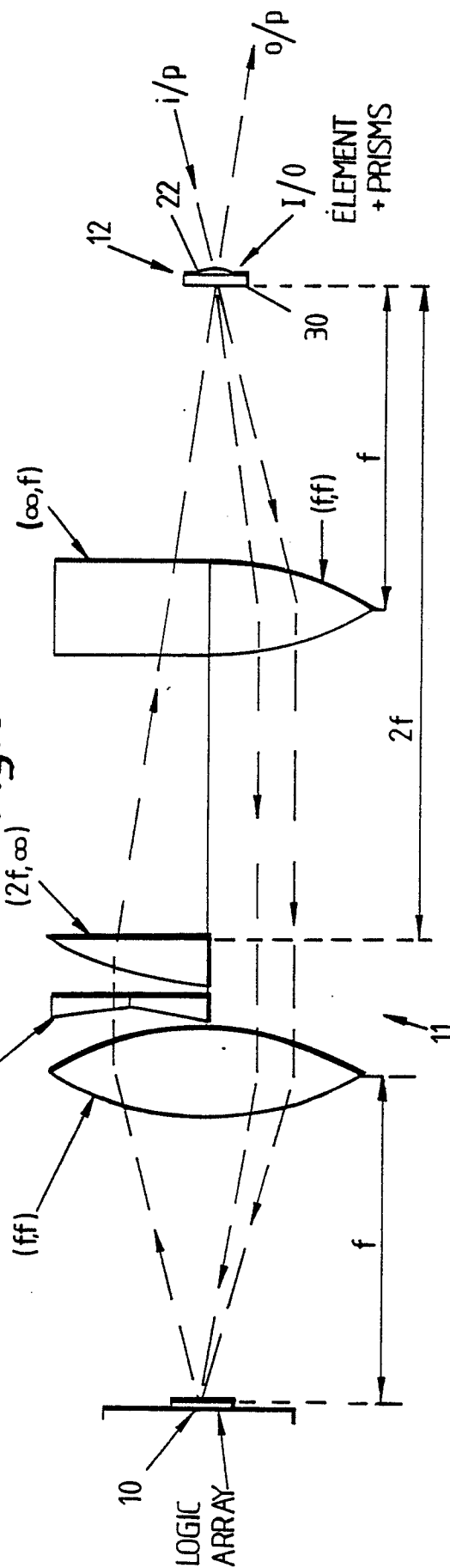


Fig.5

ROW	32 INPUT LINES															
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
10	+	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
14	+	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-
15	+	+	+	+	-	-	-	-	+	+	+	+	-	-	-	-
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	+	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
18	+	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-
19	+	+	+	+	-	-	-	-	+	+	+	+	-	-	-	-
20	+	+	+	+	+	+	+	+	-	-	-	-	-	-	-	-
21	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
22	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
23	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
24	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
25	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	32 OUTPUT LINES															

N = 32
M = 5

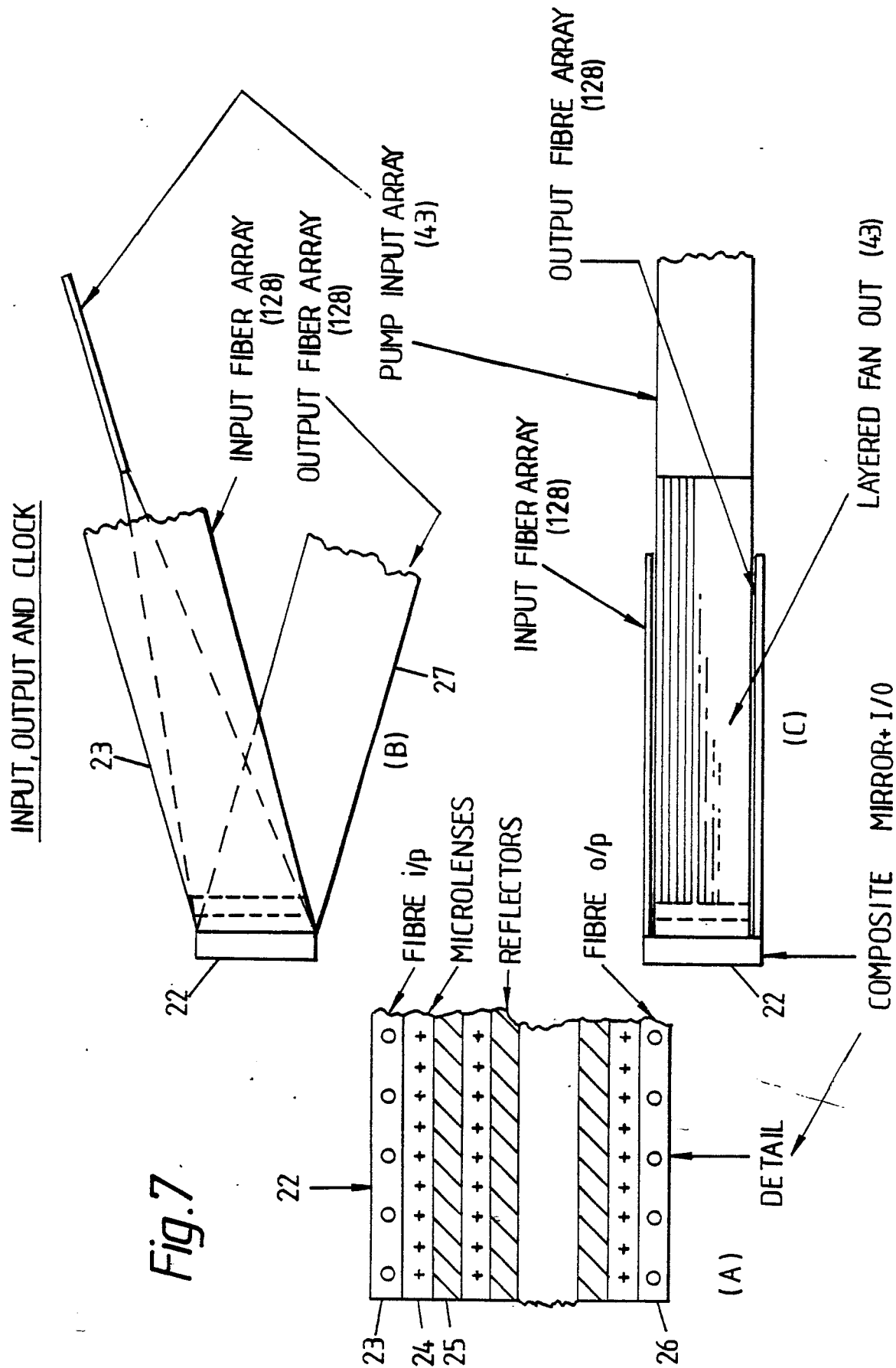


Fig. 8

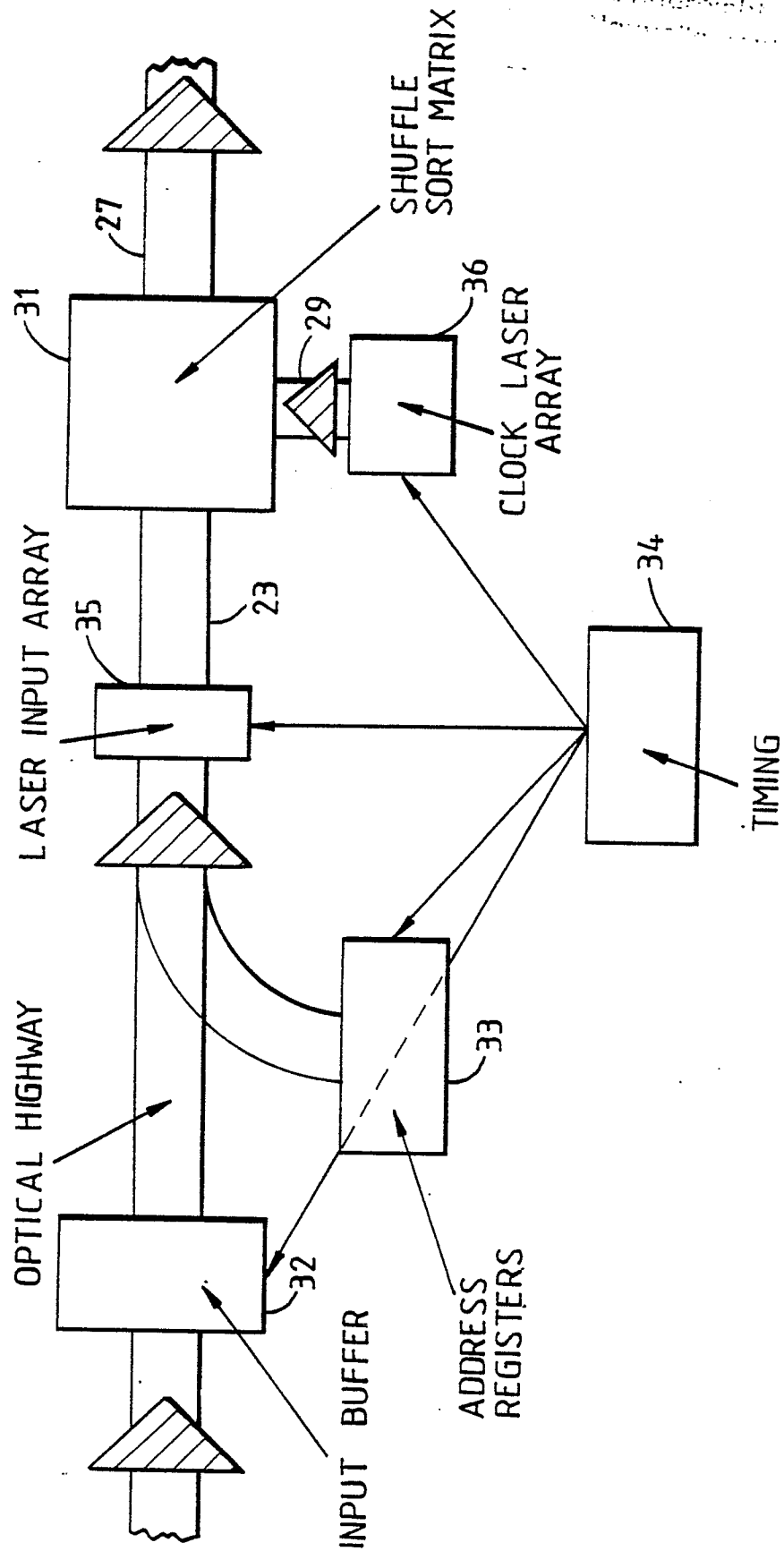
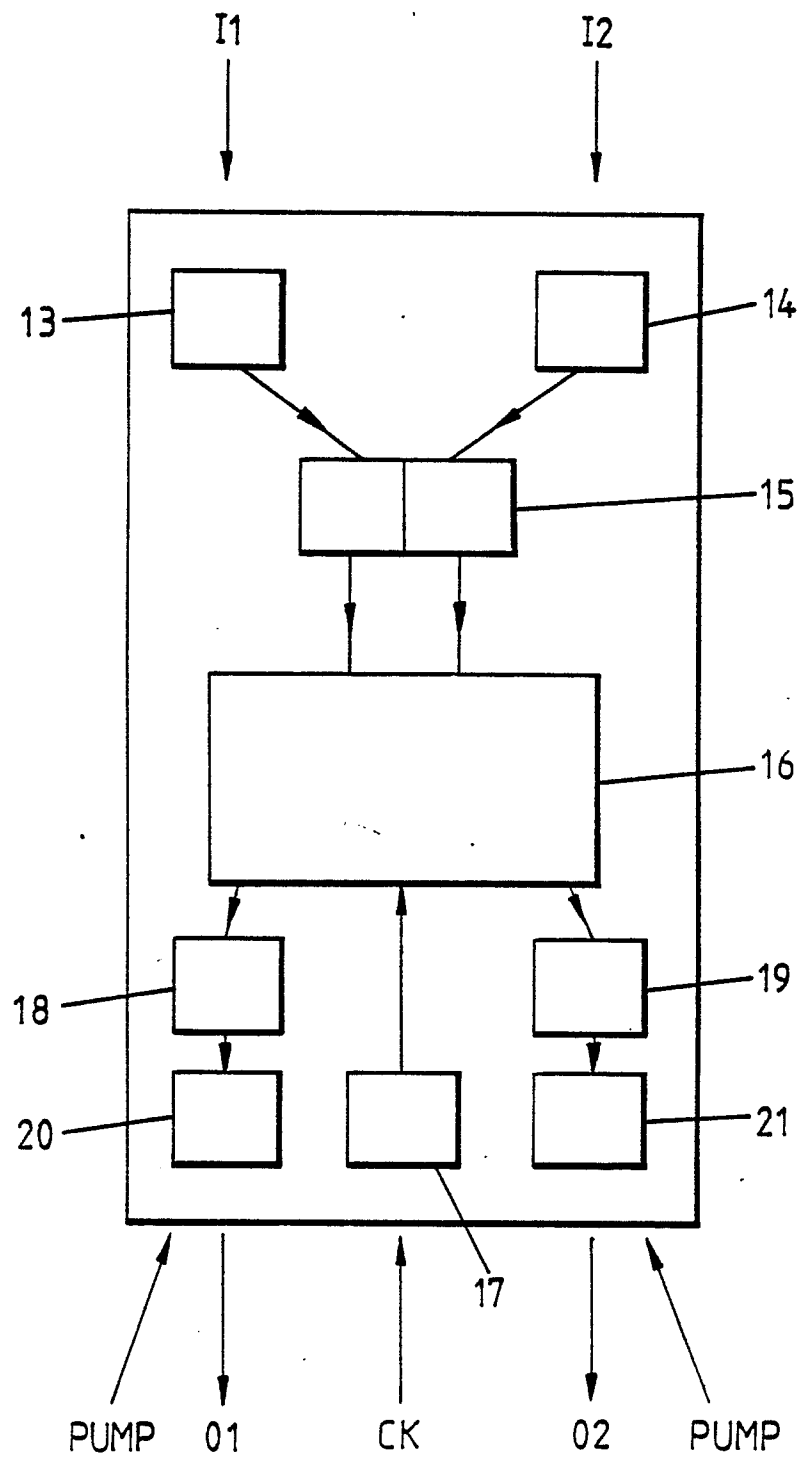
SYSTEM LAYOUT

Fig. 9

Neu eingereicht / Newly filed
Nouvellement déposé





EP 88 30 1842

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
D,A	IEE PROCEEDINGS, vol. 132, no. 6, part J, December 1985, pages 371-383, Hitchin, GB; J.E. MIDWINTER: "'Light' electronics, myth or reality?" * Pages 380,381, paragraphs 6.3,6.4 * ---	1,4,5,8	H 04 Q 3/52 H 04 B 9/00 G 06 F 7/56
A	WO-A-8 700 314 (ATT) * Figures 6-8; page 9, line 23 - page 14, line 25 * ---	1,4,5,8	
A	IEEE TRANSACTIONS ON COMPUTERS, vol. C-20, no. 2, February 1971, pages 153-161, IEEE, New York, US; H.S. STONE: "Parallel processing with the perfect shuffle" * Pages 156-159, paragraph V * ---	5,8	
A	PROCEEDINGS OF THE IEEE, vol. 72, no. 7, July 1984, pages 850-866, IEEE, New York, US; J.W. GOODMAN et al.: "Optical interconnections for VLSI systems" ---		TECHNICAL FIELDS SEARCHED (Int. Cl. 4)
A	THE 6TH ANNUAL SYMPOSIUM ON COMPUTER ARCHITECTURE, 23rd-25th April 1979, pages 168-177, IEEE, New York, US; J.H. PATEL: "Processor-memory interconnections for multiprocessors" -----		H 04 Q G 06 F H 03 K H 04 B
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 18-05-1988	Examiner VANDEVENNE M.J.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		I : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	