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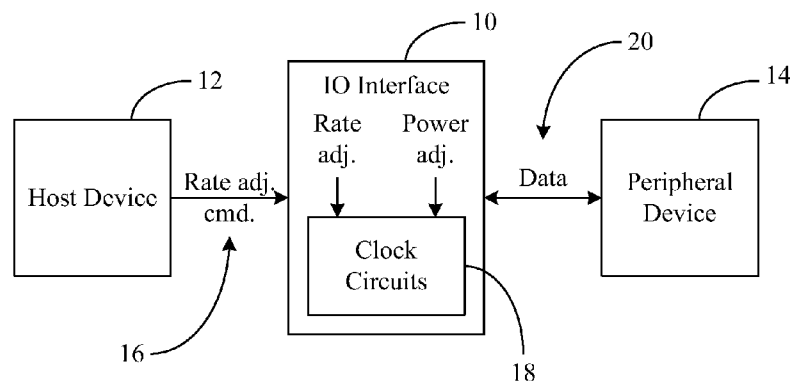
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(54) Title: RATE SCALABLE IO INTERFACE WITH ZERO STAND-BY POWER AND FAST START-UP



(57) Abstract: Systems and methods of interconnecting devices may include an input/output (IO) interface having one or more clock circuits, a power supply coupled to the one or more clock circuits, and logic to receive a rate adjustment command at the IO interface. The logic may also be configured to adjust a data rate of the IO interface in response to the rate adjustment command, and to adjust an output voltage of the power supply in response to the rate adjustment command.

RATE SCALABLE IO INTERFACE WITH ZERO STAND-BY POWER AND FAST START-UP

BACKGROUND

Technical Field

Embodiments generally relate to input/output (IO) interfaces. More particularly, embodiments relate to an IO connector configuration that has an adjustable data rate and enhanced power conservation.

Discussion

Computing systems may include one or more USB (Universal Serial Bus, e.g., USB Specification 2.0, USB Implementers Forum) ports to support IO communication with peripheral components such as keyboards, mice, cameras, and so forth. A typical USB port may be limited, however, to operation at a single data rate. Even if a lower data rate may be supported for backward compatibility, the power supply to the interface components containing the signaling circuits may remain at the nominal level required for higher speed operation. Accordingly, optimum power consumption in the interface might not be achievable for lower speed modes of operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The various advantages of the embodiments of the present invention will become apparent to one skilled in the art by reading the following specification and appended claims, and by referencing the following drawings, in which:

FIG. 1 is a block diagram of an example of a scheme of adjusting data rates in an input/output (IO) interface according to an embodiment;

FIG. 2 is a flowchart of an example of a method of adjusting data rates in an IO interface according to an embodiment;

FIGs. 3A and 3B are flowcharts of examples of methods of re-starting an IO interface according to embodiments;

FIGs. 4A and 4B are schematic diagrams of examples of IO links according to embodiments; and

FIG. 5 is a block diagram of an example of a connection between a host platform and a peripheral device according to an embodiment.

DETAILED DESCRIPTION

5 Embodiments may include an input/output (IO) interface having a datapath section with one or more clock circuits, a power supply coupled to the one or more clock circuits, and logic. The logic may be configured to receive a rate adjustment command at the IO interface, adjust a data rate of the IO interface in response to the rate adjustment command, and adjust an output voltage of the power supply in response to the rate
10 adjustment command.

 Embodiments may also include a host platform having a power supply, a host device to issue a rate adjustment command, and an IO interface with one or more datapath section clock circuits coupled to the power supply, and logic. The logic can be configured to receive the rate adjustment command at the IO interface, adjust a data rate
15 of the IO interface in response to the rate adjustment command, and adjust an output voltage of the power supply in response to the rate adjustment command.

 Other embodiments can involve a computer implemented method in which a rate adjustment command is received at an IO interface. The method may provide for adjusting a data rate of the IO interface in response to the rate adjustment command, and
20 adjusting an output voltage of a power supply associated with one or more clock circuits of the IO interface in response to the rate adjustment command.

 Additionally, embodiments may include a computer readable storage medium having a set of instructions which, if executed by a processor, cause an IO interface to receive a rate adjustment command at the IO interface. The instructions may also cause
25 the IO interface to adjust a data rate of the IO interface in response to the rate adjustment command, and adjust an output voltage of a power supply associated with one or more clock circuits of the IO interface in response to the rate adjustment command.

 Turning now to FIG. 1, an IO interface 10 between a host device 12 and a peripheral device 14 is shown. The host device 12 might include a chipset component
30 such as a processor and/or platform controller hub (PCH) of a personal digital assistant (PDA), mobile Internet device (MID), wireless smart phone, media player, imaging

device, smart tablet, desktop personal computer (PC), server, etc., or any combination thereof. In addition, the peripheral device 14 could include, for example, a keyboard, mouse, camera, PDA, MID, wireless smart phone, media player, imaging device, smart tablet, etc., or any combination thereof. In the illustrated example, the host device 12 issues a rate adjustment command 16, which is received by the IO interface 10. The IO interface 10 may incorporate, for example, USB technology, DisplayPort (DP, e.g., Embedded DisplayPort Standard (eDP) Version 1.3, January 2011, Video Electronics Standards Association) technology, High-Definition Multimedia Interface (HDMI, e.g., HDMI Specification, Ver. 1.3a, November 10, 2006, HDMI Licensing, LLC) technology, Thunderbolt (e.g., Thunderbolt™ Technology: The Transformational PC I/O, 2011, Intel Corporation) technology, Peripheral Components Interconnect Express (PCI-e, e.g., PCI Express x16 Graphics 150W-ATX Specification 1.0, PCI Special Interest Group) technology, and so forth.

The IO interface 10 may include one or more clock circuits 18 that are used to transfer data 20 between the peripheral device 14 and the platform containing the host device 12. As will be discussed in greater detail, the clock circuits 18 might include one or more phase locked loop (PLL) modules, clock and data recovery (CDR) modules, and so forth. In response to the rate adjustment command 16, the illustrated IO interface 10 adjusts the frequency of the clock circuits 18 (e.g., adjusts the data rate) and adjusts an output voltage of a power supply coupled to the clock circuits 18 and other IO signaling circuits (not shown) in the link. As will be discussed in greater detail, adjusting the data rate of the IO interface 10 enables the IO interface 10 to achieve scalable bandwidth. For example, the IO interface 10 may dynamically adapt itself to support high bandwidth when needed and scale back bandwidth support when data throughput is relatively low. Moreover, adjusting the power supplied to the clock circuits 18 in response to the rate adjustment command 16 enables the IO interface 10 to achieve significant power savings (e.g., voltage squared savings). Indeed, adjusting the power supplied to all IO signaling circuits (e.g., transmitters, receivers, coders, decoders, modulators, demodulators, etc.) may provide the best power/performance trade-off.

FIG. 2 shows a method 22 of adjusting data rates in an IO interface. The method 22 may be implemented as a set of logic instructions stored in a machine- or computer-

readable storage medium such as random access memory (RAM), read only memory (ROM), programmable ROM (PROM), flash memory, etc., in configurable logic such as programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs), in fixed-functionality logic hardware using circuit
5 technology such as application specific integrated circuit (ASIC), CMOS or transistor-transistor logic (TTL) technology, or any combination thereof. For example, computer program code to carry out operations shown in the method 22 may be written in any combination of one or more programming languages, including an object oriented programming language such as C++ or the like and conventional procedural
10 programming languages, such as the "C" programming language or similar programming languages. Moreover, the method 22 could be implemented using any of the aforementioned circuit technologies.

Processing block 24 provides for receiving a rate adjustment command. The rate adjustment command could be issued by a host device such as the host device 12 (FIG.
15 1), or other suitable computing system component and/or user. For example, the rate adjustment command could include an instruction to increase the data rate, decrease the data rate, power down the IO interface, re-start the IO interface, etc., wherein the decision to issue the rate adjustment command may be made based on the dynamic operating state of the platform (e.g., bandwidth requirements, power consumption, battery life), a static
20 condition of the platform (e.g., model/generation information), and/or a combination thereof. Illustrated block 26 adjusts a data rate of the IO interface in response to the rate adjustment command. The corresponding data rate adjustment may be conducted by modifying a frequency of one or more clock circuits such as clock circuits 18 (FIG. 1).

Processing block 28 provides for adjusting an output voltage of a power supply
25 associated with the one or more clock circuits in response to the rate adjustment command. Block 28 may also involve adjusting the power supplied to other IO signaling circuits such as transmitters, receivers, coders, decoders, modulators, demodulators, etc. The voltage adjustment could be made by modifying the output voltage of a voltage regulator residing in a semiconductor package on or near the IO interface connector, on a
30 circuit board (e.g., motherboard) containing the IO interface connector, and so forth. As will be discussed in greater detail, the adjustment could involve deactivating the voltage

regulator (e.g., in the case of the rate adjustment command including a power down command/instruction). The ability to dynamically adjust the voltage level of the power supplied to the IO interface clock circuits may provide the ability to achieve a V-squared (voltage squared) trade off in power versus performance. Indeed, deactivating the power supply to the clock circuits may result in zero stand-by power.

FIGs. 3A and 3B demonstrate varying approaches to re-starting an IO interface, for example, when the host platform has previously powered down the IO interface via a rate adjustment command. In particular, FIG. 3A shows a method 30 in which a re-start command is received at block 32, wherein illustrated block 34 activates a power supply/voltage regulator associated with one or more clock circuits of the IO interface in response to the re-start command. A common clock may be used to transfer data between the host platform and a peripheral device at block 36. The common clock could be a system clock that is distributed to all hosts and devices, or other suitable clock that is available to both the IO interface and the peripheral device (e.g., both sides of the link). Illustrated block 38 provides for determining whether a lock condition has occurred. The lock condition may include a re-locking of one or more control loops of the clock circuits so that synchronized timing and data transfer can be established for the link in question. Thus, the determination at block 38 might involve determining whether a PLL or CDR module of the IO interface can support synchronized data transfer across the link. If the lock condition is not detected, the illustrated approach continues to use the common clock to transfer data between the host platform and the peripheral device.

If the lock condition is detected, block 40 may switch to the standard reference clock of the IO interface and increase the data rate as appropriate. Thus, if the host platform is in a high bandwidth mode of operation (e.g., host device has requested a bandwidth-driven rate increase), block 40 could involve increasing the frequency of the reference clock to a maximum value supported by the IO interface. The rate increase could alternatively be to some intermediate value depending upon the circumstances. Indeed, if a higher data rate has not been requested or is otherwise not appropriate, the rate increase may be bypassed altogether in order to conserve power and/or extend battery life.

FIG. 3B shows an alternative method 42 that might be deployed in plesiochronous

environments in which a common clock is not available (e.g., link components use separate clocks that are constrained within specified limits of clock rate variability). In particular, blocks 32 and 34 may provide for receiving a re-start command and activating the power supply to the clock circuits, respectively, as already discussed. Illustrated
5 block 44, on the other hand, uses an oversampled local clock to transfer data between the host platform and the peripheral device until a lock condition is detected at block 46. Thus, the lock condition in the illustrated example might involve a link clock rate variability falling below a certain threshold. Once the lock condition is satisfied, illustrated block 48 switches to the normal sampling rate and increases the data rate of the
10 IO interface as appropriate. The methods 30, 42 may be implemented as a set of logic instructions stored in a machine- or computer-readable storage medium such as RAM, ROM, PROM, flash memory, etc., in configurable logic such as PLAs, FPGAs, CPLDs, in fixed-functionality logic hardware using circuit technology such as ASIC, CMOS or TTL technology, or any combination thereof.

15 Turning now to FIG. 4A, one example of an inbound link 50 is shown for architectures in which oversampling is used to re-start the link 50. In the illustrated example, a peripheral side 52 of the link 50 includes various signal processing components such as a coding unit 54, a modulation unit 56, an equalization unit 58, and a transmit buffer 60 to drive one or more signals onto a link medium such as a cable 62. A
20 host side 64 of the link 50 represents an IO interface such as IO interface 10 (FIG. 1), and may include a datapath section 85 having a receive buffer 66 configured to drive an edge sampling latch 68 as well as a data sampling latch 70. The architecture may also include an outbound link (not shown) having similar components for transferring data from the host side 64 to the peripheral side 52. In addition, a clock and data recovery (CDR)
25 module 72 may provide clock inputs to the latches 68, 70 based on a reference clock 74 and feedback outputs of the latches 68, 70. Thus, the CDR module 72 and latches 68, 70 may constitute a control loop for the datapath section 85. The illustrated approach also includes logic such as an IO controller 76 that sets the frequency of the reference clock 74 as well as the output voltage of a voltage regulator (VR) 78, which may provide power
30 to both sides 52, 64 of the link 50.

If the IO controller 76 receives a request to re-start the link 50, the IO controller

may activate the VR 78 and instruct a multiplexer 80 to use the output of an oversampling section 84 of the IO interface until the CDR module 72 achieves an acceptable level of clock rate variability in the datapath section 85 (e.g., lock condition is detected). In particular, the illustrated oversampling section 84 includes a set of receive
5 buffers 86 (86a, 86b) and corresponding latches 88 (88a, 88b), which are powered by a separate power supply 90 for the oversampling section 84. The output of an oversampling (post processing) module 82 may be fed to the multiplexer 80 and used on a selective basis dictated by the IO controller 76. Once the lock condition is detected, the illustrated IO controller 76 may instruct the multiplexer 80 return to use of the output of
10 the datapath section 85 for a data output 81 to the host platform. In addition, the IO controller 76 could then increase the frequency of the reference clock 74 as appropriate. The separate power supply 90 enables the oversampling section 84 to be powered down when not in use.

FIG. 4B shows an inbound link 92 in which a host side 94 of the link 92 includes an
15 IO interface with a datapath section 96 that provides a data output 101 based on either a reference clock 104 or a common clock 98. The architecture may also include an outbound link (not shown) having components for transferring data from the host side 94 to the peripheral side 52. In the illustrated example, logic such as an IO controller 100 selects the appropriate clock by providing a signal to a multiplexer 102. Thus, in normal
20 operation, the reference clock 104 may be supplied to a CDR 106, which in turn controls latches 68, 70, as already described. If, on the other hand, the IO interface is powered down and the IO controller 76 receives a re-start command, the illustrated IO controller 100 activates the VR 78 and instructs the multiplexer 102 to use the common clock 98 until the lock condition is detected. Detection of the lock condition may therefore trigger
25 a switch of the multiplexer 102 back to using the reference clock 104. In addition, the IO controller 100 may increase the frequency of the reference clock 104 if, for example, a rate increase request/command has been received.

Turning now to FIG. 5, a host platform 108 is shown in which an IO interface 110
is used to interconnect the platform 108 with a peripheral device 112. As already noted,
30 the host platform 108 could be part of a mobile device such as a PDA, MID, wireless smart phone, media player, imaging device, smart tablet, etc., or any combination thereof.

The host platform 108 could alternatively include a fixed platform such as a desktop PC or a server. In addition, the peripheral device 112 might include a keyboard, mouse, camera, PDA, MID, wireless smart phone, media player, imaging device, smart tablet, etc., or any combination thereof. In the illustrated example, the host platform 108 also
5 has a processor 114, system memory 116, a platform controller hub (PCH) 118, mass storage (e.g., hard disk drive/HDD, optical disk, flash memory) 120, a network controller 122, and various other controllers (not shown). The processor 114 may include one or more processor cores (not shown) capable of executing a set of stored logic instructions, and an integrated memory controller (IMC) 124 configured to communicate with the
10 system memory 116. The system memory 116 could include, for example, dynamic random access memory (DRAM) configured as a memory module such as a dual inline memory module (DIMM), a small outline DIMM (SODIMM), etc.

The illustrated PCH 118, sometimes referred to as a Southbridge of a chipset, functions as a host device and may communicate with the network controller 122, which
15 could provide off-platform wireless communication functionality for a wide variety of purposes such as, for example, cellular telephone (e.g., W-CDMA (UMTS), CDMA2000 (IS-856/IS-2000), etc.), Wi-Fi (e.g., IEEE 802.11-2007, Wireless Local Area Network/LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications), Low-Rate Wireless PAN (e.g., IEEE 802.15.4-2006, LR-WPAN),
20 Bluetooth (e.g., IEEE 802.15.1-2005, Wireless Personal Area Networks), WiMax (e.g., IEEE 802.16-2004, LAN/MAN Broadband Wireless LANS), Global Positioning System (GPS), spread spectrum (e.g., 900 MHz), and other radio frequency (RF) telephony purposes. The network controller 122 could also provide off-platform wired communication (e.g., RS-232 (Electronic Industries Alliance/EIA), Ethernet (e.g., IEEE
25 802.3-2005, LAN/MAN CSMA/CD Access Method), power line communication (e.g., X10, IEEE P1675), USB (e.g., Universal Serial Bus 2.0 Specification), digital subscriber line (DSL), cable modem, T1 connection), etc., functionality.

The illustrated IO interface 110 includes logic 126 to receive rate adjustment commands from the PCH 118, adjust the data rate of the IO interface 110 based on the
30 rate adjustment commands, and adjust the output voltage of a voltage regulator that supplies one or more clock circuits in response to the rate adjustment commands, as

already discussed. In particular, the logic 126 may be configured to quickly re-start the IO interface 110 by using either a common clock or an oversampled clock until the clock circuits of the IO interface 110 have had the opportunity to re-lock.

Thus, the techniques described herein may provide the ability for a link at any given generation level to operate across a wide range of data rates. To optimize the power per data rate, the clock circuit power supply can be optimized as a function of data rate using voltage regulators located either on the motherboard or in silicon dedicated to link operation and near the IO connector. Such an approach may yield a V-squared power trade-off with data rate as well as the ability to completely power a link off. In particular, all circuit elements of a link can be powered down (except those that maintain state data), and quickly returned to active status.

Embodiments of the present invention are applicable for use with all types of semiconductor integrated circuit ("IC") chips. Examples of these IC chips include but are not limited to processors, controllers, chipset components, programmable logic arrays (PLAs), memory chips, network chips, systems on chip (SoCs), SSD/NAND controller ASICs, and the like. In addition, in some of the drawings, signal conductor lines are represented with lines. Some may be different, to indicate more constituent signal paths, have a number label, to indicate a number of constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. This, however, should not be construed in a limiting manner. Rather, such added detail may be used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit. Any represented signal lines, whether or not having additional information, may actually comprise one or more signals that may travel in multiple directions and may be implemented with any suitable type of signal scheme, e.g., digital or analog lines implemented with differential pairs, optical fiber lines, and/or single-ended lines.

Example sizes/models/values/ranges may have been given, although embodiments of the present invention are not limited to the same. As manufacturing techniques (e.g., photolithography) mature over time, it is expected that devices of smaller size could be manufactured. In addition, well known power/ground connections to IC chips and other components may or may not be shown within the figures, for simplicity of illustration and discussion, and so as not to obscure certain aspects of the embodiments of the invention.

Further, arrangements may be shown in block diagram form in order to avoid obscuring embodiments of the invention, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the embodiment is to be implemented, i.e., such specifics should
5 be well within purview of one skilled in the art. Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the invention, it should be apparent to one skilled in the art that embodiments of the invention can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

10 The term “coupled” may be used herein to refer to any type of relationship, direct or indirect, between the components in question, and may apply to electrical, mechanical, fluid, optical, electromagnetic, electromechanical or other connections. In addition, the terms “first”, “second”, etc. might be used herein only to facilitate discussion, and carry no particular temporal or chronological significance unless otherwise indicated.

15 Those skilled in the art will appreciate from the foregoing description that the broad techniques of the embodiments of the present invention can be implemented in a variety of forms. Therefore, while the embodiments of this invention have been described in connection with particular examples thereof, the true scope of the embodiments of the invention should not be so limited since other modifications will become apparent to the
20 skilled practitioner upon a study of the drawings, specification, and following claims.

CLAIMS

We claim:

1. A host platform comprising:
5 a power supply;
a host device to issue a rate adjustment command; and
an input/output (IO) interface including a datapath section having one or more
clock circuits coupled to the power supply, and logic to,
receive the rate adjustment command at the IO interface,
10 adjust a data rate of the IO interface in response to the rate adjustment
command, and
adjust an output voltage of the power supply in response to the rate
adjustment command.
- 15 2. The host platform of claim 1, wherein the rate adjustment command is to
include a power down command and the logic is to deactivate the power supply in
response to the power down command.
- 20 3. The host platform of claim 2, wherein the host device is to issue a re-start
command and the logic is to,
receive the re-start command at the IO interface, and
activate the power supply in response to the re-start command.
- 25 4. The host platform of claim 3, wherein the one or more clock circuits
include one or more control loops and the logic is to,
detect a lock condition of the one or more control loops, and
increase the data rate of the IO interface in response to the lock condition.
- 30 5. The host platform of claim 4, wherein the logic is to use a common clock
to transfer data between the host platform and a peripheral device until the lock condition
is detected.

6. The host platform of claim 4, wherein the logic is to use an oversampled local clock to transfer data between the host platform and a peripheral device until the lock condition is detected.

5

7. The host platform of claim 1, wherein the one or more clock circuits include a phase locked loop (PLL) module.

8. The host platform of claim 1, wherein the one or more clock circuits
10 include a clock and data recovery (CDR) module.

9. An input/output (IO) interface comprising:
a datapath section including one or more clock circuits;
a power supply coupled to the one or more clock circuits; and
15 logic to,
receive a rate adjustment command at the IO interface,
adjust a data rate of the IO interface in response to the rate adjustment
command, and
adjust an output voltage of the power supply in response to the rate
20 adjustment command.

10. The IO interface of claim 9, wherein the rate adjustment command is to
include a power down command and the logic is to deactivate the power supply in
response to the power down command.

25

11. The IO interface of claim 10, wherein the logic is to,
receive a re-start command at the IO interface, and
activate the power supply in response to the re-start command.

30 12. The IO interface of claim 11, wherein the one or more clock circuits
include one or more control loops and the logic is to,

detect a lock condition of the one or more control loops, and
increase the data rate of the IO interface in response to the lock condition.

13. The IO interface of claim 12, wherein the logic is to use a common clock
5 to transfer data between a host platform and a peripheral device until the lock condition is
detected.

14. The IO interface of claim 12, wherein the logic is to use an oversampled
local clock to transfer data between a host platform and a peripheral device until the lock
10 condition is detected.

15. The IO interface of claim 9, wherein the one or more clock circuits include
a phase locked loop (PLL) module.

16. The IO interface of claim 9, wherein the one or more clock circuits include
15 a clock and data recovery (CDR) module.

17. A computer implemented method comprising:
receiving a rate adjustment command at an input/output (IO) interface;
20 adjusting a data rate of the IO interface in response to the rate adjustment
command; and
adjusting an output voltage of a power supply associated with one or more clock
circuits of the IO interface in response to the rate adjustment command.

18. The method of claim 17, wherein the rate adjustment command includes a
25 power down command and adjusting the output voltage includes deactivating the power
supply associated with the one or more clock circuits in response to the power down
command.

19. The method of claim 18, further including:
30 receiving a re-start command at the IO interface; and

activating the power supply in response to the re-start command.

20. The method of claim 19, further including:

detecting a lock condition of one or more control loops of the one or more clock

5 circuits; and

increasing the data rate of the IO interface in response to the lock condition.

21. The method of claim 20, further including using a common clock to

transfer data between a host platform and a peripheral device until the lock condition is

10 detected.

22. The method of claim 20, further including using an oversampled local

clock to transfer data between a host platform and a peripheral device until the lock

condition is detected.

15

23. The method of claim 17, wherein the output voltage of a power supply

associated with at least one of a phase locked loop (PLL) module and a clock and data

recovery (CDR) module is adjusted in response to the rate adjustment command.

24. A computer readable storage medium comprising a set of instructions

20 which, if executed by a processor, cause an input/output (IO) interface to:

receive a rate adjustment command at the IO interface;

adjust a data rate of the IO interface in response to the rate adjustment command;

and

25 adjust an output voltage of a power supply associated with one or more clock

circuits of the IO interface in response to the rate adjustment command.

25. The medium of claim 24, wherein the rate adjustment command is to

include a power down command and the instructions, if executed, cause the IO interface

30 to deactivate the power supply associated with the one or more clock circuits in response

to the power down command.

26. The medium of claim 25, wherein the instructions, if executed, cause the IO interface to:

receive a re-start command at the IO interface; and

5 activate the power supply in response to the re-start command.

27. The medium of claim 26, wherein the instructions, if executed, cause the IO interface to:

detect a lock condition of one or more control loops of the one or more clock
10 circuits; and

increase the data rate of the IO interface in response to the lock condition.

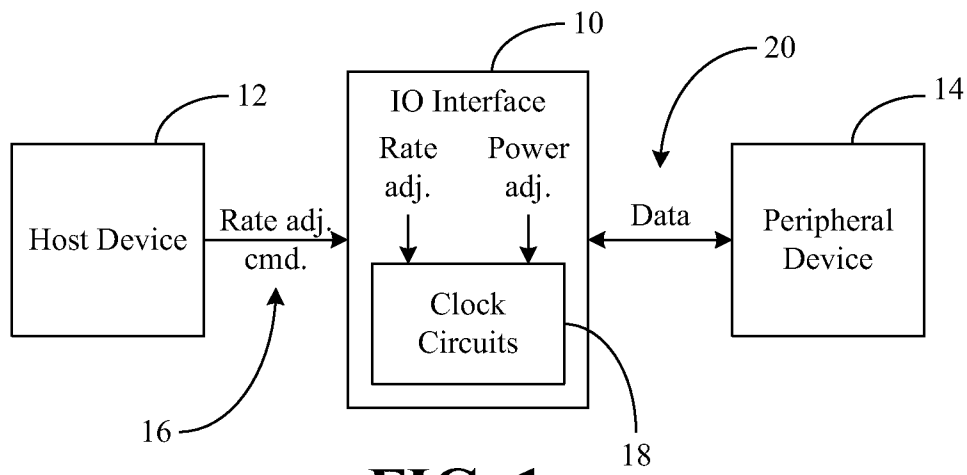
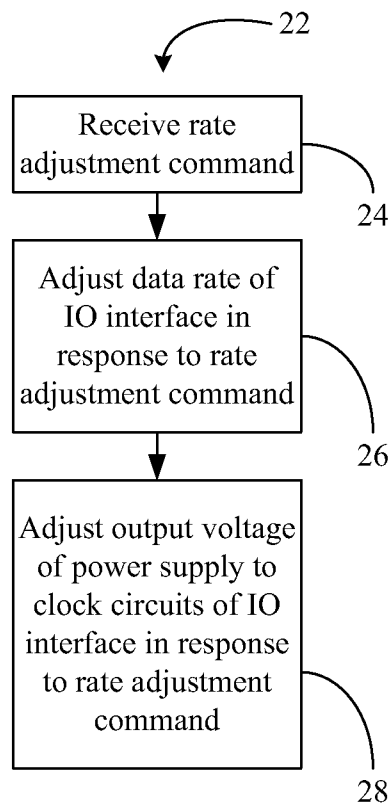
28. The medium of claim 27, wherein the instructions, if executed, cause the IO interface to use a common clock to transfer data between a host platform and a
15 peripheral device until the lock condition is detected.

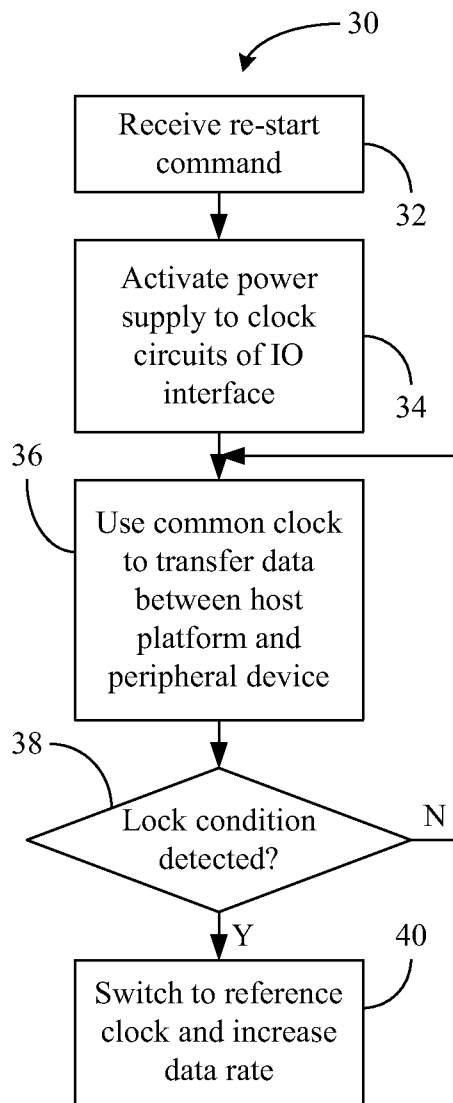
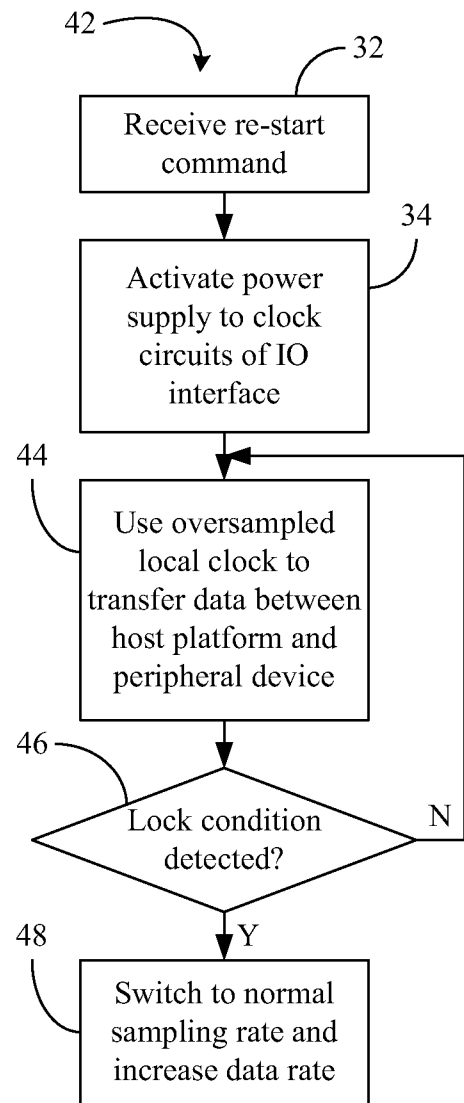
29. The medium of claim 27, wherein the instructions, if executed, cause the IO interface to use an oversampled local clock to transfer data between a host platform and a peripheral device until the lock condition is detected.

20

30. The medium of claim 24, wherein the output voltage of a power supply associated with at least one of a phase locked loop (PLL) module and a clock and data recovery (CDR) module is adjusted in response to the rate adjustment command.

25

**FIG. 1****FIG. 2**

**FIG. 3A****FIG. 3B**

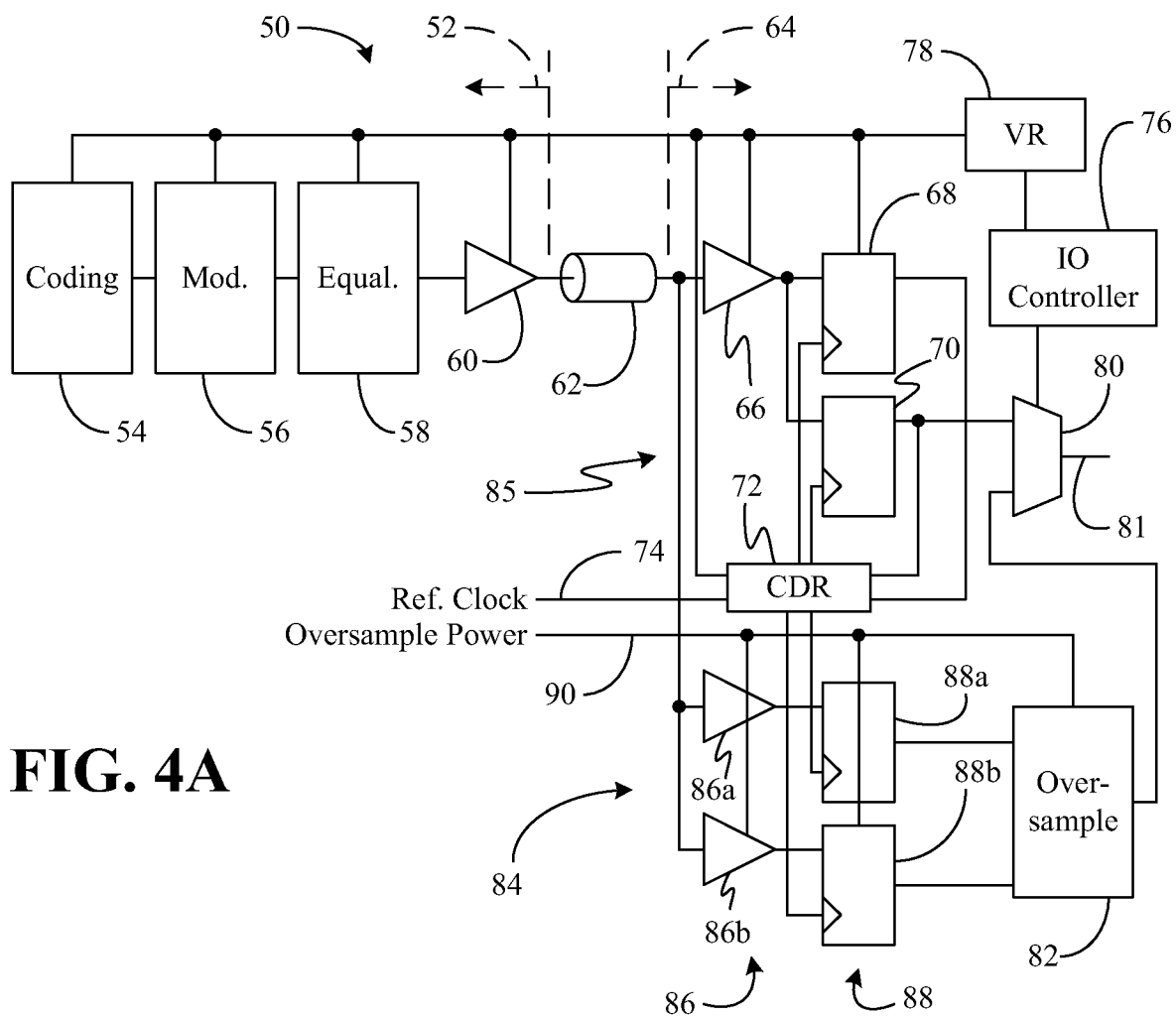


FIG. 4A

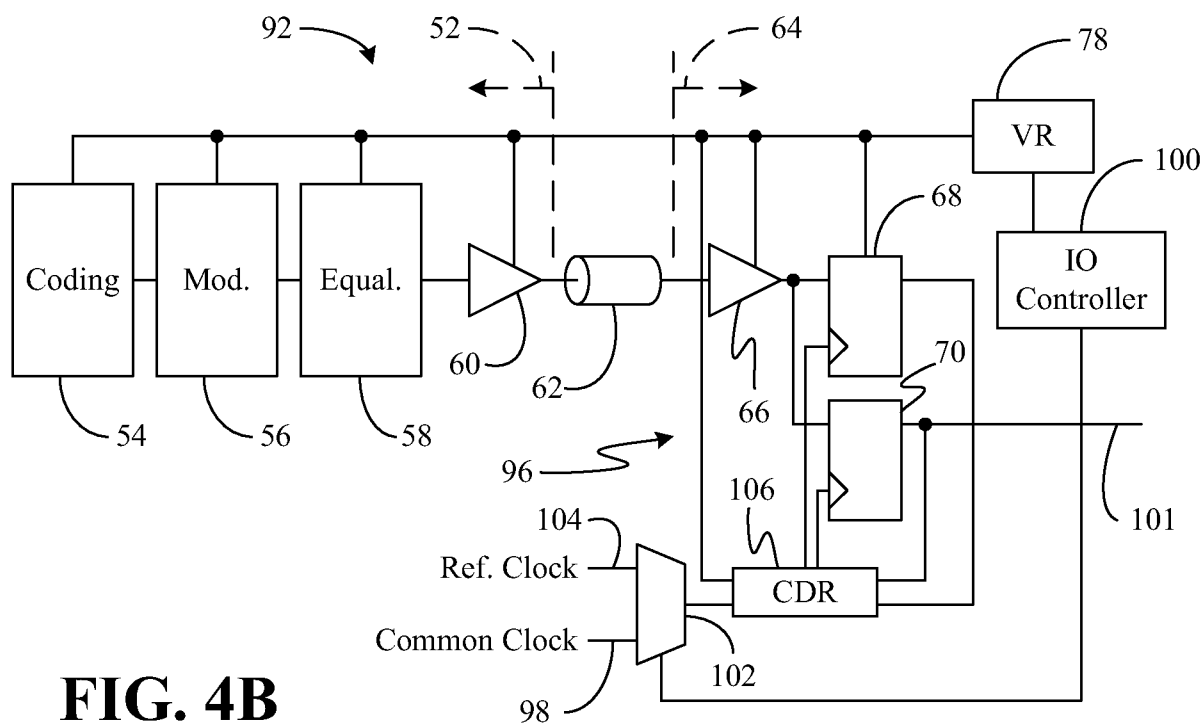
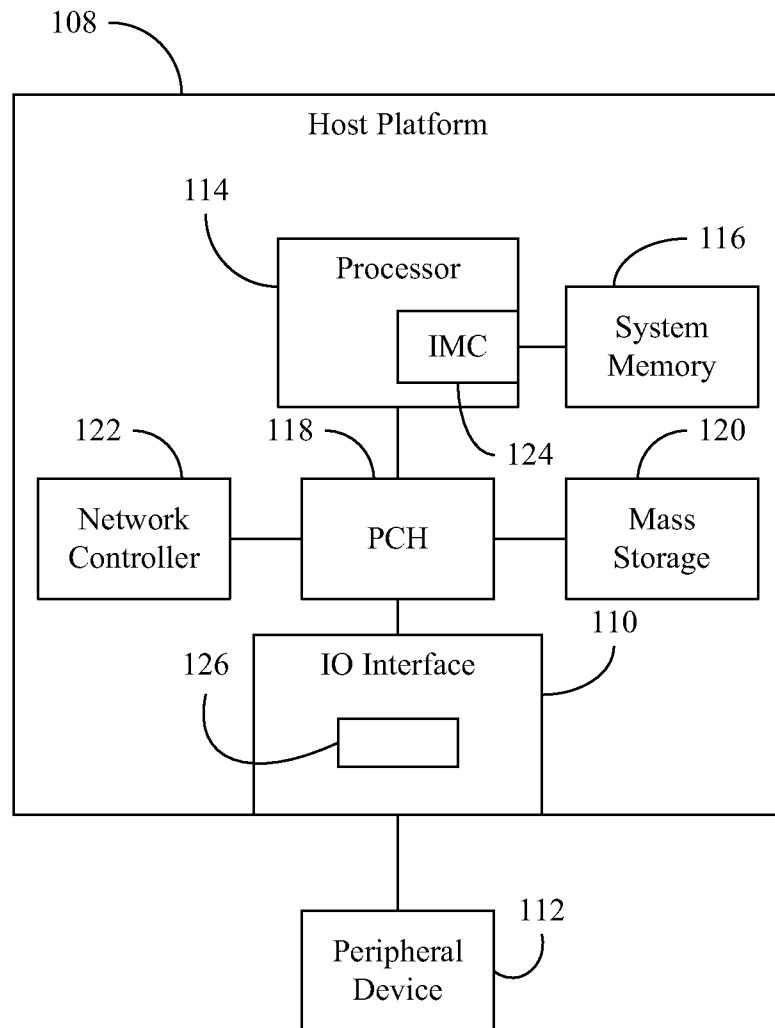


FIG. 4B

**FIG. 5**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/058194**A. CLASSIFICATION OF SUBJECT MATTER****G06F 13/14(2006.01)i, G06F 1/26(2006.01)i, G06F 1/04(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 13/14; H04N 7/173; G06F 5/06; G06F 1/26; G02F 1/00; H04B 10/00; G06F 1/12; H04N 11/02; G06F 1310

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: host, data rate, power, clock

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002-0108070 A1 (JANG GEUN OH) 08 August 2002 See the abstract; figures 3,6,8 and their corresponding description; claims 1-2, 5-9	1-30
Y	US 2005-0289621 A1 (PETER MUNGULA) 29 December 2005 See the abstract; figure 2; paragraph [0024]; claims 1-2, 5-7, 9	1-30
Y	US 2010-0257398 A1 (ALEXANDER JAMES W. et al.) 07 October 2010 See the abstract; figures 3A-3C and their corresponding description	1,7,9,15,17,23,24,30
Y	US 2009-0148155 A1 (LATCHMAN RYAN S.) 11 June 2009 See the abstract; figures 4-9 and their corresponding description	1,8,9,16,17,23,24,30
A	US 2003-0070103 A1 (HYEONG SEOG KIM) 10 April 2003 See figures 1-2; paragraphs [0025]-[0034]; claim 1	1,9,17,24
A	US 6839778 B1 (SARTORE RONALD H. et al.) 04 January 2005 See figures 1-2; column 1, line 65- column 2, line 63; claims 1,7	1,9,17,24

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search

24 MAY 2012 (24.05.2012)

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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