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(54) Title: SCRUBBING DATA IN A MEMORY DEVICE

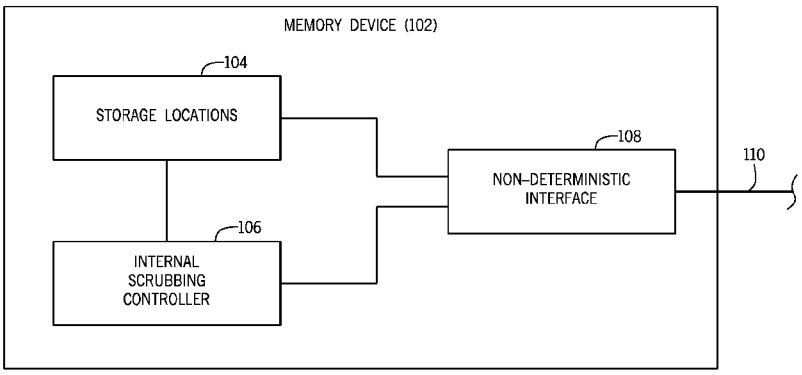

FIG. 1

(57) Abstract: A memory device includes storage locations to store data, and an internal controller to perform scrubbing of a portion of the data stored by at least one storage location of the storage locations. The memory device also includes an interface to communicate non-deterministically over a communication bus with a memory controller.

SCRUBBING DATA IN A MEMORY DEVICE

Background

[0001] An electronic device can include various electronic components, including a processor and storage media to store data. The storage media can include a memory device and a secondary storage device, where the secondary storage device can include a disk-based storage device or a solid state storage device. In some examples, the memory device can be implemented as a dynamic random access memory (DRAM) device, or other type of memory device.

Brief Description Of The Drawings

[0002] Some implementations of the present disclosure are described with respect to the following figures.

[0003] Fig. 1 is a block diagram of an example memory device, including an internal scrubbing controller according to some implementations.

[0004] Fig. 2 is a flow diagram of an example process performed by the memory device, according to some implementations.

[0005] Fig. 3 is a block diagram of an example electronic device that includes a memory controller and a memory device, according to some implementations.

[0006] Fig. 4 is a block diagram of another example electronic device according to further implementations.

Detailed Description

[0007] Errors may occur in data stored in a memory device. Such errors can include soft errors in the data caused by alpha particle emissions from the packaging of the memory device, or errors caused by structural defects in the memory device. To perform error detection and correction, a memory controller, which is external of the memory device, can store error correction code (ECC) information in the memory device. The ECC information can be used by the external memory controller to

detect errors in data, and to correct certain errors (e.g. errors of less than a predetermined number of bits of data).

[0008] Some memory designs rely on use of a communication bus (sometimes referred to as a "memory bus") between the memory controller and the memory device, where communications over the communication bus is according to a deterministic protocol. With a deterministic protocol, the memory controller can issue a memory access command to the memory device, and expects a response to the memory access command within an expected amount of time (e.g. within an expected amount of cycles of a clock signal). Failure to respond within the expected amount of time (i.e. deterministic amount of time) results in a failure condition at the memory controller.

[0009] Also, some memory designs rely on the memory controller that is external of the memory device to perform error detection and correction of data stored in the memory device. Performing error detection and correction at the memory controller using ECC information in the memory device involves communication of data and ECC information over the communication bus to the memory controller, which can lead to extra traffic over the communication bus. In arrangements where the communication bus is shared by multiple memory devices, the extra traffic for error detection and correction of data can reduce an overall bandwidth available to the memory devices.

[0010] In accordance with some implementations of the present disclosure, a memory device is provided with an internal scrubbing controller that can perform scrubbing of data stored in the memory device. The scrubbing of data includes the following operations performed within the memory device: checking the data for errors, correcting the errors, and storing the corrected data in the memory device. The scrubbing can be performed by the memory device without any scrubbing instruction (e.g. a command to initiate scrubbing) from an external memory controller. In addition, the memory device is able to communicate over a communication bus with the external memory controller according to a non-deterministic protocol.

[0011] Use of the non-deterministic protocol on the communication bus between the memory controller and the memory device can mean that an initiator of a memory transaction (e.g. the memory controller) is unable to determine when a response from the target of the memory transaction (e.g. the memory device) may be expected. Stated differently, the responding component, in this case the memory device, is unable to respond to a request from the memory controller within a deterministic amount of time (i.e. within a predefined amount of time).

[0012] Although reference is made to the memory controller and the memory device as being the initiator and target, respectively, of a memory transaction over the communication bus, it is noted that in other examples, the memory device can be the initiator of a memory transaction, and the memory controller can be the target of the memory transaction.

[0013] The internal scrubbing in the memory device can be performed as a background process in the memory device, i.e. when the memory device is not actively accessing data in response to a memory access command (e.g. command to write data or command to read data) from the memory controller. In some implementations, the internal scrubbing controller can perform the scrubbing in response to the memory device having been idle for a predetermined amount of time.

[0014] Fig. 1 is a block diagram of an example memory device 102 that includes storage locations 104 to store data, and an internal scrubbing controller 106 to perform scrubbing of the data stored by the storage locations 104. In some examples, the memory device 102 can be a dynamic random access memory (DRAM) device or a static random access memory (SRAM) device. In other examples, the memory device 102 can be a different type of memory device, including a phase change memory device, a resistive random access memory (ReRAM) device, a spin-transfer torque (STT) memory device, and so forth.

[0015] The storage locations 104 can be arranged as a storage array of storage locations, also referred to as storage cells, where the storage cells are arranged in

rows and columns in the storage array. Each storage cell can store one or multiple bits of data.

[0016] The memory device further includes a non-deterministic interface 108 to communicate non-deterministically over a communication bus 110, such as an external memory controller (not shown in Fig. 1) that it is external of the memory device 102 and that manages access of the memory device 102 in response to a memory access request received by the memory controller from a requester.

[0017] The non-deterministic interface 108 allows the memory device 102 to communicate according to a non-deterministic protocol over the communication bus 110. As noted above, use of these non-deterministic protocol means that the memory transaction requester is unable to determine when a response from the memory transaction target may be expected. In some examples, once the memory controller issues a memory access command (e.g. a command to read data from the memory device 102, a command to write data to the memory device, etc.) to the memory device 102, the memory controller can proceed to perform other tasks while the memory device 102 processes the memory access command from the memory controller. When the memory device 102 is ready to send a response to the memory controller, the memory device 102 can send an indication to the memory controller that such response is available from the memory device 102 and can be sent from the memory device 102. The indication can be in the form of a signal, a message, a field within a message, or any other type of indication.

[0018] The response from the memory device 102 can include data read from the storage locations 104 in response to a read command from the memory controller. Alternatively, the response can include an acknowledgement that a write has been completed successfully at the memory device 102 in response to a write command from the memory controller.

[0019] The internal scrubbing controller 106 can perform scrubbing of the data in the storage locations 104 on an intermittent basis. For example, the internal scrubbing controller 106 can activate scrubbing in the memory device 102 in

response to the memory device 102 having been idle for a predetermined amount of time. In some examples, if the memory device 102 has been idle for a predetermined amount of time, the memory device 102 can enter a self-refresh operation to perform refresh of data of the storage locations 104. Self-refresh is discussed further below.

[0020] The scrubbing performed by the internal scrubbing controller 106 can be performed as part of the self-refresh performed in the memory device 102, in some implementations. In other implementations, the scrubbing performed by the internal scrubbing controller 106 does not have to be part of self-refresh and can be independent of self-refresh.

[0021] Fig. 2 is a flow diagram of a process that is performed by a memory device, such as the memory device 102, according to some implementations. The memory device 102 initiates (at 202) without any scrubbing instruction from an external memory controller, scrubbing of data stored in the memory device 102. The initiating of the scrubbing can be performed by the internal scrubbing controller 106 in response to an event, such as the internal scrubbing controller 106 detecting that the memory device 102 has been idle (i.e. has not performed any operation to access the storage locations 104 in response to a memory access command from the memory controller). In other examples, the internal scrubbing controller 106 can initiate the scrubbing of data in response to another event, such as a periodic event that is triggered after passage of a predetermined amount of time.

[0022] The scrubbing is of a portion of the data stored by at least one storage location of the storage locations 104, where the scrubbing includes reading the portion of the data, detecting and correcting an error in the portion of the data to produce a corrected data portion, and writing the corrected data portion to the at least one storage location of the storage locations 104.

[0023] Once initiated, the scrubbing of data in the memory device 102 can continue (by accessing different storage locations in the memory device 102) until a stopping event is detected. In response to the stopping event, the internal scrubbing

controller 106 can stop the scrubbing. Examples of stopping events can include any of the following: a memory access command is received from the external memory controller, a predetermined amount of time has passed, data in a predetermined number of storage locations has been scrubbed, or another event.

[0024] The memory device 102 receives (at 204) a memory access command from the external memory controller over a communication bus. The memory device 102 responds (at 206) over the communication bus to the memory access command in a non-deterministic amount of time, according to the non-deterministic protocol discussed above.

[0025] Fig. 3 is a block diagram of an example electronic device 302 according to some implementations. The electronic device 302 includes the memory device 102 that is coupled over the communication bus 110 to a memory controller 304. The memory controller 304 is external of the memory device 102, and can receive a memory access request 310 from a requester (not shown) in the electronic device 302. The requester can be a processor, an input/output (I/O) component (e.g. network interface controller, graphics controller, etc.), or any other component in the electronic device 302 that is able to perform access of data in the memory device 102.

[0026] The memory device 102 includes the storage locations 104, the internal scrubbing controller 106, and the interface 108. In addition, the memory device 102 includes ECC information 306 stored in a storage region 308 of the memory device 102. The storage region 308 can be a region that is part of the storage locations 104, or alternatively, the storage region 308 to store the ECC information 306 can be separate from the storage locations 104.

[0027] The scrubbing controller 106 uses the ECC information 306 to perform scrubbing of the data in the storage locations 104. The ECC information 306 enables the scrubbing controller 106 to detect up to a first number of bits of error, and to correct up to a second number of bits of error, where the second number is less than the first number.

[0028] Fig. 4 is a block diagram of another example electronic device 402 that includes a memory device 404 according to further implementations. As shown in Fig. 4, a memory device 404 includes the storage locations 104, the storage region 308 to store the scrubbing ECC information 306 useable by the internal scrubbing controller 106.

[0029] In addition, the memory device 404 includes a self-refresh controller 406 that can perform a self-refresh in the memory device 404. Self-refresh can be performed in a memory device that can lose storage charge in a storage cell of the memory device 404. An example of a storage cell that can lose charge over time is a storage cell of a DRAM. In a DRAM, a storage cell is implemented as a storage capacitor, which can store a representation of a "0" or a "1." Over time, the charge in the storage capacitor can leak away, which can cause the data bit in the storage capacitor to be eventually lost. A refresh can be performed to refresh the storage cells of the DRAM device, to replenish the charge in the storage cells.

[0030] The self-refresh controller 406 can initiate a self-refresh operation in the memory device 404 without any refresh instruction from the memory controller 304. The self-refresh controller 406 can detect that the memory device 404 has been idle for a predetermined amount of time, and in response to such detection, the self-refresh controller 406 can initiate a self-refresh operation in the memory device 404. The self-refresh operation includes accessing portions of the storage locations 104 to read the data in the accessed portion, and replenishing the storage charge in the accessed portion of the storage locations 104.

[0031] In some implementations, the internal scrubbing controller 106 can perform scrubbing in conjunction with the self-refresh operation of the self-refresh controller 406. As data portions are being accessed by the self-refresh controller 406 to perform the self-refresh, the internal scrubbing controller 106 can use the ECC information 306 to detect errors in the accessed data portions and to correct such errors.

[0032] In the example of Fig. 4, the storage locations 104 can include a data portion 408 to store data (e.g. data written by a requester such as a processor or other requester), and an ECC portion 410 to store ECC information that is useable by the memory controller 304 to perform error detection and correction of data stored in the data portion 408 of the storage locations 104. Note that the ECC information stored in the ECC portion 410 is distinct from the scrubbing ECC information 306. During a read by the memory controller 304 of data in the data portion 408, the memory device 404 outputs the accessed data along with the corresponding ECC information. The memory controller 304 then uses the ECC information returned by the memory device 404 to check for errors in the data that is returned by the memory device 404, and to correct certain types of errors detected.

[0033] During a write operation, the memory controller 304 generates the corresponding ECC information based on the write data, and writes the write data and corresponding ECC information to the data portion 408 and the ECC portion 410, respectively, of the storage locations 104.

[0034] The memory device 404 can also include a self-training controller 412, which can perform self-training of the interface 108 to the communication bus 110. In performing the self-training on the communication bus 110, the self-training controller 412 can cause the interface 108 to transmit predetermined patterns over the communication bus 110 to the memory controller 304. The self-training controller 412 can also receive patterns transmitted by the memory controller 304. Based on the received patterns, the self-training controller 412 can detect timings between control signals on the communication bus 110 and corresponding data relative to the control signals. For example, the control signal can include a strobe or clock signal that is sent by the memory controller 304. Based on the predetermined patterns, the self-training controller 412 can detect an optimal timing from the strobe or clock signal to the peak point (highest amplitude) of the data, which determines the optimal timing between the control signal and the data. The self-training controller 412 can also determine optimal voltages to use for different signals on the communication bus 110.

[0035] The memory device 404 can also include a temperature sensor 414. In other examples, the temperature sensor 414 can be external of the memory device 404, but is coupled to the memory device 404 so that the internal scrubbing controller 106 can receive a temperature measurement of the temperature sensor 414. The temperature measurement from the temperature sensor 414 (whether internal to the memory device 404 or external of the memory device 404) is representative of the temperature of the memory device 404.

[0036] A rate at which scrubbing is performed can be based on the temperature of the memory device 404, as indicated by the temperature sensor 414. The internal scrubbing controller 106 can increase the rate at which scrubbing is performed in response to detecting a higher temperature of the memory device 404. Thus, in response to such higher temperature, the internal scrubbing controller 106 can initiate a new scrubbing operation after passage of a smaller time interval from the previous scrubbing operation. On the other hand, in response to detecting a lower temperature of the memory device 404, the internal scrubbing controller 106 can reduce a rate at which scrubbing is performed, by initiating a new scrubbing operation after passage of a larger time interval from the previous scrubbing operation.

[0037] Each of the internal scrubbing controller 106, the self-refresh controller 406, and the self-training controller 412 can be implemented as processing hardware, such as a microprocessor, a microcontroller, a programmable integrated circuit, a programmable gate array, or another type of processing hardware. Each of the internal scrubbing controller 106, the self-refresh controller 406, and the self-training controller 412 can be implemented entirely in hardware, or as a combination of processing hardware and machine-readable instructions executable on the processing hardware.

[0038] In examples where the controllers are implemented as combinations of hardware and machine-readable instructions, the machine-readable instructions can be stored in respective non-transitory computer-readable or machine-readable storage media. The storage media can include one or multiple different forms of

memory including semiconductor memory devices such as dynamic or static random access memories (DRAMs or SRAMs), erasable and programmable read-only memories (EPROMs), electrically erasable and programmable read-only memories (EEPROMs) and flash memories; magnetic disks such as fixed, floppy and removable disks; other magnetic media including tape; optical media such as compact disks (CDs) or digital video disks (DVDs); or other types of storage devices. Note that the instructions discussed above can be provided on one computer-readable or machine-readable storage medium, or alternatively, can be provided on multiple computer-readable or machine-readable storage media distributed in a large system having possibly plural nodes. Such computer-readable or machine-readable storage medium or media is (are) considered to be part of an article (or article of manufacture). An article or article of manufacture can refer to any manufactured single component or multiple components. The storage medium or media can be located either in the machine running the machine-readable instructions, or located at a remote site from which machine-readable instructions can be downloaded over a network for execution.

[0039] In the foregoing description, numerous details are set forth to provide an understanding of the subject disclosed herein. However, implementations may be practiced without some of these details. Other implementations may include modifications and variations from the details discussed above. It is intended that the appended claims cover such modifications and variations.

What is claimed is:

1. A memory device comprising:
storage locations to store data;
an internal controller to perform scrubbing of a portion of the data stored by at least one storage location of the storage locations, the scrubbing comprising reading the portion of the data, detecting and correcting an error in the portion of the data to produce a corrected data portion, and writing the corrected data portion to the at least one storage location; and
an interface to communicate non-deterministically over a communication bus with a memory controller, wherein the memory device is to provide a response through the interface to a memory access command from the memory controller in a non-deterministic amount of time.

2. The memory device of claim 1, wherein the internal controller is to perform the scrubbing in response to the memory device having been idle for a predetermined amount of time.

3. The memory device of claim 1, further comprising:
a refresh controller to perform self-refresh of the storage locations without receiving any refresh instruction from the memory controller that manages access of the memory device.

4. The memory device of claim 3, wherein the internal controller is to perform the scrubbing in conjunction with the self-refresh performed by the refresh controller.

5. The memory device of claim 4, wherein the refresh controller is to initiate the self-refresh in response to the memory device having been idle for a predetermined amount of time.

6. The memory device of claim 1, wherein the storage locations further store error correction code (ECC) information provided by an external memory controller and useable by the external memory controller to perform error detection and correction of the data stored in the storage locations.

7. The memory device of claim 6, further comprising a storage region in the memory device to store scrubbing ECC information, wherein the internal controller is to use the scrubbing ECC information to perform the scrubbing.

8. The memory device of claim 1, wherein the internal controller is to adjust a rate of the scrubbing according to a detected temperature of the memory device.

9. The memory device of claim 1, further comprising:

a self-training controller to perform self-training on the communication bus to determine signal timings and voltages on the communication bus.

10. A method comprising:

initiating, by a memory device without any scrubbing instruction from an external memory controller, scrubbing of data stored in the memory device;

receiving, by the memory device, a memory access command from the external memory controller over a communication bus; and

responding, by the memory device, over the communication bus to the memory access command in a non-deterministic amount of time.

11. The method of claim 10, further comprising:

detecting, by the memory device, that the memory device has been idle for a predetermined amount of time,

wherein initiating the scrubbing is in response to the detecting.

12. The method of claim 10, further comprising:

using error correction code stored in the memory device when performing the scrubbing.

13. The method of claim 12, wherein the memory access command is a read command, and wherein responding to the memory access command comprises sending, by the memory device to the external memory controller, data read from storage locations of the memory device and error correction code (ECC) information from the storage locations.

14. An electronic device comprising:

a memory device comprising a storage array to store data; and

a memory controller external of the memory device and to manage access of the memory device over a communication bus,

the memory device comprising:

an internal controller to control scrubbing of the storage array using error correction code (ECC) information stored in the memory device, and

an interface to communicate non-deterministically over the communication bus with the memory controller, wherein the memory device is to provide a response through the interface to a memory access request from the memory controller in a non-deterministic amount of time.

15. The electronic device of claim 14, wherein the memory controller is to receive a memory access request from a requester, and to issue a memory access command to the memory device in response to the received memory access request.

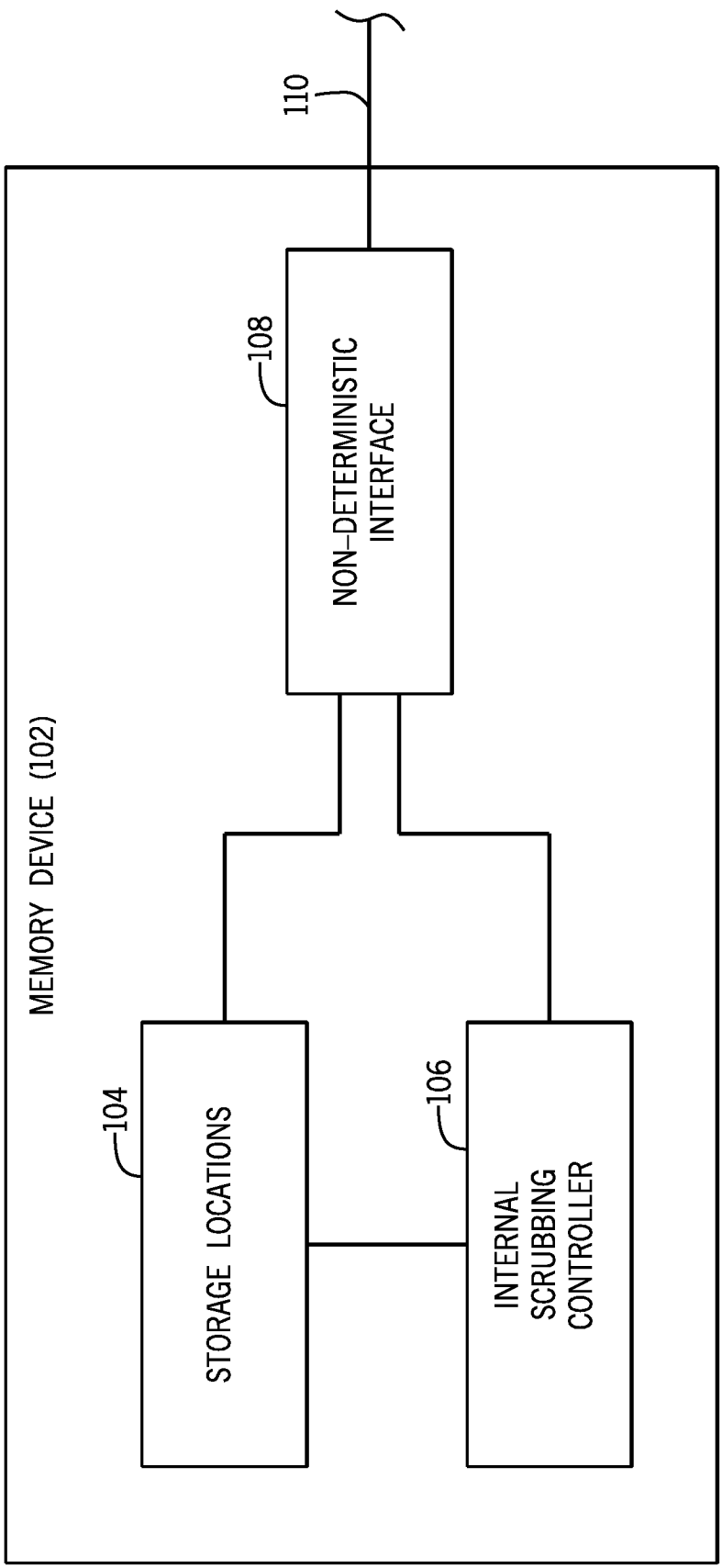
110
MEMORY DEVICE (102)
108
NON-DETERMINISTIC INTERFACE
104
STORAGE LOCATIONS
106
INTERNAL SCRUBBING CONTROLLER

FIG. 1

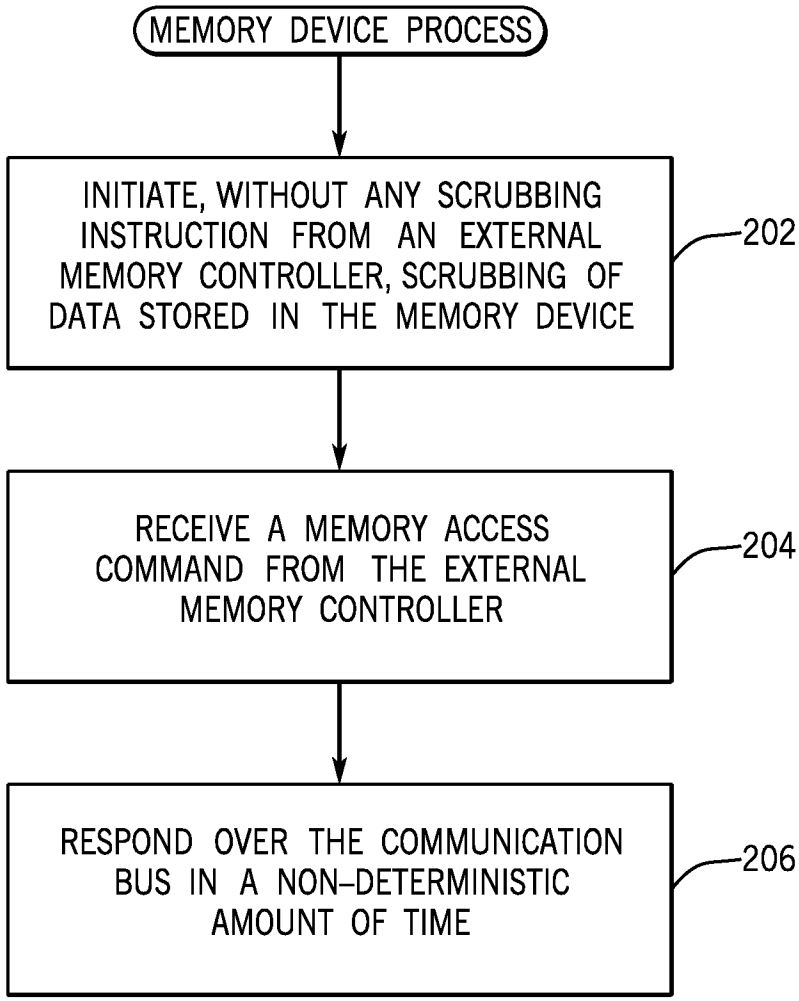
MEMORY DEVICE PROCESS
INITIATE, WITHOUT ANY SCRUBBING INSTRUCTION FROM AN EXTERNAL MEMORY CONTROLLER, SCRUBBING OF DATA STORED IN THE MEMORY DEVICE
202
RECEIVE A MEMORY ACCESS COMMAND FROM THE EXTERNAL MEMORY CONTROLLER
204
RESPOND OVER THE COMMUNICATION BUS IN A NON-DETERMINISTIC AMOUNT OF TIME
206

FIG. 2

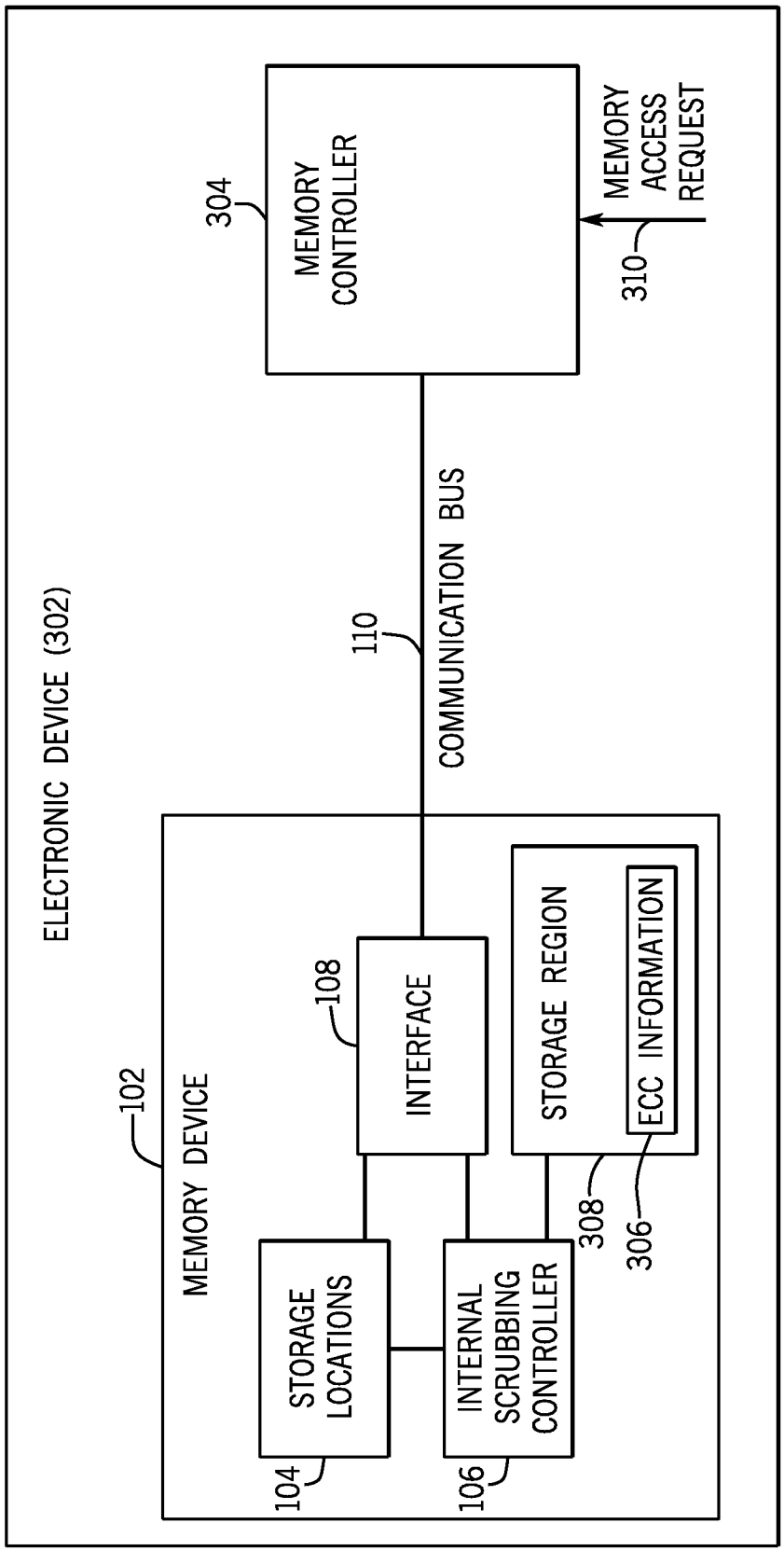
ELECTRONIC DEVICE (302)
304
MEMORY CONTROLLER
MEMORY ACCESS REQUEST
310
110
COMMUNICATION BUS
102
MEMORY DEVICE
108
INTERFACE
STORAGE REGION
ECC INFORMATION
308
306
STORAGE LOCATIONS
INTERNAL SCRUBBING CONTROLLER
104
106

FIG. 3

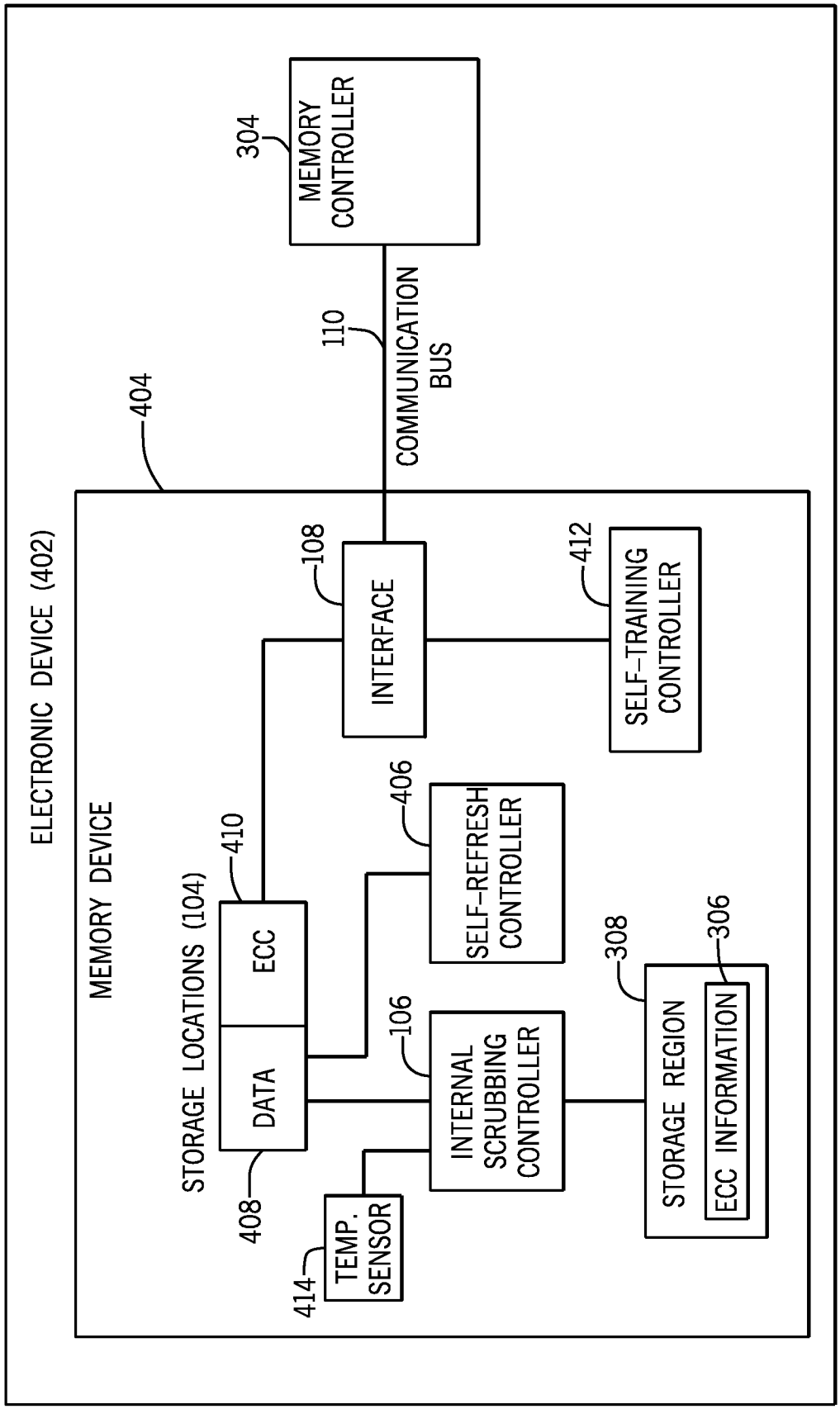
ELECTRONIC DEVICE (402)
MEMORY DEVICE
404
304
MEMORY CONTROLLER
110
COMMUNICATION BUS
108
INTERFACE
412
SELF-TRAINING CONTROLLER
406
SELF-REFRESH CONTROLLER
410
ECC
STORAGE LOCATIONS (104)
DATA
106
INTERNAL SCRUBBING CONTROLLER
308
STORAGE REGION
306
ECC INFORMATION
408
414
TEMP. SENSOR

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/055976

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/406(2006.01)i, G06F 11/10(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 11/406; G06F 12/16; G06F 12/00; G06F 12/04; G11C 29/00; G06F 11/00; G06F 11/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: storage, location, data, controller, scrubbing, reading, detecting, correcting, writing, interface, communicate, non-deterministic, access, command, time, memory

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004-0243886 A1 (DEAN A. KLEIN) 02 December 2004 See paragraphs [0004], [0019]-[0020], [0028], [0035]-[0036], [0042], [0045]-[0046]; and figures 1-7.	1-15
Y	US 2008-0082766 A1 (KENNETH A. OKIN et al.) 03 April 2008 See paragraph [0059]; and figure 6A.	1-15
A	US 2008-0177929 A1 (KEVIN C. GOWER et al.) 24 July 2008 See paragraph [0034]; and figure 8.	1-15
A	US 2003-0009721 A1 (LOUIS L. HSU et al.) 09 January 2003 See paragraphs [0006]-[0007]; and figure 2.	1-15
A	US 2013-0139008 A1 (VYDHYANATHAN KALYANASUNDHARAM et al.) 30 May 2013 See paragraphs [0016]-[0022]; and figure 1.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 July 2016 (14.07.2016)	**15 July 2016 (15.07.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
BYUN, Sung Cheal
Telephone No. +82-42-481-8262

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/055976

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