



- (51) **International Patent Classification:**
H03H 3/02 (2006.01) *H03H 9/54* (2006.01)
H03H 9/05 (2006.01) *H03H 9/56* (2006.01)
- (21) **International Application Number:** PCT/IB2016/051927
- (22) **International Filing Date:** 5 April 2016 (05.04.2016)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:** 62/299,339 24 February 2016 (24.02.2016) US
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- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

— with international search report (Art. 21(3))

(54) **Title:** BAND REJECT FILTERS

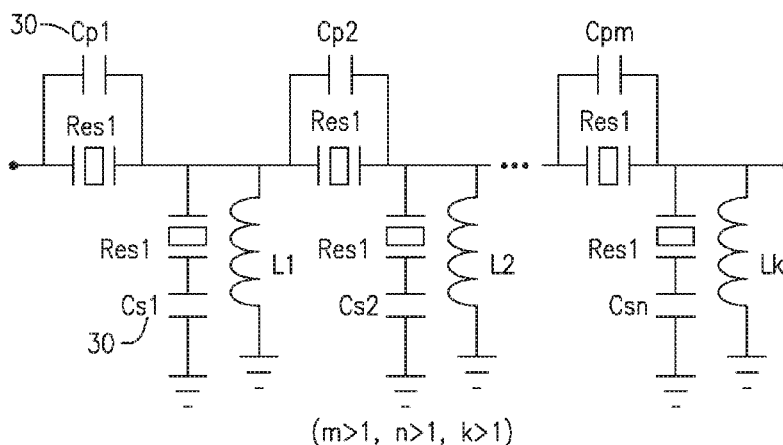


FIG. 6

(57) **Abstract:** A method and a band reject filter (BRF) using as acoustic resonators at least one of bulk acoustic wave (BAW) resonators and film bulk acoustic resonators (FBAR) are provided. The BRF includes at least one substrate having at least one of a plurality of capacitors formed thereon, the plurality of capacitors having capacitances selected to achieve a particular band reject response. The BRF also includes at least one die. At least one of a plurality of acoustic wave resonators are formed thereon. The plurality of acoustic wave resonators are one of BAW resonators and FBARs and are designed to have the same resonant frequency. A plurality of conductors between the substrate and the die are positioned to electrically connect the acoustic wave resonators and the capacitors.

WO 2017/144956 A1

BAND REJECT FILTERS

TECHNICAL FIELD

This disclosure relates to band reject filters.

BACKGROUND

Band reject filters (BRFs) are used in devices such as wireless networks base stations and wireless devices to combat interference encountered on co-location/co-site radio deployments, as well as on multi-band radio designs. In particular, demand for BRFs that are small in size, light in weight and low in cost is very strong, because of interference that occurs in cell networks such as fourth generation (4G) small cell networks.

Typically, BRFs used to mitigate interference require a steep transition band between the passband and the reject band. To achieve BRFs with such steep transition bands, a high Q resonator is desired. Surface acoustic wave (SAW) resonators have a relatively high Q of about 1000 around a 1 giga-Hertz (GHz) resonance frequency. The Q of a SAW resonator drops to about 500 when its resonance frequency is up to 2 GHz. Since a Q of 500 is not high enough to meet BRF filtering requirements in wireless networks applications, the SAW resonator-based BRF is useful to counter interference within a frequency range of 0.5 to 1.5 GHz.

Bulk acoustic wave (BAW) resonators and film bulk acoustic resonators (FBAR) are high Q devices that may be used in BRFs. They have much higher Q than SAW resonators. For example, a BAW resonator or FBAR may have a Q as high as 3000 at 2 GHz, and even show a Q of about 2000 at a frequency of 3 GHz. Thus, from the standpoint of high Q, both the BAW resonator and the FBAR are desirable.

However, the BAW resonator and the FBAR have very complicated manufacturing processes in comparison to a SAW resonator and are up to 50-100 times more expensive to design than SAW resonators. Such large expense is a chief reason why BAW resonators and FBARs are not widely used in wireless networks base stations designs because of their small amount of needs.

SUMMARY

Some embodiments advantageously provide band reject filters and the design thereof. According to one aspect, a band reject filter (BRF) using as acoustic resonators at least one of bulk acoustic wave (BAW) resonators and film bulk acoustic resonators (FBAR) is provided. The BRF includes at least one substrate having at least one of a plurality of capacitors formed thereon, the plurality of capacitors having capacitances selected to achieve a particular band reject response. The BRF also includes at least one die. At least one of a plurality of acoustic wave resonators are formed on the at least one die. Each of the plurality of acoustic wave resonators are one of BAW resonators and FBARs and designed to have the same resonant frequency. A plurality of conductors between the at least one substrate and the at least one die are positioned to electrically connect the acoustic wave resonators and the capacitors.

According to this aspect, in some embodiments, the at least one substrate, the at least one die, acoustic wave resonators, capacitors and conductors are enclosed in a sealed package. In some embodiments, the conductors are solder balls or gold bumps. In some embodiments, there are n resonators electrically in parallel and there are m resonators electrically in series, n and m being integers. In some embodiments, each of the n resonators are electrically in series with a capacitor. In some embodiments, each of the m resonators are electrically in parallel with a capacitor. In some embodiments, the BRF includes a plurality of inductors electrically in parallel with the n resonators. In some embodiments, each of the plurality of capacitors is an interdigital-type capacitor with a number of fingers selected to adjust a capacitance of the capacitor. In some embodiments, the capacitances are chosen to compensate for a deviation of an acoustic wave resonator from the designed resonant frequency.

According to another aspect, a band reject filter IC is provided. The BRF includes at least one die. The BRF also includes a plurality of acoustic wave resonators, the plurality of acoustic wave resonators being one of BAW, resonators and FBARs. The plurality of acoustic wave resonators are formed on the at least one die and are designed to have the same resonant frequency. The BRF also includes at least one substrate and formed on the at least one substrate, a plurality of capacitors, the plurality of capacitors having capacitances selected to achieve a particular band

reject response. Electrical conductors positioned between the at least one die and the at least one substrate electrically connect the capacitors on the at least one substrate to at least one acoustic wave resonators on the at least one die.

According to this aspect, in some embodiments, the at least one substrate, the
5 at least one die, the acoustic wave resonators and the conductors are enclosed in a sealed package. In some embodiments, the conductors are solder balls or gold bumps. In some embodiments, are n resonators electrically in parallel and there are m resonators electrically in series, n and m being integers. In some embodiments, each of the n resonators are electrically in series with a capacitor. In some embodiments,
10 each of the m resonators are electrically in parallel with a capacitor. In some embodiments, the BRF IC includes a plurality of inductors electrically in parallel with the n resonators. In some embodiments, each of the plurality of capacitors is an interdigital-type capacitor with a number of fingers selected to adjust a capacitance of the capacitor. In some embodiments, the capacitances are chosen to compensate for a
15 deviation of an acoustic wave resonator from the designed resonant frequency

According to yet another aspect, a method of manufacturing a band reject filter, BRF, is provided. The method includes forming a plurality of acoustic wave resonators on a die, each of the plurality of acoustic resonators being designed to have the same resonant frequency, each acoustic wave resonator being one of bulk acoustic
20 wave, BAW, resonators and film bulk acoustic resonators, FBAR. Capacitors are formed on a substrate. The capacitors have capacitances chosen to achieve a particular band reject response. A flip-chip manufacturing technique is employed to mate the die and the substrate with solder balls or gold bumps to electrically connect the capacitors on the substrate to at least one corresponding acoustic resonator on the
25 die.

According to this aspect, the method also includes sealing the die, the substrate, the acoustic wave resonators and the capacitors in an integrated circuit package. In some embodiments, each of the plurality of capacitors is an interdigital-type capacitor with a number of fingers selected to adjust a capacitance of the
30 capacitor. In some embodiments, the method further includes packaging the at least one substrate, the at least one die, acoustic wave resonators, capacitors and conductors in a sealed integrated circuit package. In some embodiments, the capacitances are

chosen to compensate for a deviation of an acoustic wave resonator from the designed resonant frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

5 A more complete understanding of the present embodiments, and the attendant advantages and features thereof, will be more readily understood by reference to the following detailed description when considered in conjunction with the accompanying drawings wherein:

FIG. 1 is a schematic diagram of a known band reject filter (BRF);

10 FIG. 2 is a graph of band reject responses for the BRFs shown in FIGS. 1 and 3;

FIG. 3 is a schematic diagram of a known BRF with tuning capacitors;

FIG. 4 is a schematic of a known BRF having six differently designed acoustic resonators;

15 FIG. 5 is an illustration of a known package including the six differently designed acoustic resonators;

FIG. 6 is a schematic diagram of a BRF according to methods presented herein;

FIG. 7 is an illustration of a BRF package according to methods described herein;

FIG. 8 is an illustration of an assembly of a BRF using a flip-chip technology according to methods described herein;

20 FIG. 9 is an illustration of interdigital capacitors on a substrate that may be integrated with a BRF according to method described herein;

FIG. 10 is a schematic diagram of a BRF according to method presented herein;

FIG. 11 is a graph of two band reject responses resulting from two different BRF designs using the same resonators; and

25 FIG. 12 is a flowchart of an exemplary process for design of a BRF according to methods described herein.

DETAILED DESCRIPTION

Before describing in detail exemplary embodiments, it is noted that the embodiments reside primarily in combinations of apparatus components and processing steps related to band reject filter implementation. Accordingly, components have been represented where appropriate by conventional symbols in the drawings, showing only those specific details that are pertinent to understanding the embodiments so as not to obscure the disclosure with details that will be readily apparent to those of ordinary skill in the art having the benefit of the description herein.

As used herein, relational terms, such as “first” and “second,” “top” and “bottom,” and the like, may be used solely to distinguish one entity or element from another entity or element without necessarily requiring or implying any physical or logical relationship or order between such entities or elements.

FIG. 1 is a schematic diagram of a typical BRF design using acoustic resonators. Each of the three different resonators of FIG. 1 is designed to have a different resonance frequency to form the width of the band reject region, as shown in FIG. 2 curve 10. For a BAW resonator or an FBAR, a different resonance frequency means a different design for each resonator. A different design requires a different combination of thicknesses of an active piezoelectric layer and mass loading metal layer. To change the thickness of these layers, a certain number of processing steps in sequence are needed for the manufacture of the resonator, which results in increased cost.

Currently, only one piezoelectric material is used for the design of BAW resonators and FBARs, which is aluminum nitride (AlN). Such resonators have an electromechanical coupling coefficient of about 6 or 6.5%. For some BRF designs, such values are too high and must be reduced by use of capacitors, so that a sharp transition band can be designed. This is shown in FIG. 3 where capacitors, Cp1 and

Cp2, are placed in parallel with the two series resonators, Res1 and Res3, and a capacitor, Cs1, is placed in series with the parallel resonator, Res2.

As shown in FIG. 2, curve 10, the stopband region of the BRF band reject response of the circuit of FIG. 1 has three valleys, one for each of the three different resonators of the BRF of FIG. 1. A sharper transition region can be achieved using the capacitors shown in the circuit of FIG. 3. This sharper transition region is shown as curve 12 of FIG. 2. Note that in FIG. 2, the area 11 between the shaded regions is a transition region of the band reject response.

A more general BRF design is shown in FIG. 4. The design shown in FIG. 4 has six different resonators and six capacitors. As shown in FIG. 5, conventionally, the six resonators are included in a package and the capacitors and matching inductors are added as peripheral components outside the package. The placement of the capacitors peripheral to the package results in the consumption of large spaces of the printed circuit board on which the package is placed.

In summary, conventional designs using BAW resonators and FBARs are expensive, involving the design of many different resonators, and use of large board space for peripheral components. Also, since the placement of the different resonant frequencies of the resonators may be critical, repeated manufacture may be required to achieve a critical resonant frequency and/or transition region, thereby increasing the cost of manufacture even further.

To address the above, embodiments of the present disclosure provide BRFs using BAW resonators and FBARs, and design methodologies for the design of BRFs using BAW resonators and FBARs, which reduce design costs, manufacturing costs and size as compared with known BRFs. FIG. 6 is a schematic of a design in which all the acoustic resonators are designed to have the same resonant frequency. Rather than design a different resonator for each resonator section of the BRF circuit to achieve different valleys within the band reject region, each of the resonators, Res1, of the BRF are designed to resonate at the same frequency, and the width of the band reject region is achieved by selection of the capacitors Cp1-Cpm and Cs1-Csn, where there are m series resonators and n parallel resonators. Each of the m series resonators has a capacitor Cp electrically in parallel with the corresponding resonator and each of the n parallel resonators has a capacitor Cs electrically in series with the

corresponding resonator. Capacitors C_p and C_s are referred to herein collectively as capacitors 30.

By using the same design for each resonator in the BRF, substantial design and manufacturing costs may be avoided. The capacitances of the capacitors may be chosen to compensate for a deviation of an acoustic wave resonator from the designed resonant frequency. In some embodiments, each capacitor may be an interdigital-type capacitor with a number of fingers selected to adjust a capacitance of the capacitor. In some embodiments, the capacitors are formed on a high Q substrate.

FIG. 7 is an illustration of a BRF in a BRF package 18 that includes not only the $n+m$ resonators having the same design, but also include the $n+m$ capacitors as well. Including the capacitors in the BRF package 18 with the resonators substantially reduces the amount of board space utilized for peripheral components. Note that the matching inductors 19 remain outside the BRF package 18 in some embodiments. In one embodiment, the BRF package is an integrated circuit (IC), also referred to herein as a BRF IC.

FIG. 8 is an illustration of an example showing how the resonators and capacitors may be integrated in the same BRF package 18 using flip chip technology. All of the resonators 21 in the BRF package 18 may be formed on a single die 20, and all of the capacitors 23 may be formed on a single substrate 22. Connections between the capacitors 23 and resonators 21 may be formed using metal bumps 24, which may be solder balls or gold bumps, for example. Note that an exterior surface of the die 20 or the substrate 22 may form a surface of the BRF package 18 or the entire die 20 and/or substrate 22 may be fully enclosed within the BRF package 18.

Thus, some embodiments include a BRF using as acoustic resonators at least one of BAW resonators and FBARs. The BRF includes a substrate and a die. A plurality of acoustic wave resonators are formed on the die. The plurality of acoustic resonators are of the same designed resonant frequency. A plurality of capacitors are formed on the substrate. The plurality of capacitors have capacitances selected to achieve a particular band reject response. Electrical conductors, such as metal bumps or solder balls or gold bumps lie between the die and the substrate and are positioned to electrically connect the acoustic wave resonators and the capacitors. In one embodiment, the components of the BRF may be a sealed package such as in an

integrated circuit (IC) package. In some embodiments, the acoustic wave resonators may be formed on more than one die, and the capacitors may be formed on more than one substrate. The acoustic wave resonators, the capacitors, the substrate(s) and the die(s) may be packaged in a sealed integrated circuit package.

5 FIG. 9 is an illustration of capacitors 30 formed on a dielectric substrate 22 such as an alumina substrate, Al₂O₃, or single crystal or multi-crystal substrates such as Quartz, LiNbO₃, LiTaO₃, sapphire, silicon, as well as some printed circuit board (PCB) materials such as FR-4 and Rogers, etc. In one embodiment, the dielectric materials used may have small loss tangent to allow the capacitors to have Q values
10 high enough to achieve a desired band reject transition region. Note that the capacitors may be aligned symmetrically or placed in an asymmetric pattern, as desired.

 Electrode patterns of the capacitors 30 (Cp1 . . . Cpm and Cs1 . . . Csn) on the substrate 22 may be any shape but an interdigital pattern as shown in FIG. 9 may be
15 used. This type of capacitor can be manufactured to within 0.01 pico-Farad (pF) of capacitance. The interlaced fingers of the interdigital capacitor 30 may have any desired pitch (spacing) except that when a SAW substrate, such as, quartz or LiTaO₃ is used, the pitch of the interdigital capacitor should be a value that is substantially different from a value of $p=v/(2f_0)$, where v is velocity of propagation of the SAW
20 (surface acoustic wave) along a direction perpendicular to the fingers of the interdigital capacitor and f₀ is the center frequency of the reject band of the BRF. This condition avoids generation of a surface acoustic wave on the substrate when signals within the reject band are passing through the capacitor.

 FIG. 10 is a schematic diagram of a BRF with three resonators 32a, 32b and
25 32c (collectively “resonators 32”), all designed to have the same resonant frequency. Electrically parallel with the series resonators 32b and 32c are capacitors 30b and 30c. In electrical series with the electrically parallel resonator 32a is a capacitor 30a. Electrically in parallel with the electrically parallel resonator 32a is a matching inductor 40. Of course, implementations are not limited to the arrangement shown in
30 FIG. 10. Other quantities of resonators and capacitors may be used. FIG. 11 is a graph of two band reject responses 42 and 44. Response 42 corresponds to the circuit of FIG. 10 when the components have the following values:

$$C_{p1}=1.28\text{pF}, C_{p2}=1.60\text{pF}, C_{s1}=0.70\text{pF}, L1=4.3\text{nH}$$

Response 44 corresponds to the circuit of FIG. 10 when the components have the following values:

$$C_{p1}=0.73\text{pF}, C_{p2}=1.04\text{pF}, C_{s1}=0.46\text{pF}, L1=4.3\text{nH}$$

5 Note that in FIG. 11, the area between the shaded regions is a transition region 45 of the band reject responses 42 and 44. Note also that the values of the capacitances and inductor are not difficult to achieve. In particular, the capacitors may be formed using photolithography.

FIGS. 10 and 11 show that the same resonators Res1 with different
10 capacitances can achieve quite different band reject responses. In other words, all the resonators can be designed to have the same resonant frequencies and the valleys in the band reject response can be adjusted by varying the capacitors of the circuit. Thus, not only is the cost of design reduced because the same design can be used for all the resonators, but the manufacturing tolerances on the resonator design may not
15 be critical since the response can be fine-tuned by varying the capacitors. Implementing capacitors of varied capacitances can be done at a low cost.

Therefore, embodiments include a method of manufacturing a band reject filter using BAW resonators or FBARs that is simple and low in cost. First, a plurality of acoustic wave resonators are formed on a die. Each of the resonators are
20 of a same design, namely designed to have a same resonant frequency. Capacitors are chosen having capacitances to achieve a particular band reject response. Capacitors having the chosen capacitances are formed on a substrate. Flip chip technology can be used to mate the die and the substrate with solder balls or gold bumps forming connections between the capacitors and the acoustic resonators. The assembled die
25 and substrate can be enclosed in a sealed integrated circuit (IC) package.

FIG. 12 is a flowchart of an exemplary process for manufacturing a band reject filter, BRF, using acoustic wave resonators chosen from a group consisting of bulk acoustic wave, BAW, resonators and film bulk acoustic resonators, FBAR. The method includes forming a plurality of acoustic wave resonators on a die, each of the
30 plurality of acoustic resonators having the same resonant frequency (block S100). The capacitors are formed on a substrate and have a predetermined capacitance chosen to achieve a particulate band reject response (block S102). A flip-chip

manufacturing technique is employed to mate the die and the substrate with solder balls or gold bumps to electrically connect the capacitors on the substrate to at least one acoustic resonator on the die (block S108).

The embodiments described herein enable a filter designer to design a
5 relatively low-cost BRF using BAW resonators or FBARs with a short design time. The BRFs described herein can be used in embodiments such as base stations and hand held wireless devices. Since BRFs using BAW resonators and FBARs have much better filtering performance than SAW resonators, BRFs using BAW resonators and FBARs can be expected to help network operators use their valuable spectrum
10 resources more efficiently.

As will be appreciated by one of skill in the art, the concepts described herein may be embodied as a method, data processing system, and/or computer program product. Accordingly, the concepts described herein may take the form of an entirely hardware embodiment, an entirely software embodiment or an embodiment
15 combining software and hardware aspects all generally referred to herein as a “circuit” or “module.” Furthermore, the disclosure may take the form of a computer program product on a tangible computer usable storage medium having computer program code embodied in the medium that can be executed by a computer. Any suitable tangible computer readable medium may be utilized including hard disks,
20 CD-ROMs, electronic storage devices, optical storage devices, or magnetic storage devices.

Some embodiments are described herein with reference to flowchart illustrations and/or block diagrams of methods, systems and computer program products. It will be understood that each block of the flowchart illustrations and/or
25 block diagrams, and combinations of blocks in the flowchart illustrations and/or block diagrams, can be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the
30 computer or other programmable data processing apparatus, create means for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks.

These computer program instructions may also be stored in a computer readable memory or storage medium that can direct a computer or other programmable data processing apparatus to function in a particular manner, such that the instructions stored in the computer readable memory produce an article of manufacture including instruction means which implement the function/act specified in the flowchart and/or block diagram block or blocks.

The computer program instructions may also be loaded onto a computer or other programmable data processing apparatus to cause a series of operational steps to be performed on the computer or other programmable apparatus to produce a computer implemented process such that the instructions which execute on the computer or other programmable apparatus provide steps for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks.

It is to be understood that the functions/acts noted in the blocks may occur out of the order noted in the operational illustrations. For example, two blocks shown in succession may in fact be executed substantially concurrently or the blocks may sometimes be executed in the reverse order, depending upon the functionality/acts involved. Although some of the diagrams include arrows on communication paths to show a primary direction of communication, it is to be understood that communication may occur in the opposite direction to the depicted arrows.

Computer program code for carrying out operations of the concepts described herein may be written in an object oriented programming language such as Java® or C++. However, the computer program code for carrying out operations of the disclosure may also be written in conventional procedural programming languages, such as the "C" programming language. The program code may execute entirely on the user's computer, partly on the user's computer, as a stand-alone software package, partly on the user's computer and partly on a remote computer or entirely on the remote computer. In the latter scenario, the remote computer may be connected to the user's computer through a local area network (LAN) or a wide area network (WAN), or the connection may be made to an external computer (for example, through the Internet using an Internet Service Provider).

Many different embodiments have been disclosed herein, in connection with the above description and the drawings. It will be understood that it would be unduly

repetitious and obfuscating to literally describe and illustrate every combination and subcombination of these embodiments. Accordingly, all embodiments can be combined in any way and/or combination, and the present specification, including the drawings, shall be construed to constitute a complete written description of all combinations and subcombinations of the embodiments described herein, and of the manner and process of making and using them, and shall support claims to any such combination or subcombination.

It will be appreciated by persons skilled in the art that the embodiments described herein are not limited to what has been particularly shown and described herein above. In addition, unless mention was made above to the contrary, it should be noted that all of the accompanying drawings are not to scale. A variety of modifications and variations are possible in light of the above teachings without departing from the scope of the following claims.

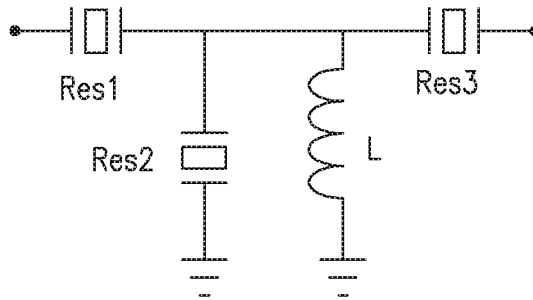
What is claimed is:

1. A band reject filter, BRF, the BRF comprising:
at least one substrate, the at least one substrate having at least one of a
5 plurality of capacitors formed thereon, the plurality of capacitors having capacitances
selected to achieve a particular band reject response;
at least one die, the at least one die having at least one of a plurality of
acoustic wave resonators formed thereon, the plurality of acoustic wave resonators
being one of bulk acoustic wave, BAW, resonators and film bulk acoustic resonators,
10 FBAR, and each of the plurality of acoustic wave resonators being designed to have a
same resonant frequency; and
a plurality of conductors between the at least one substrate and the at least one
die and positioned to electrically connect the acoustic wave resonators and the
capacitors.
15
2. The BRF of Claim 1, wherein the at least one substrate, the at least one die,
acoustic wave resonators, capacitors and conductors are enclosed in a sealed package.
3. The BRF of Claim 1, wherein the conductors are solder balls or gold bumps.
20
4. The BRF of Claim 1, wherein there are n resonators electrically in parallel and
there are m resonators electrically in series, n and m being integers.
5. The BRF of Claim 4, wherein each of the n resonators are electrically in series
25 with a capacitor.
6. The BRF of Claim 4, wherein each of the m resonators are electrically in
parallel with a capacitor.
- 30 7. The BRF of Claim 4, further comprising a plurality of inductors electrically in
parallel with the n resonators.

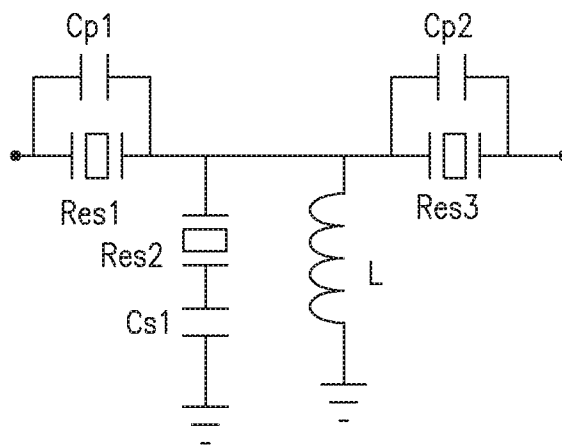
8. The BRF of Claim 1, wherein each of the plurality of capacitors is an interdigital-type capacitor with a number of fingers selected to adjust a capacitance of the capacitor.
- 5 9. The BRF of Claim 1, wherein the capacitances are chosen to compensate for a deviation of an acoustic wave resonator from the designed resonant frequency.
10. A band reject filter, BRF, integrated circuit, IC, comprising:
at least one die;
10 a plurality of acoustic wave resonators, the plurality of acoustic wave resonators being one of bulk acoustic wave, BAW, resonators and film bulk acoustic resonators, FBAR, the plurality of acoustic wave resonators being formed on the at least one die and being designed to have a same resonant frequency;
at least one substrate;
15 a plurality of capacitors, the plurality of capacitors being formed on the at least one substrate and having capacitances selected to achieve a particular band reject response; and
electrical conductors positioned between the at least one die and the at least one substrate, the electrical conductors arranged to electrically connect the capacitors
20 on the at least one substrate to at least one corresponding acoustic wave resonator on the at least one die.
11. The BRF IC of Claim 10, wherein the at least one substrate, the at least one die, the acoustic wave resonators and the conductors are enclosed in a sealed package.
25
12. The BRF IC of Claim 10, wherein the electrical conductors are solder balls or gold bumps.
13. The BRF IC of Claim 10, wherein there are n resonators electrically in parallel
30 and there are m resonators electrically in series, n and m being integers.

14. The BRF IC of Claim 13, wherein each of the n resonators are electrically in series with a capacitor.
15. The BRF IC of Claim 13, wherein each of the m resonators are electrically in parallel with a capacitor.
16. The BRF IC of Claim 13, further comprising a plurality of inductors electrically in parallel with the n resonators.
17. The BRF IC of Claim 10, wherein each of the plurality of capacitors is an interdigital-type capacitor with a number of fingers selected to adjust a capacitance of the capacitor.
18. The BRF IC of Claim 10, wherein the capacitances are chosen to compensate for a deviation of an acoustic wave resonator from the designed resonant frequency.
19. A method of manufacturing a band reject filter, BRF, the method comprising:
forming a plurality of acoustic wave resonators on a die, each of the plurality of acoustic resonators being one of bulk acoustic wave, BAW, resonators and film bulk acoustic resonators, FBAR, each of the acoustic wave resonators being designed to have a same resonant frequency;
forming a plurality of capacitors having predetermined corresponding capacitances on a substrate, the capacitances of capacitors being chosen to achieve a particular band reject response; and
employing a flip-chip manufacturing technique to electrically mate the die and the substrate using solder balls or gold bumps to electrically connect the capacitors on the substrate to at least one corresponding acoustic wave resonator on the die.
20. The method of Claim 19, further comprising sealing the die, the substrate, the acoustic wave resonators and the capacitors in an integrated circuit package.

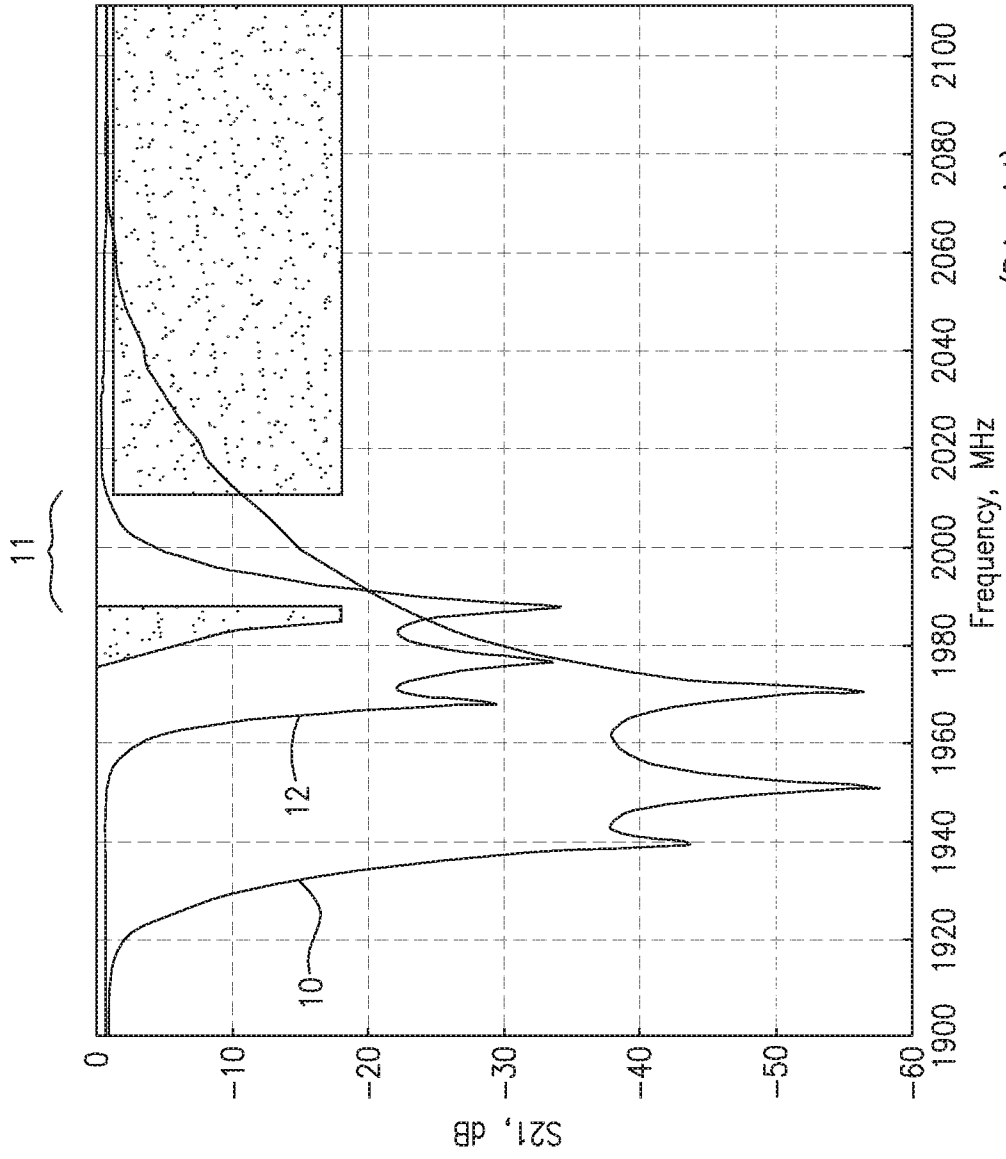
21. The method of Claim 19, wherein each of the plurality of capacitors is an interdigital-type capacitor with a number of fingers selected to adjust a capacitance of the capacitor.
- 5 22. The method of Claim 19, further packaging the at least one substrate, the at least one die, acoustic wave resonators, capacitors and conductors in a sealed integrated circuit package.
23. The method of Claim 19, wherein the capacitances are chosen to compensate
10 for a deviation of an acoustic wave resonator from the designed resonant frequency.



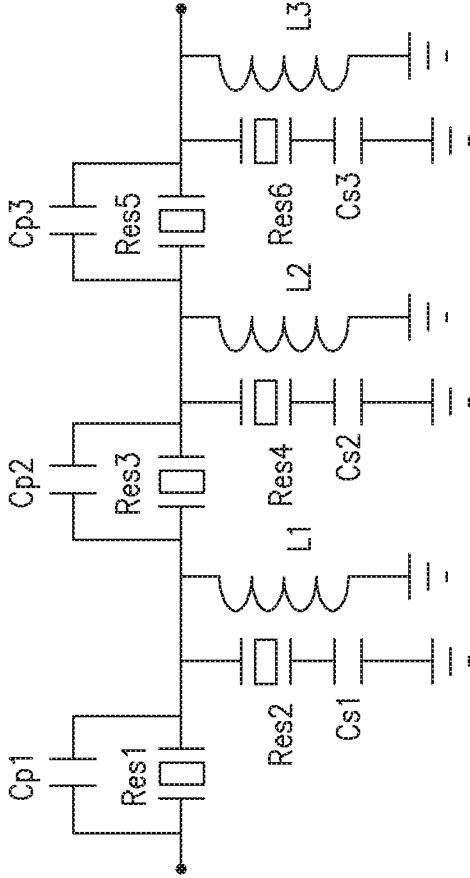
(Prior Art)
FIG. 1



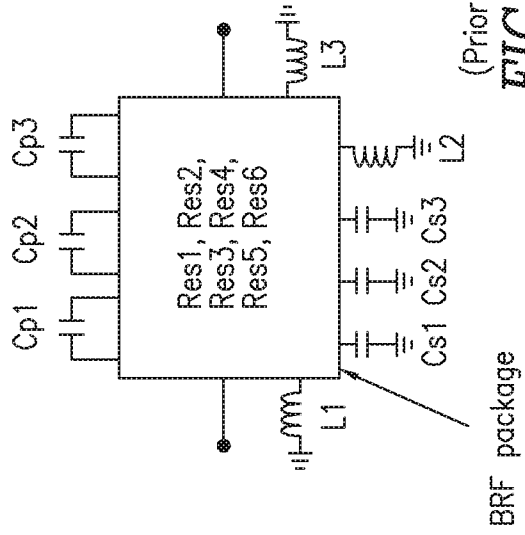
(Prior Art)
FIG. 3



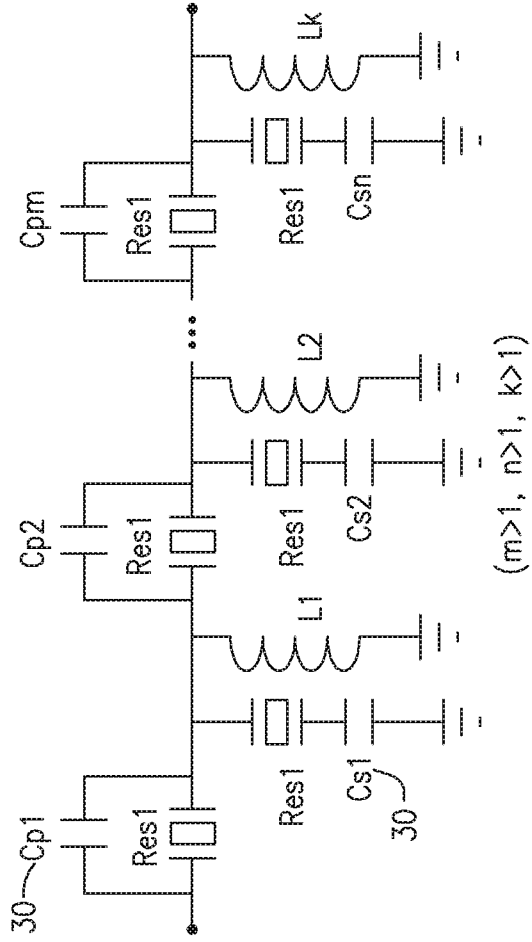
(Prior Art)
FIG. 2



(Prior Art)
FIG. 4

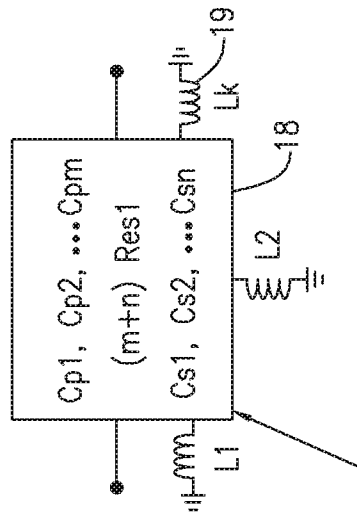


(Prior Art)
FIG. 5



($m > 1, n > 1, k > 1$)

FIG. 6



BRF package

FIG. 7

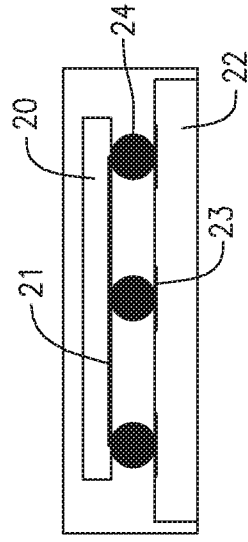


FIG. 8

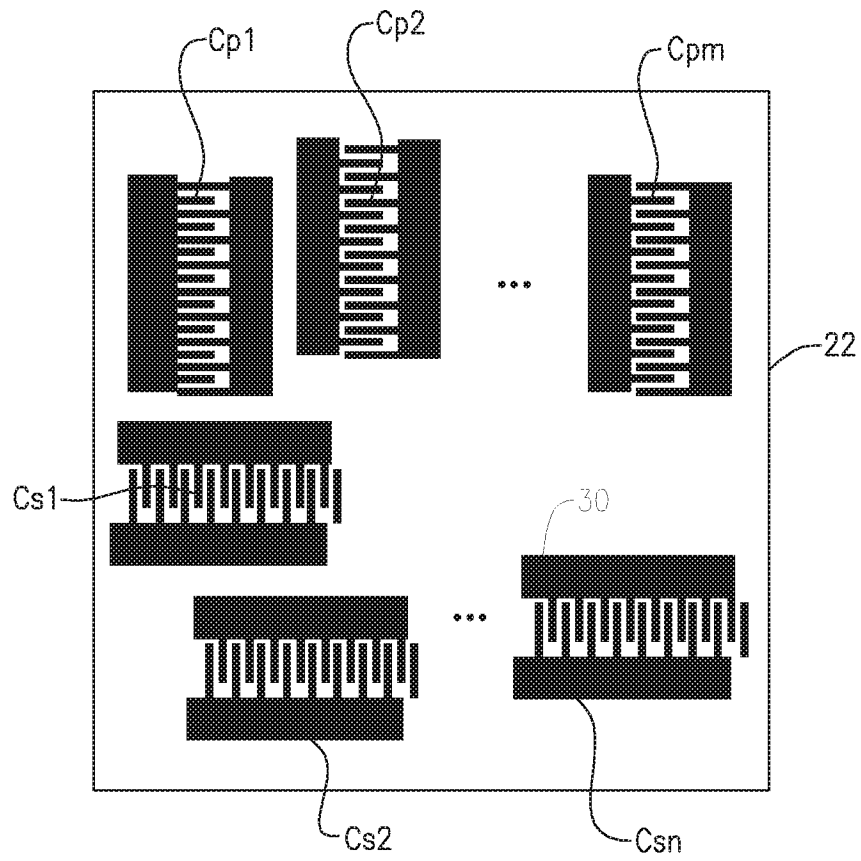


FIG. 9

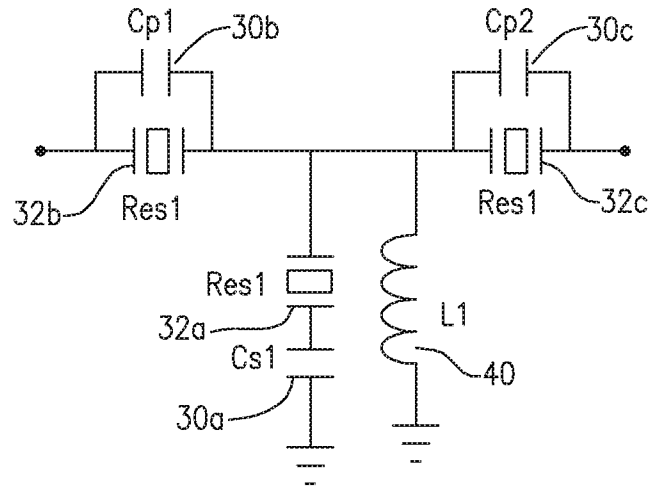


FIG. 10

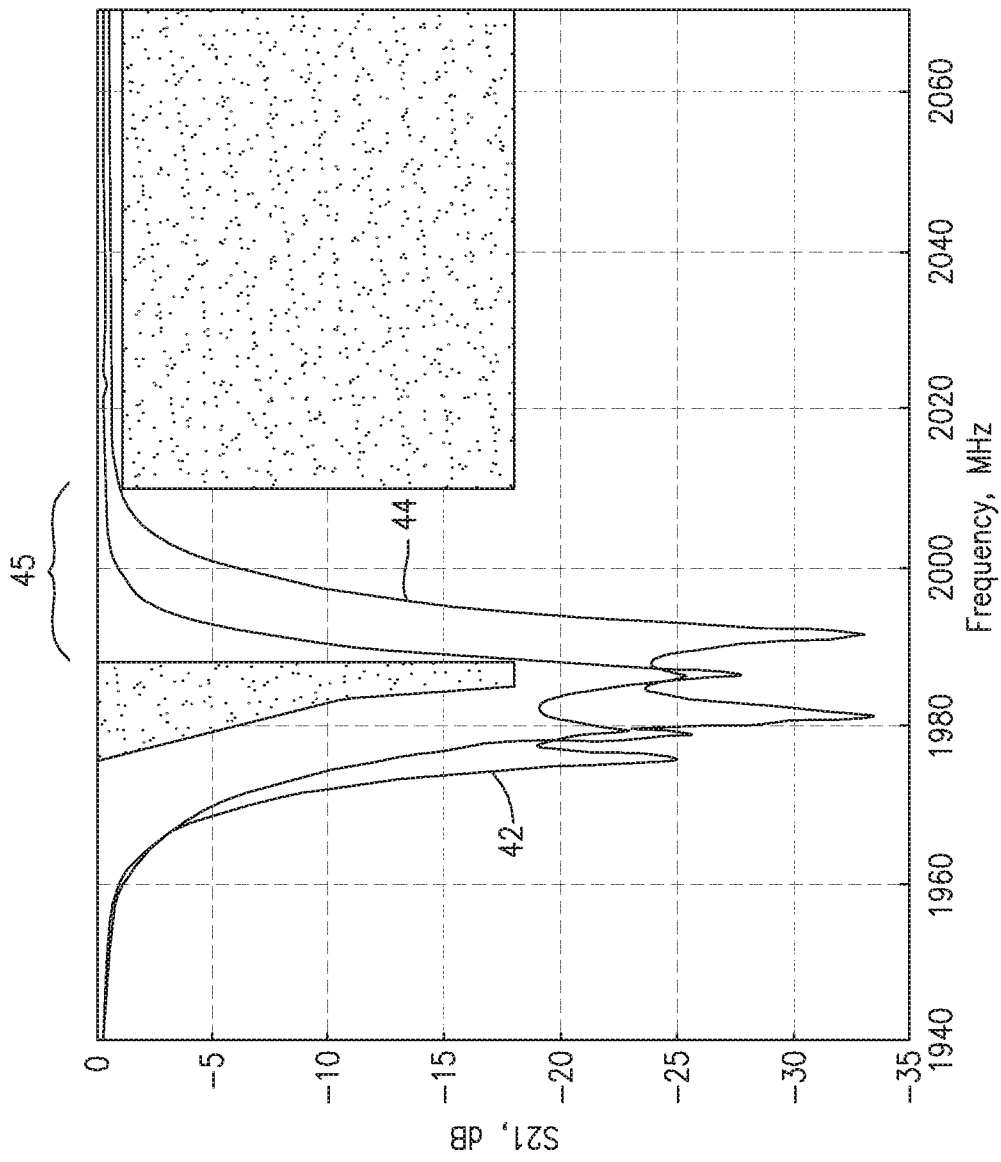
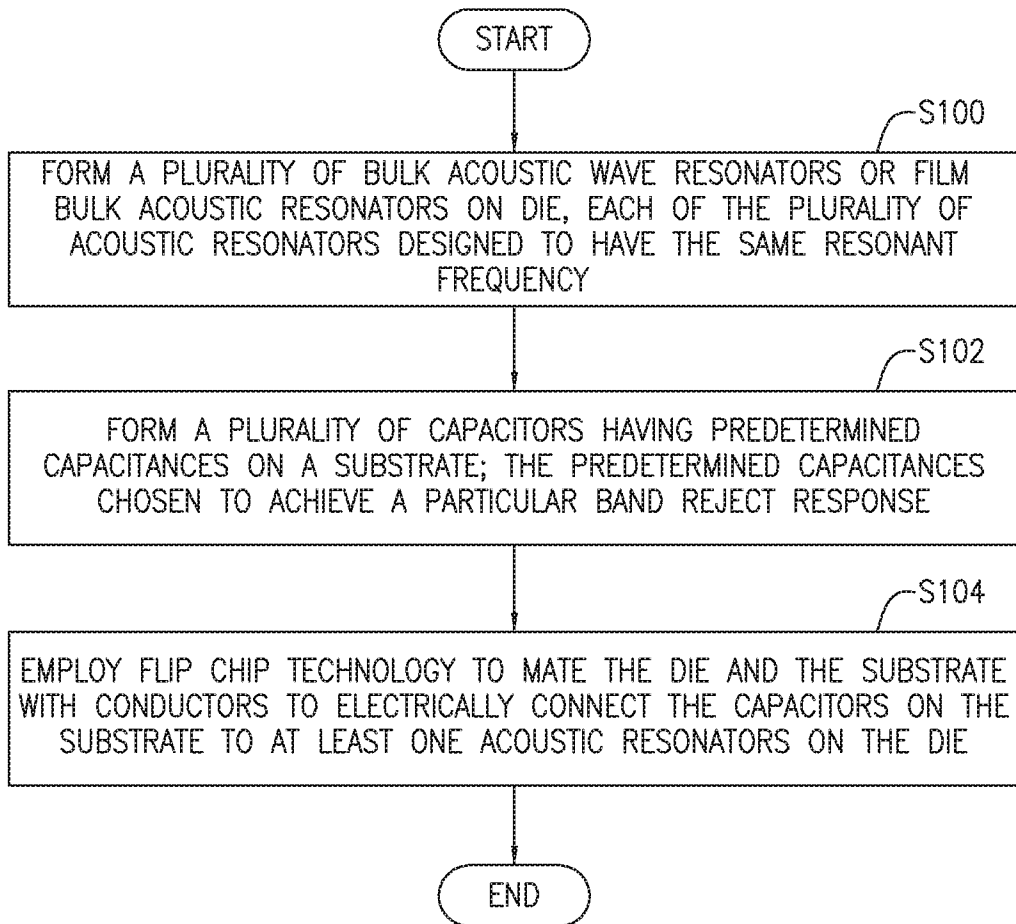


FIG. 11

*FIG. 12*

INTERNATIONAL SEARCH REPORT

International application No PCT/IB2016/051927

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H03H3/02 H03H9/05 H03H9/54 H03H9/56
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	EP 1 398 876 A1 (MATSUSHITA ELECTRIC IND CO LTD [JP]) 17 March 2004 (2004-03-17) paragraph [0080] - paragraph [0087]; figures 13, 14 paragraph [0090] - paragraph [0109]; figures 15 - 17 -----	1-3, 8-12, 17-23 4-7, 13-16
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Further documents are listed in the continuation of Box C.

See patent family annex.

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Date of the actual completion of the international search

10 November 2016

Date of mailing of the international search report

18/11/2016

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	paragraph [0111] - paragraph [0130]; figures 1 - 3, 5 paragraph [0062] - paragraph [0068] -----	4-7, 13-16

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