Dec. 5, 1967 R. R. WALSH 3,357,008

AUTOMATIC ALARM ANNUNCIATOR CIRCUITS

Filed March 17, 1964 2 Sheets-Sheet 1

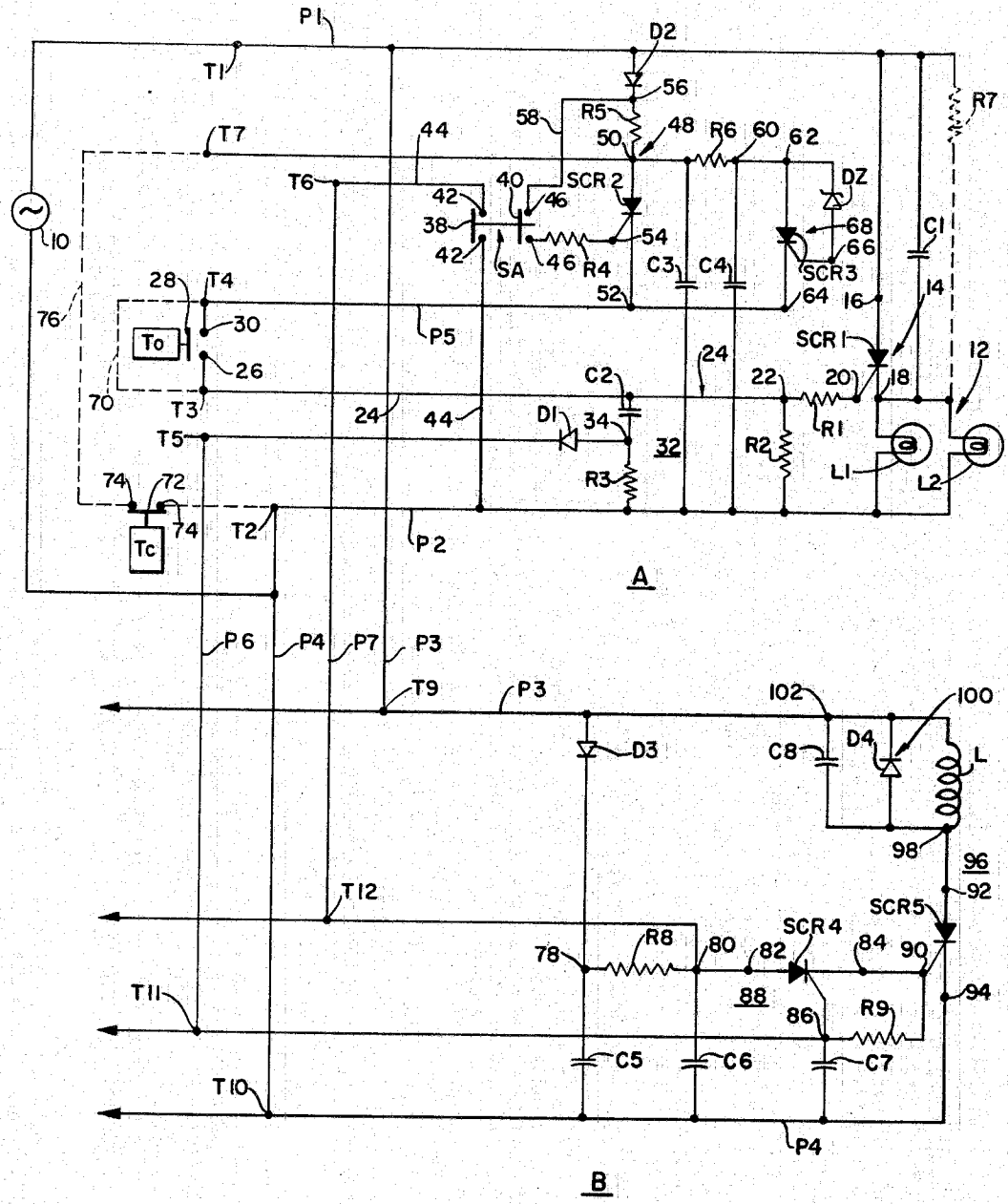


FIG. 1.

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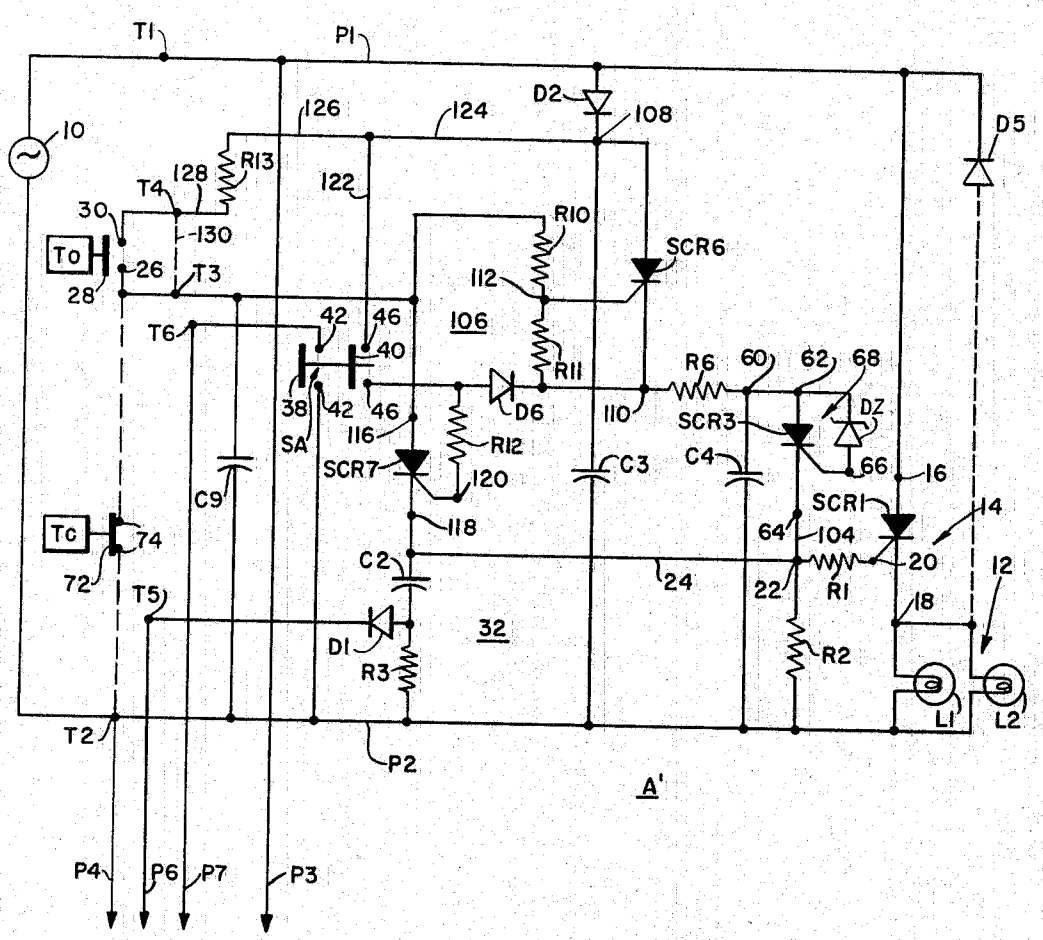


FIG. 2.

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AUTOMATIC ALARM ANNUNCIATOR CIRCUITS

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This relates to automatic alarm annunicator circuits and more particularly to such circuits having silicon controlled rectifiers as the only active element or elements therein.

The circuits comprising the subject matter of this invention are used in applications relating to chemical and other industrial processes for the purpose of monitoring such variable process parameters as temperature, pressure, flow rate, and many others. The transducer means associated with each parameter being monitored usually includes monitoring switches having either normally open or normally closed switch contacts which close or open, respectively, when the parameter being monitored exceeds its normal prescribed limits.

These monitoring switches are each connected with alarm annunicator circuits which provide audible and visual indication at a remote point or points of an abnormal or off-normal condition of a given parameter. The audible signal is of the horn or bell type while the visual signal is preferably a flashing light. The audible signal may be common to all points being monitored in a given process or the like but the visual signals are individually associated with each of the monitoring switches.

Each alarm annunciator circuit is equipped with an "acknowledge" switch at the remote monitoring point which is adapted to be closed by the operating personnel for the purpose of acknowledging the operator's awareness of an abnormal condition. This switch deenergizes the audible alarm and changes the operating format of the visual alarm from flashing to steady for the purpose of indicating that the process is still malfunctioning but that the operating personnel are aware of this condition.

As soon as normal conditions are restored, the visual alarm is restored to the state representing the said normal conditions.

The two generally preferred standards for alarm annunciator circuits in industry are commonly referred to as Sequence A and Sequence B.

In Sequence A operation the "normal" condition is signified by an extinguished visual alarm and a silenced audible alarm; the "abnormal" condition by a flashing visual signal and an energized audible alarm, and the "acknowledge" condition by a steady visual signal and a silenced audible alarm. Sequence B differs only in the provision of a dimly illuminated visual signal in the "normal" condition.

It is an object of this invention to provide new and novel alarm annunciator circuits for both Sequence A and Sequence B operation.

Another object of this invention is to provide new and novel alarm annunciator circuits in which the only active circuit means comprise silicon controlled rectifiers.

Still another object of this invention is to provide new and novel alarm annunciator circuits in which when an "abnormal" condition response is initiated by only a momentary variation at the remote monitoring point, actuation of the acknowledge switch will result in a return of the system to the "normal" state, rather than to a condition in which the visual alarm is constantly energized.

These and other objects of this invention will become more fully apparent with reference to the following specification and drawings which relate to a preferred embodiment of the invention:

In the drawings:

FIGURE 1 is a schematic of an audible and visual alarm annunciator circuit of the present invention; and

FIGURE 2 is a schematic of a second embodiment of the visual alarm and sensing circuit of the present invention.

Referring in detail to FIGURE 1 one embodiment of the alarm annunciator circuit of the present invention is shown as comprising a first visual alarm and sensing circuit A and a second audible alarm circuit B.

The first circuit A is supplied with A.C. power from an A.C. source 10 connected between first and second power leads P1 and P2 via terminals T1 and T2, respectively, P2 being a common or potential reference lead for the first circuit A.

The second circuit B is powered from the A.C. source 10 via first and second extension leads P3 and P4 connected, respectively, to the first and second terminal T1 and T2 in the visual alarm circuit A and through terminals P9 and P10 in the audible alarm circuit D. The second extension lead P4, like the second power lead P2, is a common or potential reference lead for the second circuit B.

The visual alarm means 12 comprises first and second signal lamps L1 and L2, respectively, connected in parallel. One side of the said visual alarm means is connected to the common power lead P2 while the other side is connected through one side of a visual alarm energizing circuit 14 to the first power lead P1.

The visual alarm energizing circuit 14 includes, as an active circuit element, a first silicon controlled rectifier SCR1, hereinafter referred to solely as SCR1, having anode, cathode and gate terminals 16, 18 and 20, respectively. The anode terminal 16 is connected with the first power lead P1, the cathode terminal 18 is connected with the said other side of the said visual alarm means 12, and the gate terminal 20 is connected with one side of a current limiting first resistor R1, the other side of which is connected to a junction point 22. The junction point 22 is connected through a second resistor R2, with the common power lead P2. Optionally, the alarm trigger circuit 12 may include a first capacitor C1 connected between the cathode terminal 18 of the SCR1 and the first power lead P1 for the purpose of by-passing transient pulses around the SCR1 under operating conditions which produce these pulses.

A lead 24 extends from the junction point 22 to a third terminal T3 which is connected with first switch contact 26 of a normally open transducer switch T_o additionally comprising a switch bar 28 and a second contact 30, the said contacts being adapted to be bridged by the said switch bar. The second contact 30 of the switch T_o is connected through a fourth terminal T4 to a third common lead P5 which is associated with a plurality of circuits to be hereinafter described.

A signal coupling circuit 32 for effecting a triggering of the audible alarm when the visual alarm is triggered is connected between the lead 24 and the second common lead P2. The coupling circuit 32 comprises a second capacitor C2 connected at one side to the lead 24 and at the other, through a junction point 34 in series with a third resistor R3 between the lead 24 and second common lead P2, and a diode D1 connected at its anode to the said junction point 34 and at its cathode to a lead 36 which leads to an output terminal T5.

The output terminal T5 in the first circuit A is connected to a third terminal T11 in the second circuit B via a third extension lead P6.

A sixth terminal T6 in the first circuit A is connected with a fourth terminal T12 in the second circuit B via a fourth extension lead P7. An "acknowledge" switch SA

comprising first and second ganged switch bars **38** and **40**, respectively, is interconnected with the said sixth terminal **T6**.

The first switch bar **38** is adapted to bridge a first pair of contacts **42** which are in series in a lead **44** extending from the sixth terminal **T6** to the common power lead **P2**.

The second switch bar **40** is adapted to bridge a second pair of contacts **46**.

The acknowledge trigger circuit **48** includes a second silicon controlled rectifier **SCR2**, hereinafter referred to merely as **SCR2**, having anode, cathode and gate terminals **50**, **52** and **54**, respectively. Further included is a second diode **D2** connected at its anode to the first common lead **P1** and at its cathode to a junction point **56** which in turn is connected to one of the second pair of contacts **46** in the acknowledge switch **SA** via a lead **58**. The other of the contacts **46** is connected with the gate terminal **54** of the **SCR2** via a resistor **R4**.

The junction point **56** is joined with the anode terminal **50** of the **SCR2** via a current limiting fifth resistor **R5**.

The cathode terminal **52** of the **SCR2** is connected directly to the third common lead **P5** while the anode terminal **50** is coupled to the said second common lead **P2** through a third capacitor **C3**.

The anode terminal **50** of the **SCR2** is further coupled to one side of a sixth resistor **R6**, the said resistor being coupled at its other end to a junction point **60**.

The junction point **60** is coupled with the second common lead **P2** via a fourth capacitor **C4**, and with the anode terminal **62** of a third silicon controlled rectifier **SCR3**, hereinafter referred to merely as **SCR3**. The **SCR3** further includes a cathode terminal **64** connected with the third common lead **P5** and a gate terminal **66**. The gate terminal **66** of the **SCR3** is connected to the anode terminal **62** thereof through a Zener diode D_Z, the latter having its anode at the said gate terminal **66** and its cathode at the said anode terminal **62** to complete a trigger circuit **68** for the visual alarm means **12**.

For Sequence B operation of the first circuit A, a seventh resistor **R7** shown in dotted lines is connected in shunt with the **SCR3** from the first common line **P1** to the cathode terminal **18** of the said **SCR3**.

When it is desired to use the first circuit A with detector switches which are normally closed, the terminals **T3** and **T4** thereof are short circuited by the dotted lead **70** and a normally closed transducer switch T_c comprising a switch bar **72** adapted to break the circuit between a pair of contacts **74**. The contacts **74** are in series in a dotted lead **76** extending from the terminal **T2** on the second common lead **P2** to a terminal **T7** which is directly connected with the anode terminal **50** of the **SCR2** in the acknowledge trigger circuit **48**.

The second circuit B, for audible alarm annunciation, is identical for both Sequence A and Sequence B operation and will now be described.

A first branch circuit comprising a third diode **D3** and a fifth capacitor **C5**, connected in series through a common junction point **78**, is connected between the common leads **P3** and **P4**. The anode of the said third diode **D3** is connected with the common line **P3**.

The junction point **78** is connected with another junction point **80** through an eighth resistor **R8**. The junction point **80**, in turn, is connected directly to the terminal **T12**, is connected through a sixth capacitor **C6** to the common lead **P4**, and is also directly connected to the anode terminal **82** of a fourth silicon controlled rectifier **SCR4**, hereinafter referred to merely as **SCR4**, which further includes a cathode terminal **84** and a gate terminal **86** and which comprises the active element of an audible alarm trigger circuit **88**.

The gate terminal **86** of the **SCR4** is directly connected with the terminal **T11**, is coupled with the common line **P4** through a seventh capacitor **C7** and is connected through a ninth resistor **R9** with the gate terminal **90** of a fifth silicon controlled rectifier **SCR5**, hereinafter referred to merely as **SCR5**, which further includes an anode terminal **92** and a cathode terminal **94** and which comprises the active element of an audible alarm energizing circuit **96**.

The cathode terminal **94** of the **SCR5** is directly connected with the common lead **P4**. The anode terminal is connected with a first common terminal **98** on the audible alarm means **100**. A second common terminal **102** is provided on the opposite side of the audible alarm means **100** and is connected with the other common lead **P3**.

The electrical components of the audible alarm means, which is shown as a horn or buzzer, comprise an eighth capacitor **C8** a relay coil **L** and a fourth diode **D4** all connected in parallel between the common terminals **98** and **102**. The fourth diode **D4** has its anode and cathode connected with the common terminals **98** and **102**, respectively.

OPERATION

Referring again to FIGURE 1 the operation of this embodiment of the invention in the Sequence A mode will now be described.

First, it is assumed that all conditions are initially normal in the system and that the normally open transducer switch T_o is being used to effect the monitoring of a condition.

When the given condition becomes abnormal, the switch bar **28** makes the circuit through itself and the contacts **26** and **30**, short-circuiting the terminal **T3** and **T4** and connecting the cathode terminal **64** of the **SCR3** with the junction point **22** at the gate circuit of the **SCR1** via the third common lead **P5**, the said terminals **T3** and **T4** and the lead **24**.

The current supplied to the fourth capacitor **C4** via second diode **D2**, fifth resistor **R5**, and sixth resistor **R6** charges fourth capacitor **C4** to a potential equal to the positive peak potential of the A.C. power supplied to circuit A via terminal **T1**.

This potential is designed to exceed the breakdown potential of Zener diode D_Z. When transducer T_o closes it completes the cathode circuit of **SCR3** from cathode terminal **64** via switch T_o, junction **22**, and resistor **R2**, to the second common lead **P2**. This permits Zener diode D_Z to break down under the influence of the stored potential on fourth capacitor **C4** and conduct a small current to the second common lead **P2** via the gate terminal **66** of **SCR3**, the cathode terminal **64** of **SCR3**, switch T_o, junction **22**, and resistor **R2**. The small current through the gate of **SCR3** triggers it into full conduction allowing the entire energy store of fourth capacitor **C4** to flow as a large current pulse to second common lead **P2** via anode terminal **62** of **SCR3**, cathode terminal **64** of **SCR3**, switch T_o, junction **22**, and resistor **R2**. The resistance offered by **R2** to this current pulse is sufficient to divert a portion of said current pulse through resistor **R1** to the gate terminal **20** of **SCR1** thus triggering **SCR1** into conduction causing lamps **L1** and **L2** to flash for the duration of the pulse.

As long as the acknowledge switch **SA** is not closed by an operator, the capacitor **C4** will alternately charge through **D1**, resistor **R5** and resistor **R6** and discharge through the **SCR3**, resistor **R2** and resistor **R1** to effect a flashing of the alarm lamps **L1** and **L2** at a rate determined by the time constant of the R-C combination **R5–R6–C4**.

Since in the acknowledge trigger circuit **48** the combined resistance **R5–R6–R2** is sufficient to prevent a sustaining current in the **SCR3** when the capacitor **C4** is discharged, the **SCR3** is thus only fired in accordance with the said rate determined by the above-defined time constant. The anode supply to the **SCR1** is alternating current and thus provides a periodic interruption cutting off the **SCR1**.

The energy pulse from the **SCR3** charges the second capacitor **C2** in the output circuit **32** which discharges through the third resistor **R3** and the coupling path comprising diode **D1**, lead **36**, terminal **T5**, extension lead **P6**

and terminal T11 to charge the seventh capacitor C7 in the audible alarm trigger circuit 88.

When the capacitor C7 reaches a predetermined level of charge, it delivers a charging current through the gate terminal 86 of the SCR4 triggering the same and sending a pulse of energy to the gate terminal 90 of the SCR5. This triggers the SCR5 causing current to flow in the audible alarm energizing circuit 90 and sound the alarm 100.

The SCR4 is held on by way of the D.C. voltage maintained on the filter capacitor C5 and C6 fed by the third diode D3.

The relay coil L of the audible alarm means 100 is held energized by the smoothing capacitor C8 in parallel therewith and the SCR5. The audible alarm means 100 is protected from transient surges from the relay coil L by the fourth diode D4.

Thus, at this stage in the operation, the first part of Sequence A operation has been effected, namely, flashing visual signal means 12 and continuous audible signal means 100.

Once an operator has noted the indicated abnormal condition sensed by the transducer T_o, the acknowledge switch SA is closed causing the switch bars 38 and 40 to bridge the contact pairs 42 and 46, respectively.

The filter capacitor C6 is immediately short circuited through the switch bar and contacts 38 and 42, via terminal T12, extension lead P7, and lead 44, the common leads P2 and P4 being at the same potential. This causes the voltage at the anode terminal 82 of the SCR4 to drop below that required to hold the SCR4 on and effects its cut off. When the SCR4 cuts off it removes the necessary sustaining bias from the gate terminal 90 of the SCR5 which cuts off, silencing the audible alarm means 100.

At the same time, the gate terminal 54 of the SCR2 is connected with the power source 10 through diode D2, junction 56, lead 58, switch bar and contacts 40 and 46, respectively, and resistor R4 resulting in the triggering of the SCR2.

Because of the capacitor C3, the SCR2 is continuously conductive and supplies a constant voltage through the resistor R2. Thus, a gate current is continuously applied through the resistor R1 to the gate terminal 20 of the SCR1, the latter now being, therefore, continuously conducting and the visual alarm lamps L1 and L2 providing a steady signal instead of flashing.

The SCR3 and the balance of the audible alarm trigger circuit 68 are shunted out of operation by the triggering of the SCR2 and thus, the acknowledge switch SA need only be momentarily closed.

As soon as the condition being monitored returns to normal, the transducer switch T_o opens and de-energizes the SCR2 and the SCR1, thus de-activating the acknowledge circuit 48 and the audible alarm energizing circuit 14, causing the alarm lamps L1 and L2 to be extinguished.

Thus, a complete Sequence A alarm annunciation cycle has been completed.

For the operation of the normally closed transducer means Tc, the visual alarm trigger circuit 68 is short circuited by the line 76 across terminals T7 and T2 and thus, the audible alarm trigger circuit 88 is also excluded from operation. The third common lead P5, however, is connected with the lead 24 via the short 70 at terminals T3 and T4 and therefore, when an abnormal condition causes the switch bar 72 to break with the contacts 74, the operation of the system is identical with that previously described.

For Sequence B operation, all of the operation for Sequence A is identical, the difference being that a small current through the resistor R7 keeps the alarm lamps L1 and L2 dimly illuminated.

Because of its pulse type energization via the terminal T11 and its ready extinguishment via the terminal T12, the audible alarm circuit B may be in common connection with a plurality of visual alarm circuits A. Thus, only one audible alarm means is required for multitudinous visual alarm means.

CIRCUIT RESPONSIVE TO MOMENTARY FAULTS

Referring now to FIGURE 2, a second embodiment A' of the visual alarm and sensing circuit A, of FIGURE 1, will now be described, like elements to those of FIGURE 1 bearing like numerals.

In this embodiment, the SCR1 is alternatively shunted by a fifth half-wave diode D5, connected at its cathode to the first power lead P1 and at its anode to the cathode terminal 18 of the SCR1 for a purpose to be hereinafter described.

The trigger circuit 68 for the visual alarm means 12 is connected directly with the alarm energizing circuit 14 by a lead 104 which connects the cathode terminal 64 of the SCR3 with the common node 22 in the gate circuit of the SCR1.

The visual alarm trigger circuit 68 is selectively powered from the A.C. source 10 via a sixth silicon controlled rectifier SCR6, hereinafter referred to merely as SCR6, which also comprises an active element in an acknowledge trigger circuit 106. The SCR6 includes an anode terminal 108 connected via the diode D2 to the first power lead P1, a cathode terminal 110 connected via the sixth resistor R6 to the anode terminal 62 of the SCR3, and a gate terminal 112 comprising the common junction of a voltage divider consisting of tenth and eleventh series resistors R10 and R11, respectively.

The resistor R10 is connected at its outer end with a junction point 114 common to both the third circuit terminal T3 of the circuit A' and the anode terminal 116 of a seventh silicon controlled rectifier SCR7, hereinafter referred to merely as SCR7, the said SCR7 further including cathode and gate terminals 118 and 120, respectively. The resistor R11 is connected at its outer end with the cathode terminal 110 of the SCR6. A third capacitor C3 is connected between the anode 108 of the SCR6 and the second or common power lead P2.

The cathode terminal 118 of the SCR7 is connected with the outer terminal of the second capacitor C2 in the signal coupling circuit 32.

The gate terminal 120 of the SCR7 is connected via a twelfth resistor R12 with the anode of a sixth diode D6, said anode being directly connected with one of the second pair of contacts 46 of the acknowledge switch SA. The cathode of the said sixth diode D6 is connected directly to the cathode terminal 110 of the SCR6.

The other of the second pair of contacts 46 in the acknowledge switch SA is connected directly to the anode terminal 108 of the SCR6 via the series path comprising leads 122 and 124 and is connected to the fourth circuit terminal T4 via the series path comprising leads 122 and 126, thirteenth resistor R13 and lead 128.

The anode terminal 116 of the SCR7, common node 114 and the third circuit terminal T3 are all connected with the second or common power lead P2 through a ninth capacitor C9, thus completing the acknowledge trigger circuit 106.

The normally open transducer or detector switch T_o has its contacts 26 and 30 connected, respectively, with circuit terminals T3 and T4.

For using a normally closed detector switch Tc, the pair of contacts 74 thereof are respectively connected to the circuit terminals T2 and T3; and the circuit terminals T3 and T4 are additionally short circuited via a jumper 130 as shown by dotted lines in FIGURE 2.

As already illustrated in FIGURE 1, the circuit terminals T1, T2, T5 and T6 of the sensing and visual alarm circuit A' are to be interconnected with the terminals T9, T10, T11 and T12, respectively, of the audible alarm circuit B.

OPERATION

Referring further to FIGURE 2, the operation of this embodiment of the invention will now be described.

As previously described in conjunction with FIGURE 1, the SCR1 controls the conduction of positive half-cycles of current from the A.C. power source **10** to the signal lamps L1 and L2 when gate signals of the proper magnitude are applied to the common junction **22** in the gate circuit of the SCR1.

The optional or fifth diode D5 is utilized during Sequence B operation whereby it continuously operates the lamps L1 and L2 on negative half-cycles from the A.C. source **10** at the half-wave power level while, when the SCR1 is switched on, the lamps L1 and L2 burn more brightly, being illuminated at the full-wave power level. This embodiment substantially eliminates the heat dissipation and heat rise caused by the resistor R7 in the embodiment of FIGURE 1.

The third capacitor C3 is charged via the second diode D2 to impose a D.C. potential between the fourth circuit terminal T4 and the common power lead P2.

Assuming that the normally open detector switch T_o is connected as the remote or field sensing element, and further, that the contacts **26** and **30** thereof have been shorted by the contact bar **28**, the positive potential stored in the third capacitor C3 is connected to the anode terminal **116** of the SCR7 via the series path comprising leads **124**, **126**, resistor R13, lead **128**, terminals T4, transducer T_o, terminal T3 and common junction **114**. This potential is also applied via the common junction **114** and the voltage divider R10–R11 to the gate terminal **112** of the SCR6, whereby the SCR6 is triggered into the conductive state.

This causes positive half-cycles to be applied to the fourth capacitor C4 via resistor R6 causing it to charge to a potential exceeding the breakdown voltage of Zener diode D_Z, said potential being applied via anode terminal **62** of SCR3 to the visual alarm trigger circuit **68** which cooperates with the alarm energizing circuit **14**, as already described in conjunction with FIGURE 1, to produce a flashing visual alarm via the lamps L1 and L2.

If the closing of the detecting transducer T_o has been of a momentary nature, the flashing signal will be initiated and then maintained because the charge on capacitor C3 will maintain a D.C. anode potential supply at the anode terminal **108** of SCR6 holding it in conduction. However, no D.C. potential will be applied to the anode terminal **116** of the SCR7, and thus, when the second pair of contacts **46** of the acknowledge switch SA are closed by the circuit operator in response to the visual flashing and audible signals, no conduction of the SCR7 occurs. But the closing of said contacts **46** causes a shunting of the SCR6 through the sixth diode D6, resulting in the extinguishment of the SCR6 and the flashing signal lamps L1 and L2.

Had the closing of the detecting transducer T_o been prolonged, the positive potential at the anode terminal **116** of the SCR7 and the potential applied to the gate terminal **120** thereof via the leads **124** and **122**, switch bar **40**, and the second contacts **46** of the acknowledge switch SA would result in the conduction of the SCR7, effecting a shunt of the third capacitor C3, extinguishing the SCR6, and providing a steady gate signal present at the common junction **22** in the gate circuit adjacent the gate terminal **20** of the SCR1 via the cathode terminal **118** of the SCR7 and the lead **24**. Thus, the SCR1 is held in the conducting state to maintain a steady illumination in the signal lamps L1 and L2 commensurate with the previously defined acknowledged abnormal signal for both Sequence A and Sequence B operation.

In the case of using the sensing transducers TC, with normally closed contacts, the third circuit terminal T3 is held at the potential of the common lead P2 via the normally closed contacts **74** and switch bar **72** of the transducer TC. If these contacts **74**, however, should open in response to an abnormal condition, this will permit the third circuit terminal T3 to rise to the same positive potential that exists across the third capacitor C3. At this point, because of the jumper lead **130** across the third and fourth circuit terminals T3 and T4, the circuit A' is in the same condition as it was initially when the normally open switch T_o was closed. Thus, the subsequent operation for a prolonged opening of the normally closed switch TC is the same as previously described for the prolonged closing of the normally open switch T_o.

For a momentary abnormality, even though the third terminal T3 is returned to the potential of the common lead P2, the SCR6 has been triggered into conductivity and the anode terminal **116** of the SCR7 has been placed at the potential of the common lead P2. Thus, the closing of the acknowledge switch SA will not trigger the SCR7 and will result in a return of the signal lamps L1 and L2 in the circuit A to the state representative of a "normal" condition in the Sequence A or Sequence B operating modes, as the case may be.

As can be seen from the foregoing specification and drawings, this invention provides a new and novel alarm annunciator circuit means which is highly versatile and which has only silicon controlled rectifiers as its active elements.

It is to be understood that the embodiment of the invention shown and described herein is for the purpose of example only and is not intended to limit the scope of the appended claims.

What is claimed is:

1. In an alarm annunciator circuit including a power source, visual alarm means, and audible alarm means, means actuating said alarm means from an initial state to another in response to a predetermined condition comprising transducer means monitoring said condition, relaxation oscillator means selectively connected with said power source and actuated by said transducer means, first semiconductor switch means, periodically triggered by said relaxation oscillator means, connected with said source and said alarm means comprising intermittent energizing means for said visual alarm means, pulse generating means energized by said relaxation oscillator means, trigger means interconnected with and actuated by said pulse generating means, second semiconductor switch means for said audible alarm means interconnected with and actuated by said trigger means, and acknowledge means selectively deenergizing said audible alarm means and constraining said first semiconductor switch means to continuously energize said visual alarm means including means deactuating said trigger means and said relaxation oscillator means; wherein said relaxation oscillator means includes rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source, said cathode terminal being further coupled with said semiconductor switch means, capacitance means connected from said anode terminal to the said other side of said source, and a Zener diode connected between said anode terminal and said gate terminal.

2. The invention defined in claim **1**, wherein said first semiconductor switch means comprises a silicon controlled rectifier having anode, cathode and gate terminals, said anode and cathode terminals being connected in series between said source and said visual alarm means and said gate terminal being coupled to said relaxation oscillator means.

3. The invention defined in claim **1**, wherein said pulse generating means comprises a capacitor connected on one side to said relaxation oscillator means and a resistor in series therewith having a common junction therebetween, said resistor being connected with said power source, and a diode having anode and cathode terminals, connected at

its anode to said common junction and at its cathode to said trigger means.

4. In an alarm annunciator circuit including a power source, visual alarm means, and audible alarm means, means actuating said alarm means from an initial state to another in response to a predetermined condition comprising transducer means monitoring said condition, relaxation oscillator means selectively connected with said power source and actuated by said transducer means, first semiconductor switch means, periodically triggered by said relaxation oscillator means, connected with said source and said alarm means comprising intermittent energizing means for said visual alarm means, pulse generating means energized by said relaxation oscillator means, trigger means interconnected with and actuated by said pulse generating means, second semiconductor switch means for said audible alarm means interconnected with and actuated by said trigger means, and acknowledge means selectively deenergizing said audible alarm means, and constraining said first semiconductor switch means to continuously energize said visual alarm means including means deactuating said trigger means and said relaxation oscillator means; wherein said trigger means comprises rectifier means connected with one side of said source, first capacitance means in series therewith and connected with the other side of said source, a common junction between said rectifier and capacitance means, silicon controlled rectifier means having anode, cathode and gate terminals, resistance means connected between said anode terminal and said common junction, second capacitance means connected between said anode terminal and the other side of said source, third capacitance means connected between said gate terminal and said other side of said source, and second resistance means coupling said gate terminal with said second semiconductor switch means, said anode terminal being connected with said acknowledge means, said gate terminal being connected with said pulse generating means and said cathode terminal being connected with said second semiconductor switch means.

5. The invention defined in claim 1, wherein said second semiconductor switch means comprises a silicon controlled rectifier having anode, cathode and gate terminals, said anode and cathode terminals being connected in series between said source and said audible alarm means and said gate terminal being coupled to said trigger means.

6. In an alarm annunciator circuit including a power source, visual alarm means, and audible alarm means, means actuating said alarm means from an initial state to another in response to a predetermined condition comprising transducer means monitoring said condition, relaxation oscillator means selectively connected with said power source and actuated by said transducer means, first seimconductor switch means, periodically triggered by said relaxation oscillator means, connected with said source and said alarm means comprising intermittent energizing means for said visual alarm means, pulse generating means energized by said relaxation oscillator means, trigger means interconnected with and actuated by said pulse generating means, second semiconductor switch means for said audible alarm means interconnected with and actuated by said trigger means, and acknowledge means selectively deenergizing said audible alarm means and constraining said first semiconductor switch means to continuously energize said visual alarm means including means deactuating said trigger means and said relaxation oscillator means; wherein said acknowledge means comprises first switch means selectively shunting said source from said trigger means, second switch means, semiconductor switch means having anode, cathode and gate terminals, said anode and cathode terminals being connected in shunt with said relaxation oscillator means, said anode terminal being further connected with said second switch means and coupled with one side of said source, and said cathode terminal being connected with a load resistor common to said relaxation oscillator means and coupled with said first semiconductor switch means, resistance means interconnecting said second switch means and said gate terminal, and capacitance means interconnecting said anode terminal and the other side of said source.

7. In an alarm annunciator circuit including a power source, condition responsive transducer means and a visual alarm means, means for intermittently energizing said visual alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, including rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source and having a common connection with said cathode terminal, capacitance means connected from said anode terminal to the other side of said source, and a Zener diode connected between said anode terminal and said gate terminal; and semiconductor switch means, including a gate terminal and resistance means interconnecting said gate terminal and said common connection, periodically triggered by said oscillator means, interconnected with said source and said alarm means.

8. In an alarm annunciator circuit including a power source, condition responsive transducer means and a visual alarm means, means for intermittently energizing said visual alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, including rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source and having a common connection with said cathode terminal, capacitance means connected from said anode terminal to the other side of said source, and a Zener diode connected between said anode terminal and said gate terminal; and semiconductor switch means, including anode, cathode and gate terminals, said anode and cathode terminals being connected in series with said source and said alarm means, and resistance means interconnecting said gate terminal and said common connection.

9. In an alarm annunciator circuit including a power source, condition responsive transducer means and a visual alarm means, means for intermittently energizing said visual alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, including rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source and having a common connection with said cathode terminal, capacitance means connected from said anode terminal to the other side of said source, and a Zener diode connected between said anode terminal and said gate terminal; and semiconductor switch means, including a gate terminal and resistance means interconnecting said gate terminal and said common connection, periodically triggered by said oscillator means, interconnected with said source and said alarm means, and means providing a minimum energization of said alarm means superimposed on said intermittent energization thereof.

10. In an alarm annunciator circuit including a power source, condition responsive transducer means and a visual alarm means, means for intermittently energizing said visual alarm means comprising relaxation oscillator

means selectively connected with said power source and actuated by said transducer means including rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source and having a common connection with said cathode terminal, capacitance means connected from said anode terminal to the other side of said source, and a Zener diode connected between said anode terminal and said gate terminal; semiconductor switch means, including a gate terminal and resistance means interconnecting said gate terminal and said common connection, periodically triggered by said oscillator means, interconnected with said source and said alarm means; and acknowledge means including second semiconductor switch means in shunt with said silicon controlled rectifier and connecting said source with said load resistor, and selective control means energizing said second semiconductor switch means to thereby preclude intermittent energization of said alarm means by said oscillator means and continuously energize said first semiconductor switch means.

11. In an alarm annunciator circuit including a power source, condition responsive transducer means and a visual alarm means, means for intermittently energizing said visual alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means including rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source and having a common connection with said cathode terminal, capacitance means connected from said anode terminal to the other side of said source, and a Zener diode connected between said anode terminal and said gate terminal; first semiconductor switch means, including anode, cathode and gate terminals, said anode and cathode terminals being connected in series with said source and said alarm means, and resistance means interconnecting said gate terminal and said common connection; and acknowledge means including second semiconductor switch means having anode, cathode and gate terminals, said anode and cathode terminals being connected in shunt with said silicon controlled rectifier and said cathode terminal being further connected with said common connection, said anode terminal being further connected with one side of said source, capacitance means connected between said anode terminal and the other side of said source, switch means connected on one side with said anode means and resistance means interconnecting said gate terminal with the other side of said switch means.

12. The invention defined in claim **10**, wherein said means further includes means providing a minimum energization of said alarm means superimposed on said intermittent energization thereof.

13. The invention defined in claim **11**, wherein said means further includes means providing a minimum energization of said alarm means superimposed on said intermittent energization thereof.

14. In an alarm annunciator circuit including a power source, audible alarm means and condition responsive transducer means, means for energizing said audible alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, pulse generating means connected with said oscillator means and producing energy pulses in response to the energization of said oscillator means, trigger means actuated by said pulse generating means and semiconductor switch means energized by said trigger means and connected in series with said source and said audible alarm means; said relaxation oscillator comprising rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source, said cathode terminal being further coupled with said semiconductor switch means, capacitance means connected from said anode terminal to the said other side of said source, and a Zener diode connected between said anode terminal and said gate terminal.

15. In an alarm annunciator circuit including a power source, audible alarm means and condition responsive transducer means, means for energizing said audible alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, and including a load resistor, pulse generating means connected in shunt with said load resistor producing energy pulses in response to the energization of said oscillator means and having an output; trigger means actuated by said pulse generating means including a resistance-capacitance input network connected across said source, a silicon controlled rectifier having anode, cathode and gate terminals, said gate terminal being connected with said output of said pulse generating means, said anode terminal being connected with said input network, and capacitance means coupling said gate terminal with one side of said source; and semiconductor switch means, including a resistance means and a gate terminal connected with said cathode terminal and coupled through said resistance means to the said gate terminal of said silicon controlled rectifier, connected in series with said source and said audible alarm means.

16. In an alarm annunciator circuit including a power source, audible alarm means and condition responsive transducer means, means for automatically energizing and selectively deenergizing said audible alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, pulse generating means connected with said oscillator means and producing energy pulses in response to the energization of said oscillator means, trigger means actuated by said pulse generating means, semiconductor switch means energized by said trigger means and connected in series with said source and said audible alarm means, and acknowledge means selectively deenergizing said trigger means and thus deenergizing said semiconductor switch means said relaxation oscillator comprising rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source, said cathode terminal being further coupled with said semiconductor switch means, capacitance means connected from said anode terminal to the said other side of said source, and a Zener diode connected between said anode terminal and said gate terminal.

17. In an alarm annunciator circuit including a power source, audible alarm means and condition responsive transducer means, means for automatically energizing and selectively deenergizing said audible alarm means comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means and including a load resistor, pulse generating means connected in shunt with said load resistor producing energy pulses in response to the energization of said oscillator means and having an output; trigger means actuated by said pulse generating means including a resistance-capacitance input network connected across said source, a silicon controlled rectifier having anode, cathode and gate terminals, said gate terminal being connected with said output of said pulse generating means, said anode

terminal being connected with said input network, and capacitance means coupling said gate terminal with one side of said source; semiconductor switch means, including a resistance means and a gate terminal connected with said cathode terminal and coupled through said resistance means to the said gate terminal of said silicon controlled rectifier, connected in series with said source and said audible alarm means; and acknowledge means comprising switch means short circuiting said input network of said trigger means thereby deenergizing said trigger means and thus, deenergizing said semiconductor switch means.

18. In an alarm annunciator circuit including a power source, condition responsive transducer means and a visual alarm means having a normally quiescent state of energization, means for automatically energizing said alarm intermittently in response to both prolonged and momentary responses of said transducer means and subsequent to the respective ones of said responses selectively energizing said alarm means continuously and returning said alarm means to its quiescent state, respectively, comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, semiconductor switch means periodically triggered by said oscillator means interconnected with said source and said alarm means, and acknowledge means deenergizing said oscillator means and continuously energizing said semiconductor switch means in the event of said prolonged responses of said transducer means including first and second semiconductor means, said first semiconductor means interconnected with and controlling the energization of said oscillator means, and said second semiconductor means disabling said first semiconductor means, said oscillator means and said semiconductor switch means in the event of said momentary responses of said transducer means and maintaining a state of energization in said semiconductor switch means in the event of said prolonged responses; said relaxation oscillator comprising rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source, said cathode terminal being further coupled with said semiconductor switch means, capacitance means connected from said anode terminal to the said other side of said source, and a Zener diode connected between said anode terminal and said gate terminal.

19. In an alarm annunciator circuit including a power source, condition responsive transducer means and a visual alarm means having a normally quiescent state of energization, means for automatically energizing said alarm intermittently in response to both prolonged and momentary responses of said transducer means and subsequent to the respective ones of said responses selectively energizing said alarm means continuously and returning said alarm means to its quiescent state, respectively, comprising relaxation oscillator means selectively connected with said power source and actuated by said transducer means, semiconductor switch means periodically triggered by said oscillator means interconnected with said source and said alarm means, and acknowledge means deenergizing said oscillator means and continuously energizing said semiconductor switch means in the event of said prolonged responses of said transducer means including first and second semiconductor means, said first semiconductor means interconnected with and controlling the energization of said oscillator means, and said second semiconductor means disabling said first semiconductor means, said oscillator means and said semiconductor switch means in the event of said momentary responses of said transducer means and maintaining a state of energization in said semiconductor switch means in the event of said prolonged responses; and means providing a minimum energization of said alarm means superimposed on all other conditions thereof comprising half-wave rectifier means in series with said power source and said visual alarm means having the direction of conductivity therethrough opposite to the direction of conductivity through said semiconductor switch means.

20. In an alarm annunciator circuit including a power source, visual alarm means, and audible alarm means, means actuating said alarm means from an initial state to another in response to a predetermined condition comprising transducer means monitoring said condition, relaxation oscillator means selectively connected with said power source and actuated by said transducer means, first semiconductor switch means periodically triggered by said oscillator means connected with said source and said alarm means comprising intermittent energizing means for said visual alarm means, pulse generating means energized by said oscillator means, trigger means interconnected with and actuated by said pulse generating means, second semiconductor switch means for said audible alarm means interconnected with and actuated by said trigger means, and acknowledge means selectively deenergizing said audible alarm means and constraining said semiconductor switch means to continuously energize said visual alarm means including means deactuating said trigger means and said oscillator means in the event of a prolonged occurrence of said predetermined condition and further, in the event of a momentary occurrence of said predetermined condition, including means deactuating said semiconductor switch means to return said visual alarm means to its initial state and deactuating said trigger means and said oscillator means; wherein said relaxation oscillator means includes rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source, said cathode terminal being further coupled with said semiconductor switch means, capacitance means connected from said anode terminal to the said other side of said source, and a Zener diode connected between said anode terminal and said gate terminal.

21. The invention defined in claim 20, wherein said semiconductor switch means comprises a silicon controlled rectifier having anode, cathode and gate terminals, said anode and cathode terminals being connected in series between said source and said visual alarm means and said gate terminal being coupled to said relaxation oscillator means.

22. The invention defined in claim 20, wherein said pulse generating means comprises a capacitor connected on one side to said relaxation oscillator means and a resistor in series therewith having a common junction therebetween, said resistor being connected with said power source, and a diode having anode and cathode terminals, connected at its anode to said common junction and at its cathode to said trigger means.

23. In an alarm annunciator circuit including a power source, visual alarm means, and audible alarm means, means actuating said alarm means from an initial state to another in response to a predetermined condition comprising transducer means monitoring said condition, relaxation oscillator means selectively connected with said power source and actuated by said transducer means, first semiconductor switch means periodically triggered by said oscillator means connected with said source and said alarm means comprising intermittent energizing means for said visual alarm means, pulse generating means energized by said oscillator means, trigger means interconnected with and actuated by said pulse generating means, second semiconductor switch means for said audible alarm means interconnected with an actuated by said trigger means, and acknowledge means selectively deenergizing said audible alarm means and constraining said semiconductor

switch means to continuously energize said visual alarm means including means deactuating said trigger means and said oscillator means in the event of a prolonged occurrence of said predetermined condition and further, in the event of a momentary occurrence of said predetermined condition, including means deactuating said semiconductor switch means to return said visual alarm means to its initial state and deactuating said trigger means and said oscillator means; wherein said trigger means comprises rectifier means connected with one side of said source, first capacitance means in series therewith and connected with the other side of said source, a common junction between said rectifier and capacitance means, silicon controlled rectifier means having anode, cathode and gate terminals, resistance means connected between said anode terminal and said common junction, second capacitance means connected between said anode terminal and the other side of said source, third capacitance means connected between said gate terminal and said other side of said source, and second resistance means coupling said gate terminal with said second semiconductor switch means, said anode terminal being connected with said acknowledge means, said gate terminal being connected with said pulse generating means and said cathode terminal being connected with said second semiconductor switch means.

24. The invention defined in claim 20, wherein said second semiconductor switch means comprises a silicon controlled rectifier having anode, cathode and gate terminals, said anode and cathode terminals being connected in series between said source and said audible alarm means and said gate terminal being coupled to said trigger means.

25. In an alarm annunciator circuit including a power source, visual alarm means, and audible alarm means, means actuating said alarm means from an initial state to another in response to a predetermined condition comprising transducer means monitoring said condition, relaxation oscillator means selectively connected with said power source and actuated by said transducer means, first semiconductor switch means periodically triggered by said first oscillator means connected with said source and said alarm means comprising intermittent energizing means for said visual alarm means, pulse generating means energized by said first oscillator means, trigger means interconnected with and actuated by said pulse generating means, second semiconductor switch means for said audible alarm means interconnected with and actuated by said trigger means, and acknowledge means comprising first switch means selectively shunting said source from said trigger means, third semiconductor switch means in series with said source and said relaxation oscillator means, second switch means selectively shunting said source from said third semiconductor switch means, and fourth semiconductor switch means in circuit with said transducer means selectively shunting said source from said relaxation oscillator means and interconnected with said first semiconductor switch means wherein said relaxation oscillator means includes rectifier means connected with one side of said source, resistance means in series therewith, a silicon controlled rectifier having anode, cathode and gate terminals, said anode terminal being coupled with said resistance means, a load resistor connected in series with said cathode terminal and the other side of said source, said cathode terminal being further coupled with said first semiconductor switch means, capacitance means connected from said anode terminal to the said other side of said source, and a Zener diode connected between said anode terminal and said gate terminal.

26. The invention defined in claim 1, wherein said trigger means comprises rectifier means connected with one side of said source, first capacitance means in series therewith and connected with the other side of said source, a common junction between said rectifier and capacitance means, silicon controlled rectifier means having anode, cathode and gate terminals, resistance means connected between said anode terminal and said common junction, second capacitance means connected between said anode terminal and the other side of said source, third capacitance means connected between said gate terminal and said other side of said source, and second resistance means coupling said gate terminal with said second semiconductor switch means, said anode terminal being connected with said acknowledge means, said gate terminal being connected with said pulse generating means and said cathode terminal being connected with said second semiconductor switch means.

27. The invention defined in claim 1, wherein said acknowledge means comprises first switch means selectively shunting said source from said trigger means, second switch means, semiconductor switch means having anode, cathode and gate terminals, said anode and cathode terminals being connected in shunt with said relaxation oscillator means, said anode terminal being further connected with said second switch means and coupled with one side of said source, and said cathode terminal being connected with a load resistor common to said relaxation oscillator means and coupled with said first semiconductor switch means, resistance means interconnecting said second switch means and said gate terminal, and capacitance means interconnecting said anode terminal and the other side of said source.

28. The invention defined in claim 1, wherein said trigger means comprises rectifier means connected with one side of said source, first capacitance means in series therewith and connected with the other side of said source, a common junction between said rectifier and capacitance means, silicon controlled rectifier means having anode, cathode and gate terminals, resistance means connected between said anode terminal and said common junction, second capacitance means connected between said anode terminal and the other side of said source, third capacitance means connected between said gate terminal and said other side of said source, and second resistance means coupling said gate terminal with said second semiconductor switch means, said anode terminal being connected with said acknowledge means, said gate terminal being connected with said pulse generating means and said cathode terminal being connected with said second semiconductor switch means; and wherein said acknowledge means comprises first switch means selectively shunting said source from said trigger means, second switch means, semiconductor switch means having anode, cathode and gate terminals, said anode and cathode terminals being connected in shunt with said relaxation oscillator means, said anode terminal being further connected with said second switch means and coupled with one side of said source, and said cathode terminal being connected with a load resistor common to said relaxation oscillator means and coupled with said first semiconductor switch means, resistance means interconnecting said second switch means and said gate terminal, and capacitance means interconnecting said anode terminal and the other side of said source.

29. The invention defined in claim 20, wherein said trigger means comprises rectifier means connected with one side of said source, first capacitance means in series therewith and connected with the other side of said source, a common junction between said rectifier and capacitance means, silicon controlled rectifier means having anode, cathode and gate terminals, resistance means connected between said anode terminal and said common junction, second capacitance means connected between said anode terminal and the other side of said source, third capacitance means connected between said gate terminal and said other side of said source, and second resistance means coupling said gate terminal with said second semiconductor switch means, said anode terminal being connected with said acknowledge means, said gate terminal being connected with said pulse generating means and said

cathode terminal being connected with said second semiconductor switch means.

30. The invention defined in claim 25, wherein said trigger means comprises rectifier means connected with one side of said source, first capacitance means in series therewith and connected with the other side of said source, a common junction between said rectifier and capacitance means, silicon controlled rectifier means having anode, cathode and gate terminals, resistance means connected between said anode terminal and said common junction, second capacitance means connected between said anode terminal and the other side of said source, third capacitance means connected between said gate terminal and said other side of said source, and second resistance means coupling said gate terminal with said second semiconductor switch means, said anode terminal being connected with said acknowledge means, said gate terminal being connected with said pulse generating means and said

cathode terminal being connected with said second semiconductor switch means.

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