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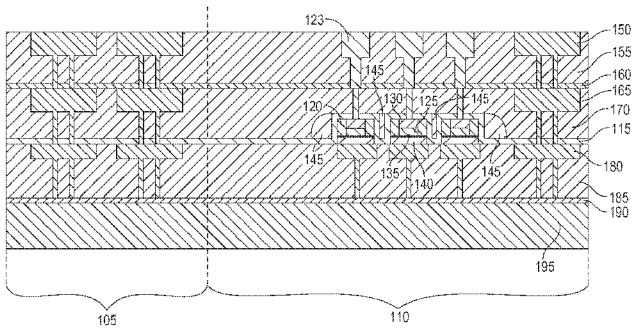


FIG. 1

(57) Abstract: An embodiment integrates memory, such as spin-torque transfer magnetoresistive random access memory (STT-MRAM) within a logic chip. The STT-MRAM includes a magnetic tunnel junction (MTJ) with an upper MTJ layer, lower MTJ layer, and tunnel barrier directly contacting the upper MTJ layer and the lower MTJ layer; wherein the upper MTJ layer includes an upper MTJ layer sidewall and the lower MTJ layer includes a lower MTJ sidewall horizontally offset from the upper MTJ layer. Another embodiment includes a memory area, comprising a MTJ, and a logic area located on a substrate; wherein a horizontal plane intersects the MTJ, a first Inter-Layer Dielectric (ILD) material adjacent the MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another. In an embodiment the first and second ILDs directly contact one another. Other embodiments are described herein.

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LOGIC CHIP INCLUDING EMBEDDED MAGNETIC TUNNEL JUNCTIONS

Technical Field

[0001] Embodiments of the invention are in the field of semiconductor devices and, in particular, logic chips having embedded memory.

Background

[0002] Integrating memory directly onto a logic chip (e.g., microprocessor chip) enables wider buses and higher operation speeds compared to having physically separate logic and memory chips. Such memory may include traditional charge-based memory technologies such as dynamic random-access memory (DRAM) and NAND Flash memory.

Brief Description of the Drawings

[0003] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures, in which:

[0004] Figure 1 depicts a logic chip including embedded magnetic tunnel junctions in an embodiment of the invention.

[0005] Figures 2-16 depict a process for fabricating a logic chip including embedded magnetic tunnel junctions in an embodiment of the invention.

[0006] Figure 17 depicts a logic chip including embedded magnetic tunnel junctions in an embodiment of the invention.

[0007] Figure 18 depicts a magnetic tunnel junction in an embodiment of the invention.

[0008] Figure 19 depicts a system for use with embodiments of the invention.

Detailed Description

[0009] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of integrated circuit structures. Thus, the actual appearance of the

fabricated integrated circuit structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are in direct physical or electrical contact with each other and "coupled" may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact. Also, while similar or same numbers may be used to designate same or similar parts in different figures, doing so does not mean all figures including similar or same numbers constitute a single or same embodiment. Terms such as "upper" and "lower" "above" and "below" may be understood by reference to the illustrated X-Z coordinates, and terms such as "adjacent" may be understood by reference to X-Y coordinates or to non-Z coordinates.

[0010] As stated above, integrating memory directly onto a logic chip has advantages. Such memory may include DRAM and NAND Flash memory. However, DRAM and NAND Flash memory have scalability issues related to increasingly precise charge placement and sensing requirements, and hence embedding charge-based memory directly onto a high performance logic chip is problematic at, for example, sub-20 nm technology nodes.

[0011] An embodiment includes a logic chip integrated with a memory; however the memory scales to smaller geometries than possible with traditional charge-based memories. In one embodiment the memory is a spin-torque transfer magnetoresistive random access memory (STT-MRAM), which relies on resistivity

rather than charge as the information carrier. More specifically, an embodiment includes at least one STT-MRAM memory embedded within a memory layer of a logic chip (e.g., processor). The at least one STT-MRAM memory may include at least one STT-MRAM array having at least one magnetic tunnel junction (MTJ). Other memories besides STT-MRAM, such as resistive RAM (RRAM), are used in other embodiments.

[0012] An embodiment integrates a STT-MRAM within a logic chip, where the memory includes a MTJ that has an upper MTJ layer, a lower MTJ layer, and a tunnel barrier directly contacting the upper MTJ layer and the lower MTJ layer; wherein the upper MTJ layer includes an upper MTJ layer sidewall and the lower MTJ layer includes a lower MTJ sidewall horizontally offset from the upper MTJ layer. Another embodiment includes a memory area, comprising a MTJ, and a logic area located on a substrate; wherein a horizontal plane intersects the MTJ, a first Inter-Layer Dielectric (ILD) material adjacent the MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another. In an embodiment the first and second ILDs directly contact one another. Other embodiments are described herein.

[0013] Figure 1 depicts a logic chip including embedded MTJs in an embodiment. Although MTJs may comprise multiple layers of very thin metal films, for discussion purposes the MTJ film stack is divided into four portions in Figure 1: "bottom MTJ" 140 (the bottom layer of the MTJ), "tunnel barrier" 135, "top MTJ" 125 (the top layer of the MTJ), and hardmask layer 130. Figure 1 shows three MTJs all included in M2 metal layer 165. The three MTJs are included on silicon substrate 195 and various build up layers generally represented by layer 190. The three MTJs are shown as being embedded in M2 165 for discussion purposes but could be embedded in other interconnect layers such as metal layers M1 180, M3 150, and the like.

[0014] For clarity purposes some details are not labeled in Figure 1 but those details will become clearer when discussing a manufacturing process for the device of Figure 1 using Figures 2-16. For example, although there are several spacer portions in Figure 1 possibly only one such portion is labeled for purposes of clarity. However, other portions may be labeled in one or more of Figures 2-16.

[0015] In the embodiment of Figure 1 sidewall spacer 120 is located along the edges of patterned hardmask 130 and top MTJ 125 films. Sidewall spacer 120 protects the edges of top MTJ films 125 from oxidation and/or corrosion.

[0016] In an embodiment there is horizontal separation between the edges of hardmask 130 and top MTJ 125 films compared to the edges of tunnel barrier 135 and bottom MTJ 140 films. This horizontal separation provides a margin with respect to top MTJ-to-bottom MTJ shorting.

[0017] An embodiment includes remnants of etch-stop film 115 on the edges of tunnel barrier 135 and bottom MTJ 140 films. Film 115 protects tunnel barrier film 135 and bottom MTJ films 140 from sidewall oxidation and/or corrosion.

[0018] An embodiment retains the same regular low-k ILD material 155, 170, 185 in logic area 105 (e.g., processor) and memory layer 110 that includes embedded MTJs. Doing so helps the embodiment meet stringent RC delay requirements of modern high performance logic chips. However, area 110 also includes flowable oxide layer 145, which provides an ILD not found in area 105 (or at least portions of area 105).

[0019] Figure 1 shows four elements: (1) sidewall spacer 120, (2) horizontal separation between the edges of hardmask 130 and top MTJ 125 films compared to the edges of tunnel barrier 135 and bottom MTJ 140 films, (3) remnants of etch-stop film 115 on the edges of tunnel barrier 135 and bottom MTJ 140 films, and (4) the same regular low-k ILD material 155, 170, 185 in logic area 105 (e.g., processor) and memory layer 110, other embodiments need not include all of these elements. Other embodiments may include any combination or subset of these four elements such as, for example, elements (1) and (2) but not elements (3) and/or (4).

[0020] Figures 2-16 depict a process for fabricating a logic chip area 105 including an embedded MTJ area 110 in an embodiment of the invention. In Figure 2 the process sequence begins with wafer 195 on which the topmost surface has a patterned interconnect layer within M1 layer 180. M1 layer 180 is included within ILD 185. For the purposes of discussion the process flow is shown beginning with a wafer having a patterned M1 interconnect on its topmost surface, but the topmost

surface could be some other interconnect layer (i.e. M2, M3, M4 and the like). Wafer 195 may also have other back-end and front-end layers 190 beneath the topmost patterned interconnect layers.

[0021] In Figure 3 the MTJ metal film stack (layers 140, 135, 125) is deposited followed by the deposition of hardmask material 130. In an embodiment the method of depositing the MTJ metal film stack is physical vapor deposition (PVD) sputtering. In an embodiment bottom MTJ film 140 consists of (from bottom to top) 3 nm tantalum (Ta); 20 nm platinum manganese (PtMn); 2.3 nm cobalt iron ($Co_{70}Fe_{30}$); 0.8 nm Ruthenium (Ru); 2.5 nm cobalt iron boron ($Co_{60}Fe_{20}B_{20}$), tunnel barrier 135 includes 1.2 nm magnesium oxide (MgO), top MTJ 125 film includes 2.5 nm $Co_{60}Fe_{20}B_{20}$; and hardmask 130 material includes 50 nm Ta. In such an embodiment the hardmask (1) can be deposited sequentially within the same sputter tool that is used for depositing the MTJ metal film stack, and (2) is conductive. Regarding the sputter tool, since all films in the hardmask, top MTJ, tunnel barrier, and bottom MTJ are sputtered films, all of those films may be deposited sequentially inside one sputter tool without breaking vacuum. An advantage of not breaking vacuum is that the surfaces of the various metal films do not oxidize, and hence there is little to no deterioration of the electrical properties of the MTJ layers. Regarding the conductive nature of the hardmask, as a result of the conductivity of the hardmask the hardmask does not need to be removed later in the flow when an electrical connection needs to be made to the top surface of the MTJ. Other embodiments have other thicknesses for bottom MTJ 140, tunnel barrier 135, and/or top MTJ 125 to alter the MTJ electrical characteristics as desired. Likewise, other materials may be used in bottom MTJ 140, tunnel barrier 135, top MTJ 125, and hardmask 130 to obtain different MTJ electrical characteristics, as desired.

[0022] In Figure 4 resist layer 112 is applied and patterned over those areas of the wafer surface where MTJs are desired (area 110).

[0023] In Figure 5 exposed hardmask 130 material is etched using, for example, dry etch techniques and any remaining resist is removed using, for example, a plasma ash process. In Figure 6, top MTJ film 125 is etched using, for example, RIE dry etch techniques, stopping at tunnel barrier 135 material. In Figure 7 the wafer

surface is covered with “spacer” 120 film, such as, for example, silicon nitride, silicon oxide, silicon oxynitride, silicon carbide, or carbon doped silicon nitride. In Figure 8 an anisotropic dry etch process is used to remove spacer 120 material from all of the horizontal surfaces of the wafer while leaving the spacer material on the vertical sidewalls. In Figure 9 tunnel barrier 135 and bottom MTJ films 140 are etched using, for example, RIE dry etch techniques, stopping on the underlying M1 180 interconnect and/or ILD 185 materials. In Figure 10 the wafer surface is covered with etch-stop material 115, such as silicon nitride or silicon carbide. Note that film 115 acts as a flowable oxide etch stop, and it protects the etched sidewalls of the tunnel barrier and bottom MTJ films from oxidation/corrosion.

[0024] In one embodiment the processes corresponding to Figures 5-10 occur in-situ in a large cluster tool without breaking vacuum in order to minimize any chance of oxidation or corrosion of the etched MTJ sidewalls.

[0025] In Figure 11 the wafer surface is covered with flowable oxide material 145, which may fill any gaps between MTJs. In one embodiment flowable oxide material 145 may include polymer hydrogen silsesquioxane (HSQ) solution in methyl isobutyl ketone (MIBK), but other embodiments are not so limited.

[0026] In Figure 12 flowable oxide 145 overburden is removed using, for example, a dry etchback process. In an embodiment flowable oxide material 145 remains in the gaps between the MTJs.

[0027] In Figure 13 low-k ILD material 170 is deposited. In an embodiment, ILD material 170 will ultimately remain in the area of the wafer where the logic circuits are located (area 105). Areas 105, 110 may be identified in a variety of ways. For example, area 110 may include a STT-RAM bit cell array where MTJs are visible and a fairly regular bit cell transistor layout is present. In contrast, the transistor layout in area 105 is not so regular (e.g., not included in a repetitively structured array as is the case with memory) and few to no MTJs are present. ILD 170 satisfies various technical requirements for ILD material(s) used in the corresponding interconnect layer of area 105. Such technical requirements may concern, for example, electrical properties (e.g., dielectric constant, breakdown voltage) and/or mechanical

properties (e.g., modulus, toughness, film stress) dictated by design concerns for area 105. In various embodiments etch-stop materials include, for example, silicon nitride, silicon carbide, carbon-doped silicon nitride, and the like. ILD material 170 may be any ILD material whose properties are suitable for use in the logic circuits and interconnect layer of area 105. Embodiments include ILD materials such as, for example, silicon oxide, fluorinated silicon oxide (SiOF), and carbon-doped oxide.

[0028] In Figure 14, the low-k ILD film 170 is planarized (polished). In Figure 15 trenches and via openings are fabricated into low-k ILD material 170 using, for example, dual damascene patterning. In Figure 16 copper interconnect structures are formed inside the trenches and via openings using, for example, dual damascene barrier/seed deposition, copper electroplating, and copper CMP processes.

[0029] The process then produces the device included in Figure 1, wherein subsequent etch stop 160 is formed and copper interconnect layer(s) 123 are formed in M3 layer 150. Furthermore, ILD layer(s) 155 are formed, as desired, using, for example, dual damascene process techniques.

[0030] Figure 18 includes a less idealized version of a portion of Figure 1. In Figure 18 tunnel barrier 1835 is located between bottom MTJ layer 1840 and top MTJ layer 1825. Spacer 1820 is vertically adjacent layer 1835 and horizontally adjacent layer 1825 and hardmask 1830.

[0031] Another embodiment utilizes a different process and end product. The process and embodiments of Figures 2-10 are used. However, going forward from the product of Figure 10 the process differs. At that point a low-k ILD material is deposited onto the wafer to a thickness in the logic areas approximately equal to that of the height of the MTJ's, followed by a hardmask film. This ILD material occupies the area of the wafer where the logic circuits are located (e.g., a processor in area 105) and consequently includes the properties for an ILD material used in the logic circuits at that specific interconnect layer. Suitable ILD materials include, for example, silicon oxide, SiOF, and carbon-doped oxide. Suitable hardmask films include, for example, titanium nitride and silicon nitride.

[0032] Next, a resist layer is applied and patterned to mask off logic circuit area 105 from area 110 where MTJs are located. The exposed hardmask layer is etched, stopping on the low-k ILD film, and then the exposed low-k ILD material is etched, stopping on the underlying etch-stop film (layer 175). The hardmask and low-k ILD films are etched using, for example, dry etch process techniques. Then the resist residue is removed.

[0033] Afterwards, the wafer surface is covered with a flowable oxide material (material 145), which fills the gaps in between the MTJs. Flowable oxide overburden is then removed using, for example, an oxide CMP process that selectively stops on the underlying etch-stop material which was formed at the beginning of this alternative method. The flowable oxide material remains inside the gaps in between the MTJs.

[0034] Next the exposed etch-stop material is removed using, for example, a wet or dry etch process (depending on the film composition). Additional low-k ILD material is deposited onto the wafer, such that the total low-k ILD thickness is built up to the value desired for forming the regular interconnect structures in the logic circuit area (area 105). This value is highly variable and depends on, for example, which metal layer the MTJs are integrated into. In one embodiment, the total low-k ILD thickness may be between 30 - 750 nm, including 50, 100, 200, 300, 400, 500, 600, 700 nm thicknesses. Trenches and via openings are then fabricated into the low-k ILD material using, for example, dual damascene patterning and etching techniques. Copper interconnect structures are then formed inside the trenches and via openings using, for example, dual damascene barrier/seed deposition, copper electroplating, and copper CMP processes. Subsequent copper interconnect layer(s) are formed, as desired, using dual damascene process techniques. Figure 17 includes a product resultant from the alternative embodiment. Figure 17 is similar to Figure 1, however certain flowable oxide portions 145 have a different shape and etch stop 115 no longer “wraps” over portions of the MTJs.

[0035] Although the alternate embodiment has more total process steps compared to the embodiment of Figures 2-16, the alternate embodiment avoids the low-k ILD polish process (see Figure 14).

[0036] In an embodiment an incoming wafer may include patterned copper interconnects fabricated using standard copper damascene processing (e.g., Figure 2). In such a case the entire wafer surface is planar. In some embodiments the MTJ film stack (e.g., Figure 3) is opaque to a scanner alignment system and there may be no alignment "feature" for the scanner to align the MTJ pattern to the prior layer on the wafer. In such a case an additional masking layer may be used to create a scanner alignment mark in the scribe area for aligning the MTJ resist pattern to the underlying substrate (Figure 4).

[0037] Accordingly, various processes have been addressed above, any of which may result in the embodiment of Figure 1.

[0038] Various embodiments (e.g., Figures 1 and 17) depict a cross-section of a device having: (a) different ILD materials in the logic area as opposed to the MTJ array area. For example, a single horizontal plane intersects the 3 MTJs, ILD 170, as well as ILD portions in logic area 105. The ILD portions in logic area 105 may include ILD materials different from that of ILD 170 located in area 110. For example, the ILD portions in logic area 105 may include silicon oxide ILD materials and the ILD portions in MTJ area 110 may include flowable oxide. However, in other embodiments the ILD materials may be the same.

[0039] Various embodiments (e.g., Figures 1 and 17) depict a cross-section of a device having: (b) presence of a sidewall spacer on the edges of the patterned hardmask and/or top MTJ films. For example, there are 3 MTJs shown in Figure 1. The top MTJ layer 125 for each of the MTJs is located adjacent two vertical spacer portions (sidewall spacers). These sidewall spacers are also adjacent and on the edge of the hardmask portions that are atop the 3 MTJs. However, in other embodiments the spacers may be directly adjacent and contacting only one of the top MTJ and hardmask layers.

[0040] Various embodiments (e.g., Figures 1 and 17) depict a cross-section of a device having: (c) horizontal separation between the edges of the top MTJ films compared to the edges of the tunnel barrier and the bottom MTJ films. For example, for each MTJ the overall horizontal width of the top MTJ layer is less than the overall

width of the corresponding tunnel barrier and/or the overall horizontal width of the top MTJ layer is less than the overall width of the corresponding bottom MTJ layer. The differential between the width of the tunnel barrier and top MTJ layer is equal to the width of the two spacer sidewalls. The differential between the width of the bottom MTJ layer and top MTJ layer is equal to the width of the two spacer sidewalls. In some embodiments the bottom MTJ layer and the tunnel barrier have the same widths for some or all MTJs but in other embodiments they are not the same for some or all MTJs.

[0041] Various embodiments (e.g., Figures 1 and 17) depict a cross-section of a device having: (d) remnants of the etch-stop film on the edges of the tunnel barrier and bottom MTJ films. For example, there are 3 MTJs shown in Figure 1. The tunnel barrier and/or bottom MTJ layer 140 for each of the MTJs is located adjacent and directly contacting etch stop portions. The etch stop portions may be vertical portions. These vertical etch stop portions may also be adjacent portions of vertical sidewall spacers.

[0042] Embodiments may have various combinations such as any combination of the immediately aforementioned elements (a), (b), (c), and/or (d).

[0043] As used herein a layer may have sublayers. For example, a top MTJ layer may actually be composed of many sublayers. For example and as explained above, in one embodiment MTJ film 140 consists of (from bottom to top) 3 nm tantalum (Ta); 20 nm platinum manganese (PtMn); 2.3 nm cobalt iron ($Co_{70}Fe_{30}$); 0.8 nm Ruthenium (Ru); 2.5 nm cobalt iron boron ($Co_{60}Fe_{20}B_{20}$). Thus, 5 sublayers are included in MTJ film 140. Tunnel barrier 135 includes 1.2 nm magnesium oxide (MgO) but in alternative embodiments layer 135 may include one or more sublayers. Top MTJ 125 film includes 2.5 nm $Co_{60}Fe_{20}B_{20}$ but in alternative embodiments the layer may include one or more sublayers. Hardmask 130 material includes 50 nm Ta but in alternative embodiments the layer may include tantalum nitride, titanium and titanium nitride and/or one or more sublayers. For example, an embodiment may include a top MTJ film with sublayers (1.7 nm Co60Fe20B20 / 5 nm Ta / 5 nm Ru), a tunnel barrier (0.85 nm MgO), and a bottom MTJ film with sublayers (5nm Ta / 1nm Co60Fe20B20). Another embodiment may include a top MTJ film with sublayers

(1.0 - 1.7 nm Co60Fe20B20 / 5 nm Ta / 5 nm Ru), a tunnel barrier (0.85 – 0.9 nm MgO), and a bottom MTJ film with sublayers (5nm Ta / 10nm Ru / 5nm Ta/ 1.0 – 1.3 nm $Co_{60}Fe_{20}B_{20}$). Another embodiment may include a top MTJ film with sublayers (CoFeB), a tunnel barrier (MgO), and a bottom MTJ film with sublayers (PtMn / CoFe/ Ru / CoFeB). Another embodiment may include a top MTJ film with sublayers (CoFeB(3nm) / Ru(7nm) / Cu(110nm) / Ru(2nm) / Ta(10nm) or CoFeB(3nm) / Ta(8nm) / Ru(7nm)), a tunnel barrier with sublayers (Mg(0.4nm) + MgO(0.6nm)), and a bottom MTJ film with sublayers (Ta(5nm) / CuN(20nm) / Ta(10nm) / PtMn(15nm) / CoFe(2.5nm) / Ru(0.8nm) / CoFeB(3nm)). Many other examples are possible and understood to those of ordinary skill in the art and are not described herein for purposes of brevity.

[0044] Embodiments may be used in many different types of systems. For example, in one embodiment a communication device (e.g., cell phone, Smartphone, netbook, notebook, personal computer, watch, camera) can be arranged to include various embodiments described herein. Referring now to Figure 19, shown is a block diagram of a system in accordance with an embodiment of the present invention. Multiprocessor system 700 is a point-to-point interconnect system, and includes a first processor 770 and a second processor 780 coupled via a point-to-point interconnect 750. Each of processors 770 and 780 may be multicore processors. First processor 770 may include a memory controller hub (MCH) and point-to-point (P-P) interfaces. Similarly, second processor 780 may include a MCH and P-P interfaces. The MCHs may couple the processors to respective memories, namely memory 732 and memory 734, which may be portions of main memory (e.g., a dynamic random access memory (DRAM)) locally attached to the respective processors. However, the processors may be located on the same chip as memory as described herein. First processor 770 and second processor 780 may be coupled to a chipset 790 via P-P interconnects, respectively. Chipset 790 may include P-P interfaces. Furthermore, chipset 790 may be coupled to a first bus 716 via an interface. Various input/output (I/O) devices 714 may be coupled to first bus 716, along with a bus bridge 718, which couples first bus 716 to a second bus 720. Various devices may be coupled to second bus 720 including, for example, a keyboard/mouse 722, communication devices 726, and data storage unit 728 such

as a disk drive or other mass storage device, which may include code 730, in one embodiment. Code may be included in one or more memories including memory 728, 732, 734, memory coupled to system 700 via a network, and the like. Further, an audio I/O 724 may be coupled to second bus 720.

[0045] Notably, at times herein "top MTJ" and "bottom MTJ" layers are used for purposes of explanation, however, a MTJ can be "inverted" making the top layer into the bottom layer (i.e., changing the viewing perspective) without deviating from innovative concepts of embodiments described herein.

[0046] As a further example, at least one machine readable medium comprises a plurality of instructions that in response to being executed on a computing device, cause the computing device to carry out any of the methods described herein. An apparatus for processing instructions may be configured to perform the method of any of the methods described herein. And an apparatus may further include means for performing any of the methods described herein.

[0047] Embodiments may be implemented in code and may be stored on a machine readable storage medium having stored thereon instructions which can be used to program a system to perform the instructions. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0048] The following examples pertain to further embodiments.

[0049] Example 1 includes an apparatus comprising: a monolithic substrate; a memory area, comprising a magnetic tunnel junction (MTJ) that includes a tunnel barrier directly contacting lower and upper MTJ layers, located on the substrate; and a logic area located on the substrate; wherein a horizontal plane, which is parallel to

the tunnel barrier, intersects the MTJ, a first Inter-Layer Dielectric (ILD) material adjacent the MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another; wherein the first and second ILDs directly contact one another.

[0050] In Example 2, the subject matter of Examples 1 can optionally include wherein the upper MTJ layer includes an upper MTJ layer sidewall and the lower MTJ layer includes a lower MTJ sidewall horizontally offset from the upper MTJ layer sidewall by a horizontal offset space that defines a horizontal offset distance.

[0051] In Example 3, the subject matter of Examples 1-2 can optionally include a spacer, having a width equal to the horizontal offset distance, directly contacting the upper MTJ layer and the tunnel barrier.

[0052] In Example 4, the subject matter of Examples 1-3 can optionally include a hardmask directly contacting an upper surface of the upper MTJ layer and the spacer.

[0053] In Example 5, the subject matter of Examples 1-4 can optionally include wherein the horizontal plane intersects etch stop material included between the MTJ and the first ILD material; and the etch stop material is included in an etch stop layer that directly contacts the hardmask.

[0054] In Example 6, the subject matter of Examples 1-5 can optionally include wherein the horizontal plane intersects etch stop material included between the MTJ and the first ILD material; and the etch stop material is included in an etch stop layer that directly contacts an upper surface of the spacer.

[0055] In Example 7, the subject matter of Examples 1-6 can optionally include wherein the horizontal plane intersects etch stop material included between the MTJ and the first ILD material.

[0056] In Example 8, the subject matter of Examples 1-6 can optionally include wherein the etch stop material directly contacts at least one of the tunnel barrier and the lower MTJ layer.

[0057] In Example 9, the subject matter of Examples 1-8 can optionally include wherein the etch stop material is included in an etch stop layer having directly connected horizontal and vertical lengths that both directly contact the first ILD.

[0058] In Example 10, the subject matter of Examples 1-9 can optionally include wherein the etch stop material is included in an etch stop layer extends from the memory area to the logic area.

[0059] In Example 11, the subject matter of Examples 1-10 can optionally include wherein: the first ILD material includes at least one of silicon oxide, silicon oxynitride, porous silicon oxide, fluorinated silicon oxide, carbon-doped oxide, porous carbon-doped oxide, polyimide, polynorbornene, benzocyclobutene, flowable oxide, and polytetrafluoroethylene and the second ILD material includes an additional at least one of silicon oxide, silicon oxynitride, porous silicon oxide, fluorinated silicon oxide, carbon-doped oxide, porous carbon-doped oxide, polyimide, polynorbornene, benzocyclobutene, flowable oxide, and polytetrafluoroethylene; and the first bottom MTJ includes sublayers comprising at least two of tantalum, platinum manganese; cobalt iron; Ruthenium (Ru); and cobalt iron boron.

[0060] In Example 12, the subject matter of Examples 1-11 can optionally include wherein the logic area is included in a processor and the memory is spin torque transfer magnetoresistive random access memory (STT-MRAM).

[0061] In Example 13, the subject matter of Examples 1-12 can optionally include wherein at least one of the first upper MTJ layer, first lower MTJ layer, and first tunnel barrier includes sublayers.

[0062] In Example 14, the subject matter of Examples 1-13 can optionally include the memory area comprises an additional MTJ, having a additional tunnel barrier directly contacting additional lower and upper MTJ layers, located on the substrate; and the horizontal plane intersects the additional MTJ; a contiguous etch stop portion directly contacts both the MTJ and the additional MTJ.

[0063] In Example 15, the subject matter of Examples 1-14 can optionally include wherein the contiguous etch stop portion directly contacts the first ILD.

[0064] Example 16 includes a method comprising: forming a memory area, comprising a magnetic tunnel junction (MTJ) that includes a tunnel barrier directly contacting lower and upper MTJ layers, on a monolithic substrate; and forming a logic area located on the substrate; wherein a horizontal plane, which is parallel to the tunnel barrier, intersects the MTJ, a first Inter-Layer Dielectric (ILD) material adjacent the MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another.

[0065] In Example 17, the subject matter of Example 16 can optionally include forming a sidewall of the upper MTJ layer horizontally offset a horizontal offset distance from a sidewall of the lower MTJ layer.

[0066] In Example 18, the subject matter of Examples 16-17 can optionally include forming a hardmask directly contacting an upper surface of the upper MTJ layer; and forming a spacer, having a width equal to the horizontal offset distance, in direct contact with the upper MTJ layer and the hardmask.

[0067] In Example 19, the subject matter of Examples 16-18 can optionally include forming a spacer, having a width equal to the horizontal offset distance, in direct contact with the upper MTJ layer and the tunnel barrier.

[0068] In Example 20, the subject matter of Examples 16-19 can optionally include forming an etch stop layer directly contacting the MTJ and forming the first ILD in direct contact with the etch stop; forming the second ILD in direct contact with the first ILD and the etch stop; and polishing the second ILD while the second ILD is in direct contact with the first ILD.

[0069] In Example 21, the subject matter of Examples 16-20 can optionally include forming an etch stop layer directly contacting the MTJ and forming the second ILD in direct contact with the etch stop; forming the first ILD in direct contact with the second ILD and the etch stop; and polishing the first ILD while the first ILD is in direct contact with the second ILD.

[0070] Example 22 includes an apparatus comprising: a first magnetic tunnel junction (MTJ) including a first upper MTJ layer, a first lower MTJ layer, and a first tunnel barrier directly contacting a first lower surface of the first upper MTJ layer and

a first upper surface of the first lower MTJ layer; a memory area, including the first MTJ, and a logic area form on a monolithic substrate; wherein the first upper MTJ layer includes a first upper MTJ layer sidewall and the first lower MTJ layer includes a first lower MTJ sidewall horizontally offset from the first upper MTJ layer sidewall by a first horizontal offset space that defines a first horizontal offset distance; wherein a first spacer, having a width equal to the first horizontal offset distance, directly contacts the first upper MTJ layer and the first tunnel barrier; wherein a first horizontal plane, parallel to the first lower surface of the first upper MTJ layer, intersects the first MTJ, a first ILD material adjacent the first MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another.

[0071] In Example 23, the subject matter of Example 22 can optionally include wherein the first horizontal plane intersects a first polish stop material included between the first MTJ and the first ILD material.

[0072] In Example 24, the subject matter of Examples 22-23 can optionally include a first hardmask directly contacting a first upper surface of the first upper MTJ layer and the first spacer.

[0073] In Example 25, the subject matter of Examples 22-24 can optionally include wherein the first ILD material includes flowable oxide and the second ILD material includes at least one of silicon oxide, porous silicon oxide, fluorinated silicon oxide, carbon-doped oxide, porous carbon-doped oxide, polyimide, polynorbornene, benzocyclobutene, and polytetrafluoroethylene.

[0074] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. An apparatus comprising:
a monolithic substrate;
a memory area, comprising a magnetic tunnel junction (MTJ) that includes a tunnel barrier directly contacting lower and upper MTJ layers, located on the substrate; and
a logic area located on the substrate;
wherein a horizontal plane, which is parallel to the tunnel barrier, intersects the MTJ, a first Inter-Layer Dielectric (ILD) material adjacent the MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another;
wherein the first and second ILDs directly contact one another.

2. The apparatus of claim 1, wherein the upper MTJ layer includes an upper MTJ layer sidewall and the lower MTJ layer includes a lower MTJ sidewall horizontally offset from the upper MTJ layer sidewall by a horizontal offset space that defines a horizontal offset distance.

3. The apparatus of claim 2 comprising a spacer, having a width equal to the horizontal offset distance, directly contacting the upper MTJ layer and the tunnel barrier.

4. The apparatus of claim 3 further comprising a hardmask directly contacting an upper surface of the upper MTJ layer and the spacer.

5. The apparatus of claim 4 wherein the horizontal plane intersects etch stop material included between the MTJ and the first ILD material; and the etch stop material is included in an etch stop layer that directly contacts the hardmask.

6. The apparatus of claim 3 wherein the horizontal plane intersects etch stop material included between the MTJ and the first ILD material; and the etch stop

material is included in an etch stop layer that directly contacts an upper surface of the spacer.

7. The apparatus of claim 1 wherein the horizontal plane intersects etch stop material included between the MTJ and the first ILD material.

8. The apparatus of claim 7 wherein the etch stop material directly contacts at least one of the tunnel barrier and the lower MTJ layer.

9. The apparatus of claim 7 wherein the etch stop material is included in an etch stop layer having directly connected horizontal and vertical lengths that both directly contact the first ILD.

10. The apparatus of claim 7 wherein the etch stop material is included in an etch stop layer that extends from the memory area to the logic area.

11. The apparatus of claim 1, wherein:

the first ILD material includes at least one of silicon oxide, silicon oxynitride, porous silicon oxide, fluorinated silicon oxide, carbon-doped oxide, porous carbon-doped oxide, polyimide, polynorbornene, benzocyclobutene, flowable oxide, and polytetrafluoroethylene and the second ILD material includes an additional at least one of silicon oxide, silicon oxynitride, porous silicon oxide, fluorinated silicon oxide, carbon-doped oxide, porous carbon-doped oxide, polyimide, polynorbornene, benzocyclobutene, flowable oxide, and polytetrafluoroethylene; and

the first bottom MTJ includes sublayers comprising at least one of tantalum, platinum manganese; cobalt iron; Ruthenium (Ru); and cobalt iron boron.

12. The apparatus of claim 1, wherein the logic area is included in a processor and the memory is spin torque transfer magnetoresistive random access memory (STT-MRAM).

13. The apparatus of claim 1, wherein at least one of the first upper MTJ layer, first lower MTJ layer, and first tunnel barrier includes sublayers.

14. The apparatus of claim 1 wherein:

the memory area comprises an additional MTJ, having a additional tunnel barrier directly contacting additional lower and upper MTJ layers, located on the substrate;

the horizontal plane intersects the additional MTJ; and

a contiguous etch stop portion directly contacts both the MTJ and the additional MTJ.

15. The apparatus of claim 1 wherein the contiguous etch stop portion directly contacts the first ILD.

16. A method comprising:

forming a memory area, comprising a magnetic tunnel junction (MTJ) that includes a tunnel barrier directly contacting lower and upper MTJ layers, on a monolithic substrate; and

forming a logic area located on the substrate;

wherein a horizontal plane, which is parallel to the tunnel barrier, intersects the MTJ, a first Inter-Layer Dielectric (ILD) material adjacent the MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another.

17. The method of claim 16 comprising forming a sidewall of the upper MTJ layer horizontally offset a horizontal offset distance from a sidewall of the lower MTJ layer.

18. The method of claim 17 comprising:

forming a hardmask directly contacting an upper surface of the upper MTJ layer; and

forming a spacer, having a width equal to the horizontal offset distance, in direct contact with the upper MTJ layer and the hardmask;

wherein forming the hardmask and the spacer includes forming the hardmask and the spacer under a single vacuum without discontinuing the single vacuum between forming the hardmask and the spacer.

19. The method of claim 17 comprising forming a spacer, having a width equal to the horizontal offset distance, in direct contact with the upper MTJ layer and the tunnel barrier.

20. The method of claim 16 comprising:

forming an etch stop layer directly contacting the MTJ and forming the first ILD in direct contact with the etch stop;

forming the second ILD in direct contact with the first ILD and the etch stop; and

polishing the second ILD while the second ILD is in direct contact with the first ILD.

21. The method of claim 16 comprising:

forming an etch stop layer directly contacting the MTJ and forming the second ILD in direct contact with the etch stop;

forming the first ILD in direct contact with the second ILD and the etch stop; and

polishing the first ILD while the first ILD is in direct contact with the second ILD.

22. An apparatus comprising:

a first magnetic tunnel junction (MTJ) including a first upper MTJ layer, a first lower MTJ layer, and a first tunnel barrier directly contacting a first lower surface of the first upper MTJ layer and a first upper surface of the first lower MTJ layer;

a memory area, including the first MTJ, and a logic area form on a monolithic substrate;

wherein the first upper MTJ layer includes a first upper MTJ layer sidewall and the first lower MTJ layer includes a first lower MTJ sidewall horizontally offset from

the first upper MTJ layer sidewall by a first horizontal offset space that defines a first horizontal offset distance;

wherein a first spacer, having a width equal to the first horizontal offset distance, directly contacts the first upper MTJ layer and the first tunnel barrier;

wherein a first horizontal plane, parallel to the first lower surface of the first upper MTJ layer, intersects the first MTJ, a first ILD material adjacent the first MTJ, and a second ILD material included in the logic area, the first and second ILD materials being unequal to one another.

23. The apparatus of claim 22 wherein the first horizontal plane intersects a first polish stop material included between the first MTJ and the first ILD material.

24. The apparatus of claim 23 further comprising a first hardmask directly contacting a first upper surface of the first upper MTJ layer and the first spacer.

25. The apparatus of claim 24, wherein the first ILD material includes flowable oxide and the second ILD material includes at least one of silicon oxide, porous silicon oxide, fluorinated silicon oxide, carbon-doped oxide, porous carbon-doped oxide, polyimide, polynorbornene, benzocyclobutene, and polytetrafluoroethylene.

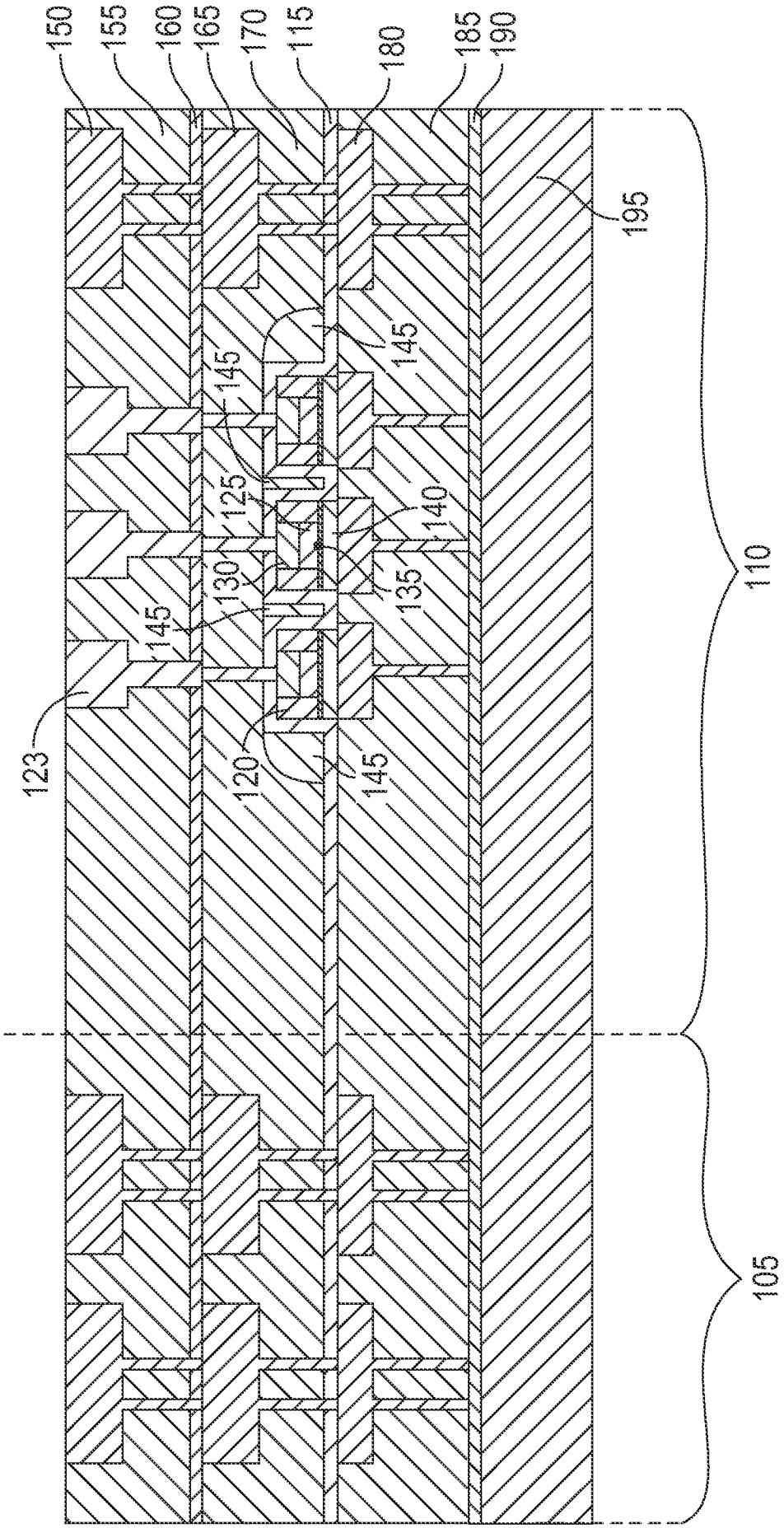

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FIG. 1

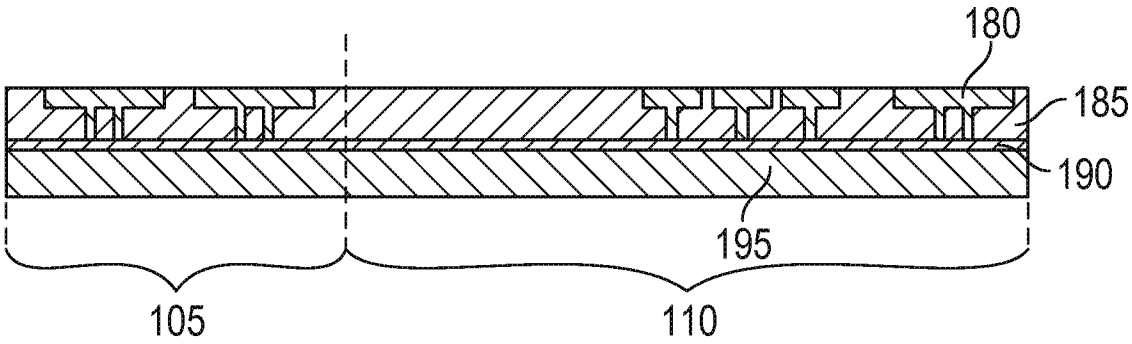


FIG. 2

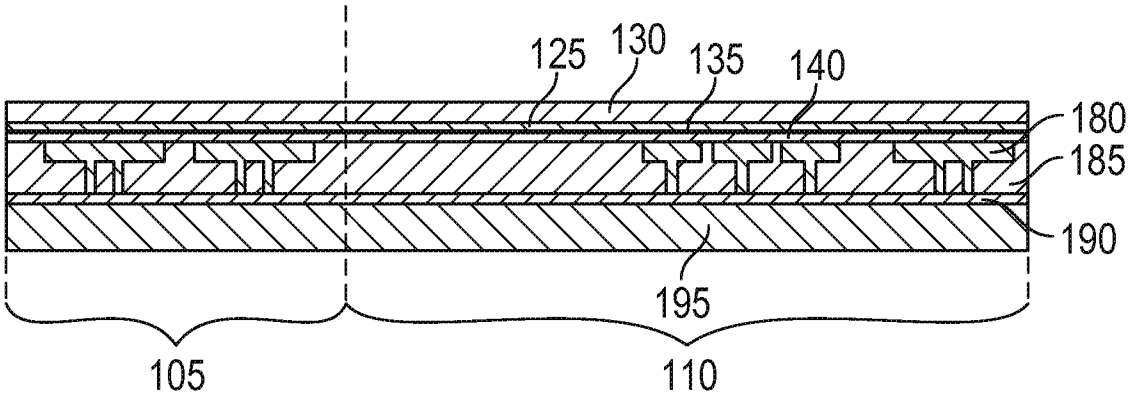


FIG. 3

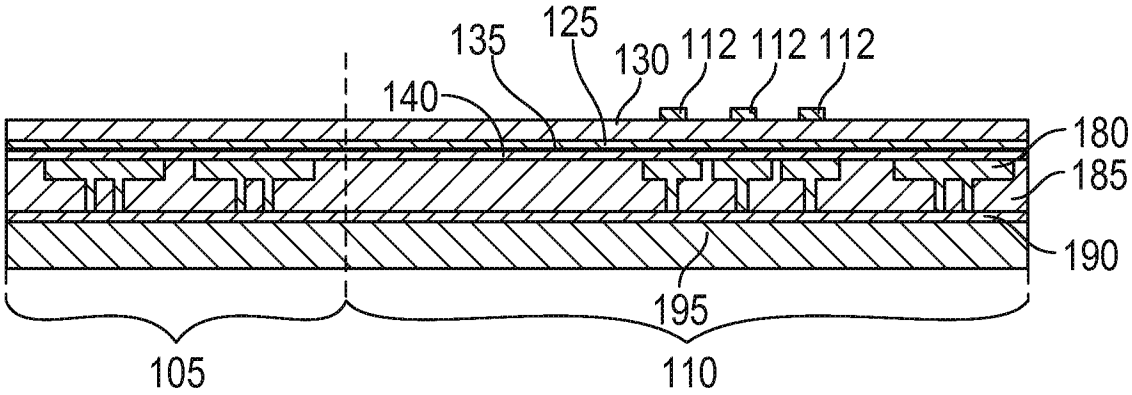


FIG. 4

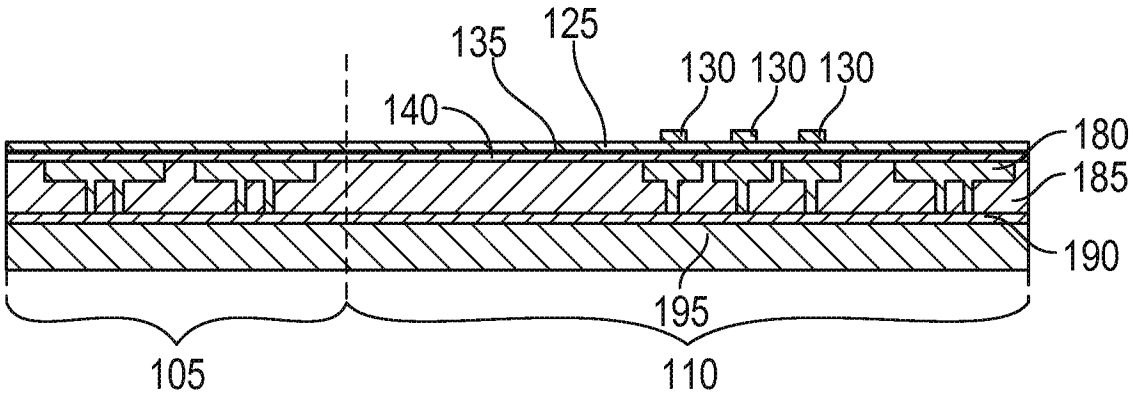


FIG. 5

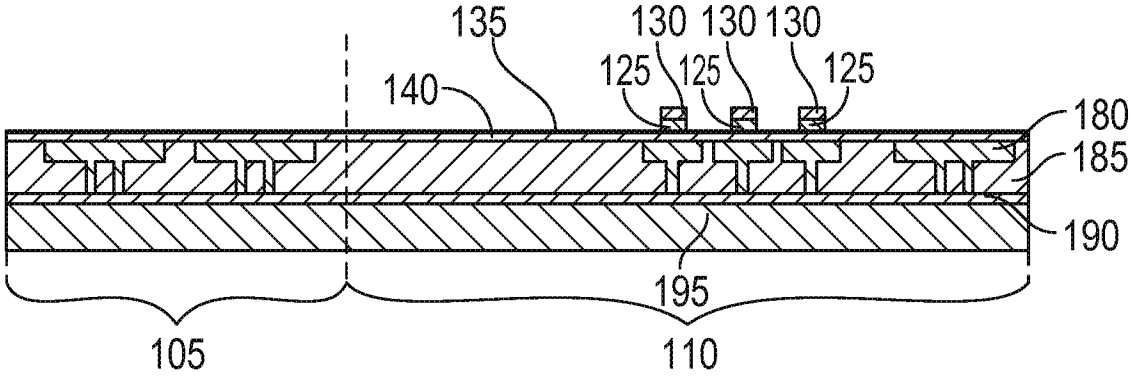


FIG. 6

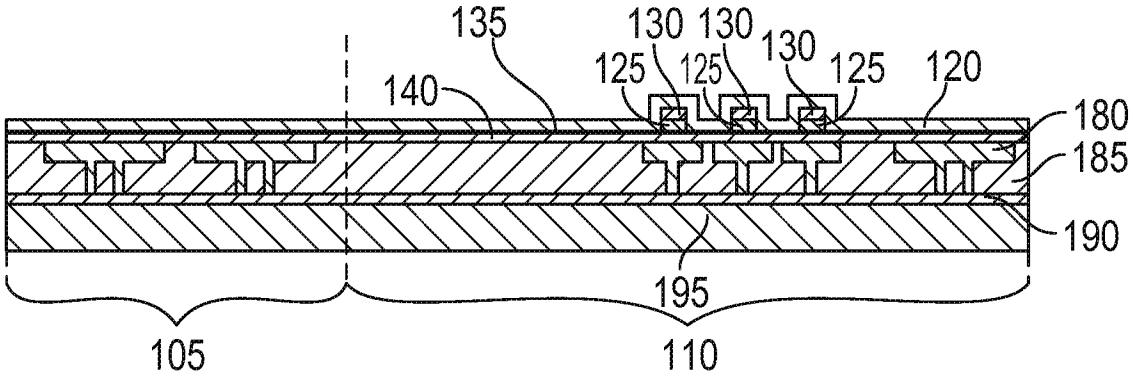


FIG. 7

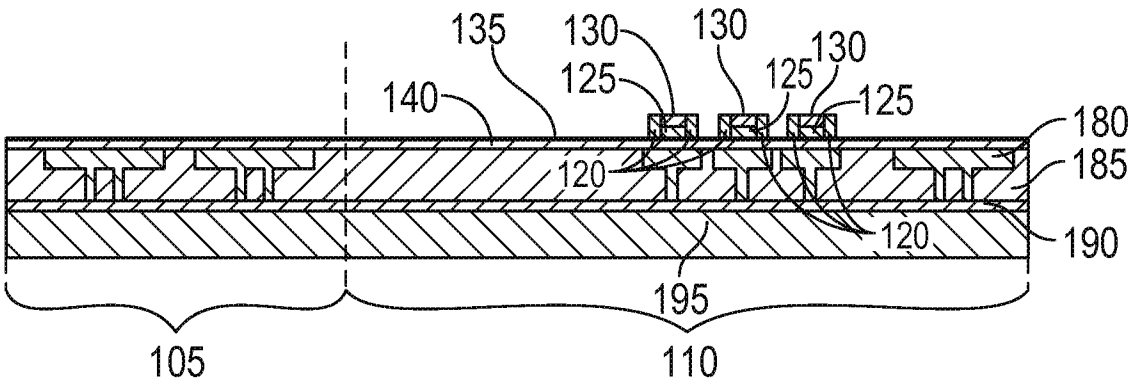


FIG. 8

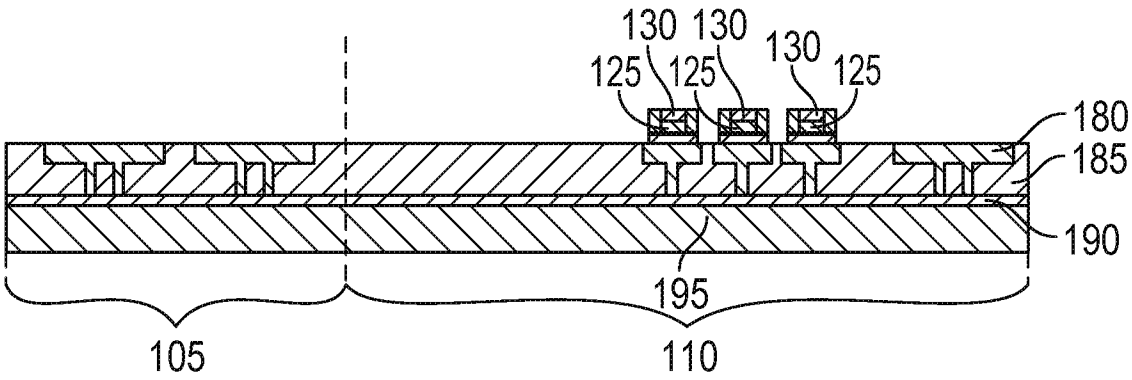


FIG. 9

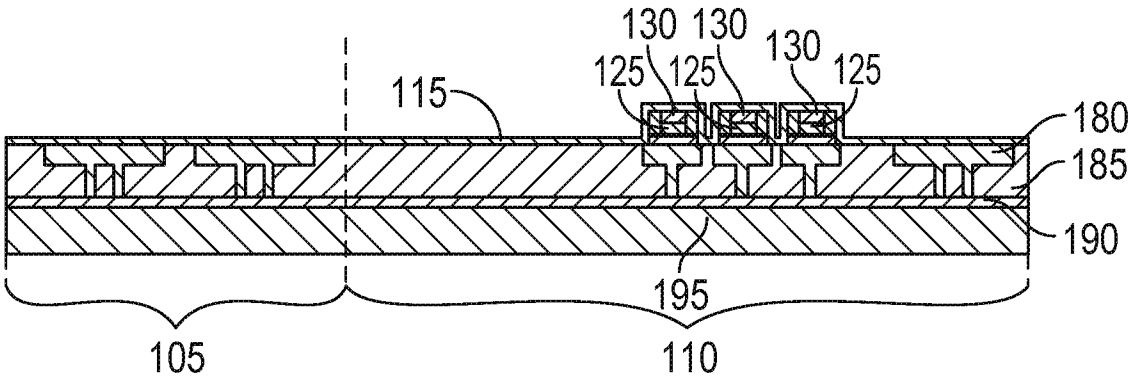


FIG. 10

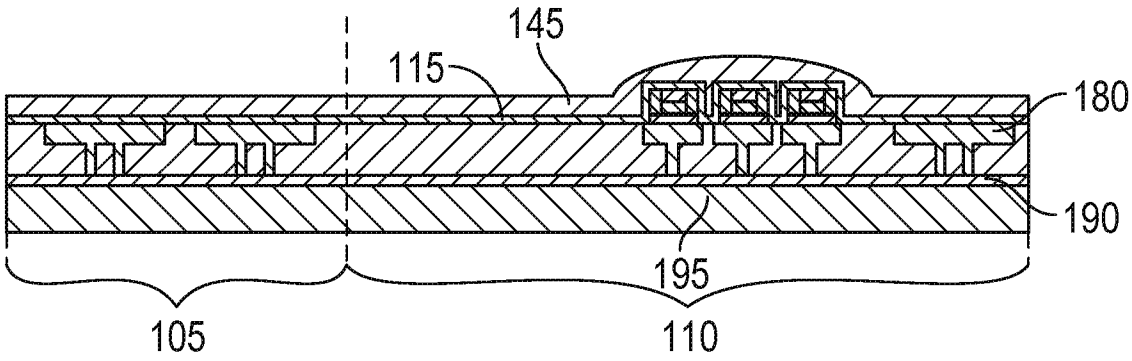


FIG. 11

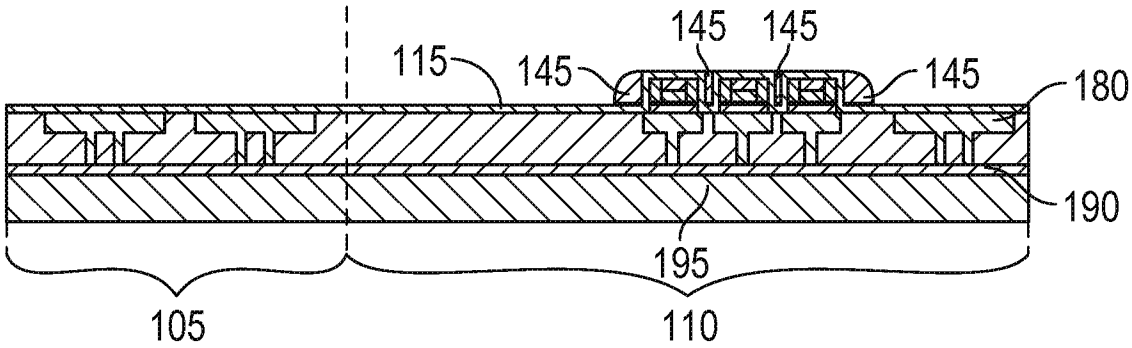


FIG. 12

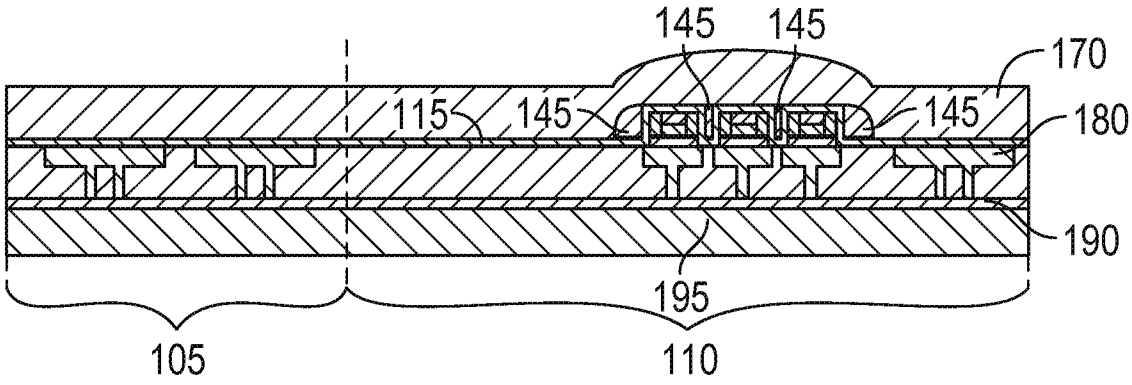


FIG. 13

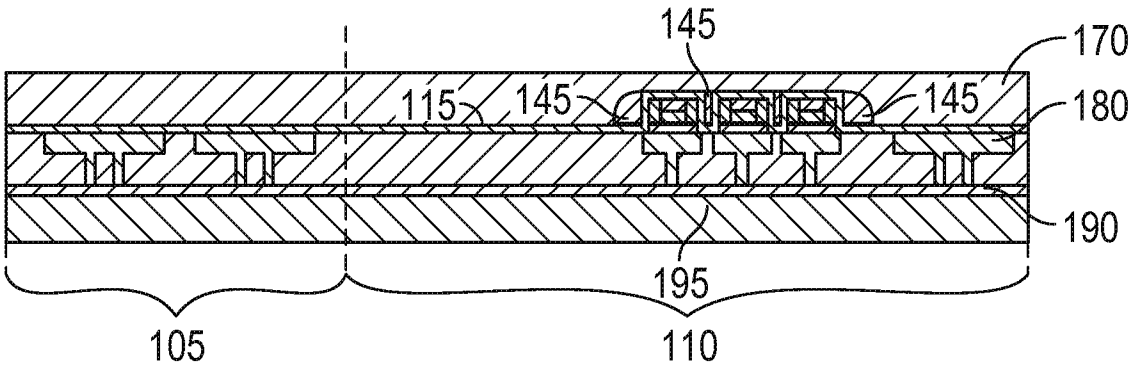


FIG. 14

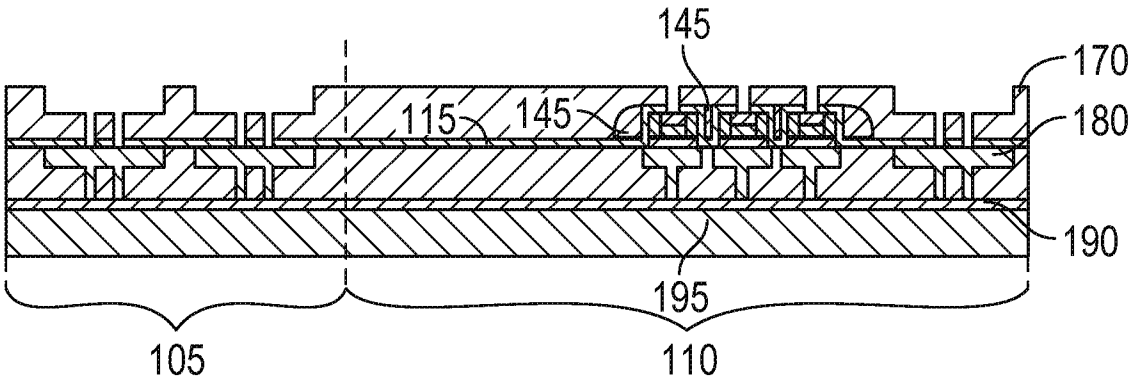


FIG. 15

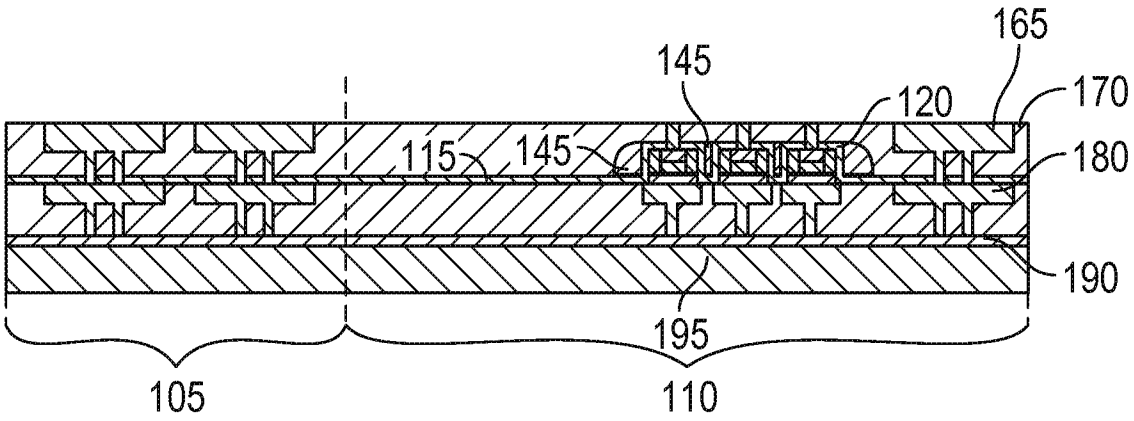


FIG. 16

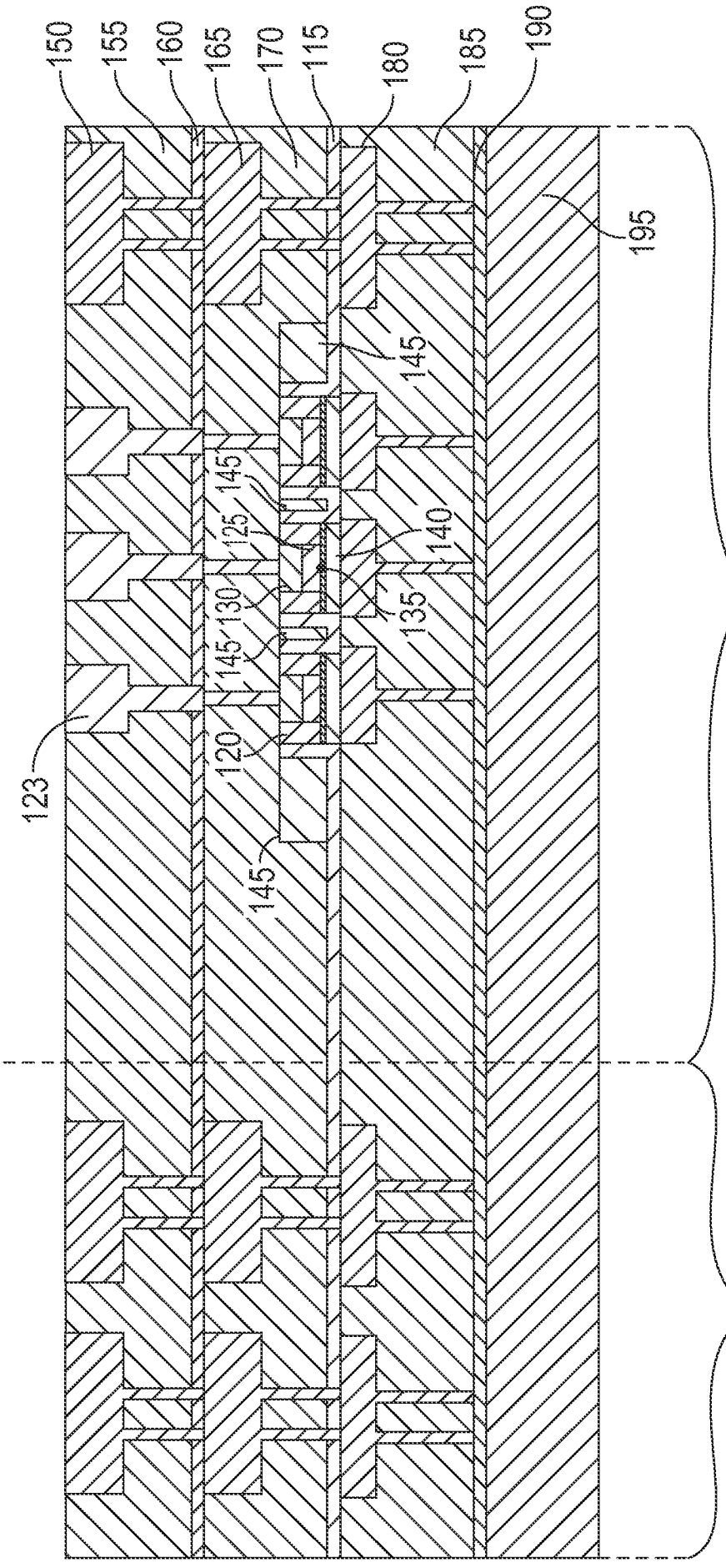

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FIG. 17

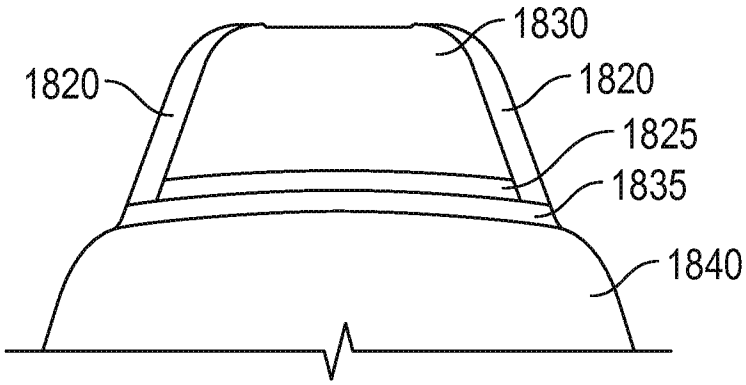


FIG. 18

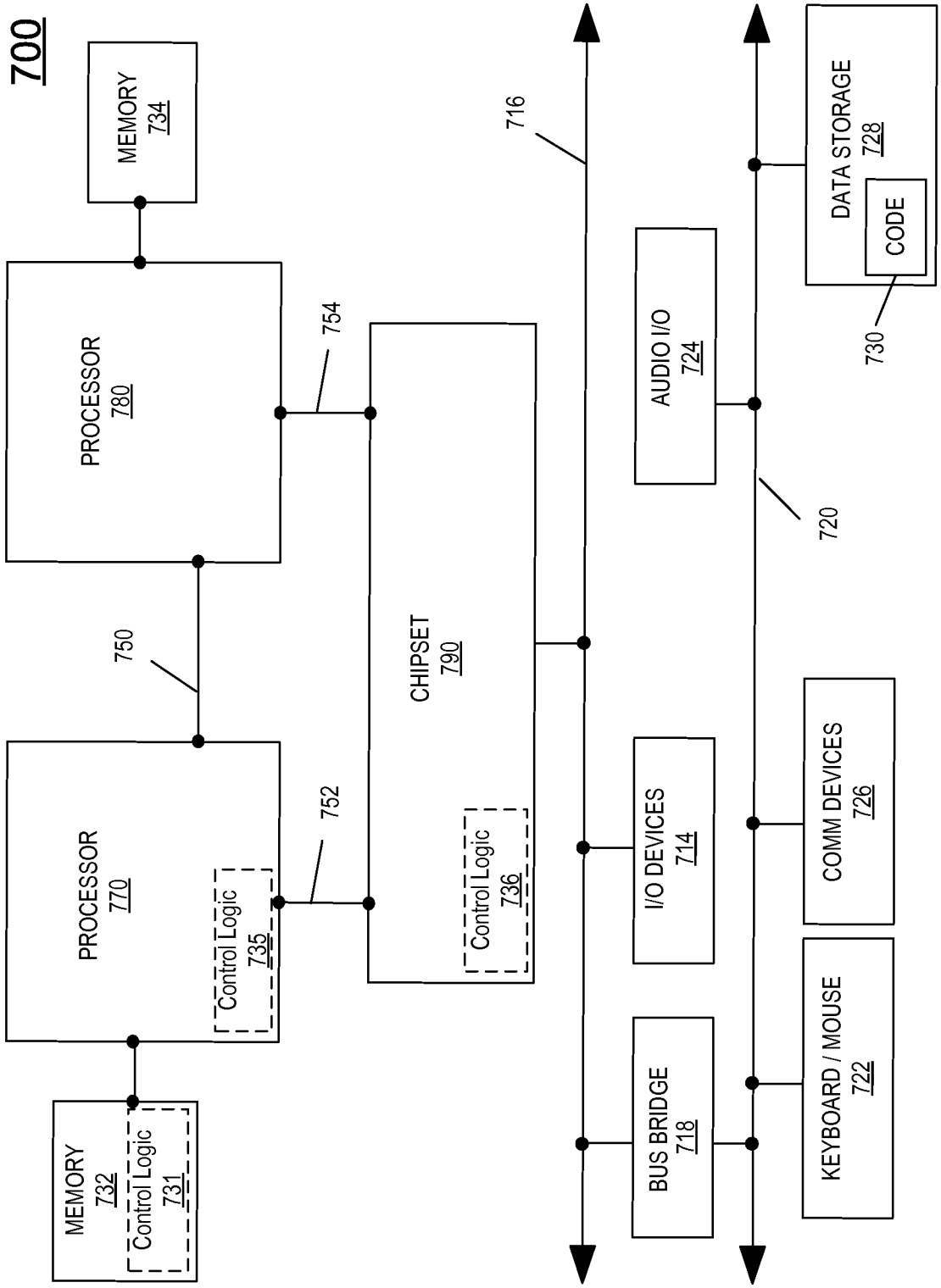

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COMM DEVICES
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BUS BRIDGE
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KEYBOARD / MOUSE
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FIG. 19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/032151

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/15(2006.01)i, H01L 27/115(2006.01)i, H01L 21/8247(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 11/15; H01L 43/12; G03F 7/26; H01L 29/82; H01L 21/8242; G03F 7/004; H01L 21/02; H01L 27/10; H01L 21/8239; H01L 21/00; H01L 27/115; H01L 21/8247

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: MRAM, magnetic tunnel junction (MTJ), interlayer dielectric (ILD), logic, material, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 2013-0015541 A1 (HIROYUKI KANAYA) 17 January 2013 See paragraphs 24, 37-44, 54; and figures 2, 4B.	1-25
A	US 2010-0297820 A1 (SE-YOUNG LEE et al.) 25 November 2010 See paragraphs 27-58; figures 1A-1B; and claim 1.	1-25
A	KR 10-2010-0094905 A (SANG YOON LEE) 27 August 2010 See paragraphs 14-27; figure 1; and claims 1-2.	1-25
A	US 2009-0302405 A1 (MICHAEL C. GAIDLS et al.) 10 December 2009 See paragraphs 26, 34-35; and figures 2, 9.	1-25
A	US 2009-0261433 A1 (SEUNG H. KANG et al.) 22 October 2009 See paragraphs 30-36, 47-48; and figure 3.	1-25
A	US 2009-0291388 A1 (SOLOMON ASSEFA et al.) 26 November 2009 See paragraphs 16-19; and figure 1.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 December 2013 (13.12.2013)	**13 December 2013 (13.12.2013)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
BYUN, Sung Cheal
Telephone No. +82-42-481-8262

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/032151

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