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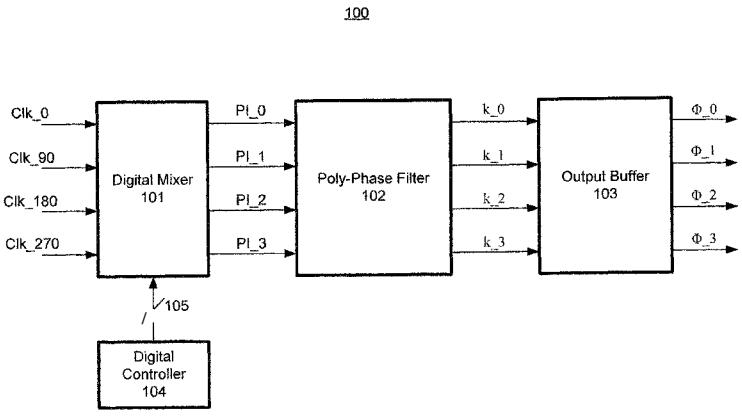

FIG. 1A

(57) Abstract: Described herein is an apparatus, method and system corresponding to relate to a low power digital phase interpolat - or (PI). The apparatus comprises: a digital mixer unit to generate phase signals from a series of input signals, the phase signals hav - ing phases which are digitally controlled; a poly-phase filter, coupled to the digital mixer unit, to generate a filtered signal by redu - cing phase error in the phase signals; and an output buffer, coupled to the poly-phase filter, to generate an output signal by buffering the filtered signal. The low power digital PI consumes less power compared to traditional current-mode Pis operating on the same power supply levels because the digital PI is independent of any bias circuit which are needed for current mode Pis.

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Low POWER DIGITAL PHASE INTERPOLATOR

FIELD OF THE INVENTION

[0001] Embodiments of the invention relate generally to the field of processors. More particularly, embodiments of the invention relate to a low power digital phase interpolator (PI).

BACKGROUND

[0002] Phase interpolators (Pis) are used in many application including high speed input-output (I/O) receivers to generate interpolated signals from input clock signals. These interpolated signals are used to sample input data received by the I/O receiver. As power consumption requirements for a processor are becoming stringent and processors are required to operate at lower power supply levels, for example 0.8V power supply level, performance of traditional analog-based Pis degrade.

[0003] The term "performance" herein generally refers to power supply rejection ratio (PSRR), power consumption, process-temperature-voltage (PVT) variations, area, scalability to lower power supply voltages, I/O transfer rate, etc.

[0004] A typical PI is a current mode PI. The current mode PI shows poor performance at low power supply levels because the current mode PI, being analog-based design, is highly sensitive to PVT variations, exhibits a lower power supply rejection ratio (PSRR) due to high analog bias dependency on the power supply and due to low swing operation requirements, consumes higher power, and requires complementary metal-oxide semiconductor (CMOS) to current mode logic (CML) and CML to CMOS converters to operate at low voltages resulting in larger area, and has lower I/O transfer rates at lower power supply levels. Such current mode-based Pis are unable to meet the stringent low power specifications of Mobile Industry Processor Interface (MIPI®) as described in the MIPI® Alliance Specification for M-PHY℠ Version 1.00.00 of February 8, 2011 and approved on April 28, 2011.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Embodiments of the invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention, which, however, should not be taken to limit the

invention to the specific embodiments, but are for explanation and understanding only.

[0006] **Fig. 1A** is a low voltage digital phase interpolator (PI), according to one embodiment of the invention.

[0007] **Fig. 1B** are waveforms input to a mixer unit of the PI, according to one embodiment of the invention.

[0008] **Fig. 2** is an input-output (I/O) receiver unit with the low voltage digital PI, according to one embodiment of the invention.

[0009] **Figs. 3A-B** are multiplexer-based implementations of the mixer unit, according to one embodiment of the invention.

[0010] **Fig. 3C** is a transistor-level implementation of the multiplexer, according to one embodiment of the invention.

[0011] **Fig. 3D** is a two stage poly-phase filter of the low voltage digital PI, according to one embodiment of the invention.

[0012] **Fig. 3E** is a differential output buffer of the low voltage digital PI, according to one embodiment of the invention.

[0013] **Figs. 4A-C** illustrates the generation of phase-interpolated signals in the multiplexers of the mixer unit of the low voltage digital PI, according to one embodiment of the invention.

[0014] **Fig. 5** is a method flowchart for generating digital phase-interpolated signals, according to one embodiment of the invention.

[0015] **Fig. 6** is a system-level diagram of a smart device comprising a processor including the low voltage PI, according to one embodiment of the invention.

SUMMARY

[0016] The following presents a simplified summary of the embodiments of the invention in order to provide a basic understanding of some aspects of the embodiments. This summary is not an extensive overview of the embodiments of the invention. It is intended to neither identify key or critical elements of the embodiments nor delineate the scope of the embodiments. Its sole purpose is to present some concepts of the embodiments of the invention in a simplified form as a prelude to the more detailed description that is presented later.

[0017] Embodiments of the invention relate to apparatus, method, and system corresponding to a low power digital phase interpolator.

[0018] In one embodiment, the apparatus comprises: a digital mixer unit to generate phase signals from a series of input signals, the phase signals having phases which are digitally controlled; a poly-phase filter, coupled to the digital mixer unit, to generate a filtered signal by reducing phase error in the phase signals; and an output buffer, coupled to the poly-phase filter, to generate an output signal by buffering the filtered signal.

[0019] In one embodiment, the method comprises: generating phase signals from a series of input signals, the phase signals having phases which are digitally controlled; generating a filtered signal by reducing phase error in the phase signals; and buffering the filtered signal.

[0020] In one embodiment, the system comprises a display unit (e.g., touch screen or touch pad); and a receiver, coupled to the display unit, having a digital phase interpolator, the digital phase interpolator including: a digital mixer unit to generate phase signals from a series of input signals, the phase signals having phases which are digitally controlled; a poly-phase filter, coupled to the digital mixer unit, to generate a filtered signal by reducing phase error in the phase signals; and an output buffer, coupled to the poly-phase filter, to generate an output signal by buffering the filtered signal, wherein the digital mixer, the poly-phase filter, and the output buffer are positioned in the receiver which is one of: a Mobile Industry Processor Interface (MIPI®) M-PHY$^{(SM)}$ receiver; a Peripheral Component Interconnect Express (PCIe) receiver; a Serial Advanced Technology Attachment (SATA) receiver; a Serial Attached SCSI (SAS) receiver; a Double Data Rate x (DDRx) receiver, were 'x' is an integer; a High-Definition Multimedia Interface (HDMI) receiver; or a Universal Serial Bus x (USBx) receiver, where 'x' is an integer.

[0021] The following description and the annexed drawings set forth in detail certain illustrative aspects of the embodiments of the invention. These aspects are indicative, however, of but a few of the various ways in which the principles of the embodiments of the invention may be employed. The embodiments of the invention are intended to embrace all equivalents in the form of alternatives, modifications, and variations that fall within the broad scope of the appended claims. Other advantages and novel features of the embodiments of the invention will become apparent from

the following detailed description of the embodiments of the invention when considered in conjunction with the drawings.

DETAILED DESCRIPTION

[0022] Embodiments of the invention relate to a low power digital phase interpolator (PI) which is highly scalable over process generations because of its digital architecture which is not sensitive to bias voltage levels as observed in analog circuits. In one embodiment, the low power digital PI applies a ratio-based voltage phase interpolation to a set of quadrature clock signals. In one embodiment, the low power digital PI provides a high power supply rejection ratio (PSRR) by using passive circuit elements (resistors and capacitors) as filtering elements. In one embodiment, the low power digital PI has smaller area than traditional current-mode based Pis because the transistors can be drawn with minimum process dimensions of width and length. In the embodiments discussed herein, the low power digital PI consumes less power compared to traditional current-mode Pis operating on the same power supply levels because the digital PI is independent of any bias circuit which is needed for operating current mode Pis.

[0023] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present invention. It will be apparent, however, to one skilled in the art, that embodiments of the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present invention.

[0024] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0025] In the following description and claims, the term "coupled" and its derivatives may be used. The term "coupled" herein refers to two or more elements

which are in direct contact (physically, electrically, magnetically, optically, etc.). The term "coupled" herein may also refer to two or more elements that are not in direct contact with each other, but still cooperate or interact with each other.

[0026] As used herein, unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0027] **Fig. 1A** is a low voltage digital PI 100, according to one embodiment of the invention. In one embodiment, the digital PI 100 comprises a mixer unit 101 which receives a set of quadrature clock signals—Clk_0, Clk_90, Clk_180, and Clk_270—and generates interpolated signals—PI_0, PI_1, PI_2, and PI_3—that have phase transitions between the phase transitions of the quadrature clock signals. Unlike traditional mixers, the mixer 101 herein is a digital mixer and does not require any analog bias generation circuit. Being a digital mixer 101, the transistors used to implement the mixer 101 (also called mixer unit 101) are drawn with minimum allowed dimensions of width and length, according to one embodiment of the invention. In one embodiment, the digital mixer 101 receives control or select signals 105 from a digital controller 104. The digital controller 104 is part of a feedback loop that determines the position of the phase transition of the interpolated signals that are used for sampling a signal, for example, a signal received by an I/O receiver.

[0028] **Fig. IB** are a set of quadrature clock signals 120—Clk_0, Clk_90, Clk_180, and Clk_270—input to the mixer unit 101 of the digital phase interpolator 100, according to one embodiment of the invention. The terms "0, 90, 180, and 270" for the quadrature clock signals refer to the position in degrees of the phases of the clock signals in degrees relative to Clk_0 signal. The period of each clock signal is 'T,' where 't' is the distance between the transition edge of Clk_0 to the transition edge of any of the remaining quadrature clock signals.

[0029] Referring back to **Fig. 1A,** in one embodiment the digital PI 100 comprises a poly-phase filter (PPF) 102 to provide phase error rejection across PVT corners and across wide frequency ranges. In one embodiment, the PPF 102 is a two stage PPF to provide second order compensation to the errors in phases of PI_0, PI_1, PI_2, and PI_3 signals. In the embodiments discussed herein, the PPF 102 comprises passive elements such as resistors (R) and capacitors (C).

[0030] The term "wide frequency ranges" herein refers to at least ranges high speed (HS) GEAR ranges from HS-GEAR 1 to HS-GEAR 3 as described in the MIPI® Alliance Specification for M-PHY℠ Version 1.00.00 of February 8, 2011 and approved on April 28, 2011.

[0031] **Fig. 3D** is a two stage PPF 330/102 of the low voltage digital PI 100, according to one embodiment of the invention. In one embodiment, the first stage 331 and the second stage 332 of the two stage PPF 330/102 are coupled in series with one another. Each stage of the PPF 330/102 comprises an RC filter with resistors connected between the input PI_N node and an output node, where N=0, 1, 2, and 3, and with cross coupled capacitors, as illustrated in **Fig, 3D.** In one embodiment, the first stage 331 of the PPF 330/102 comprises a network of series resistors R1 and cross-coupled capacitors CI. In one embodiment, the second stage 332 of the PPF 330/102 comprises a network of series resistors R2 and cross-coupled capacitors C2. The values of Rl, CI, R2, and C2 are selected such that the time constant (Rl x CI) of the first stage 331 is less than the time constant (R2 x C2) of the second stage 332, according to one embodiment of the invention. The output of the two-stage PPF 330/102 comprises the filtered signals k_0, k_l, k_2, and k_3 which are then buffered for sampling purposes.

[0032] In one embodiment, the values of the resistors and capacitors—Rl, CI, R2, and C2—are digitally programmable by enabling and/or disabling additional resistors and capacitors connected in parallel to the resistors and capacitors Rl, CI, R2, and C2. In other embodiments, fuses or metal options may be used to program the values of the resistors and capacitors Rl, CI, R2, and C2.

[0033] In one embodiment, the first and second stages (331 and 332) of the PPF 330/102 are configured such that the first stage 331 is configured to reduce frequency components of multi-phase clock signals PI_0, PI_1, PI_2, and PI_3 between approximately 10 and 20 percent below an image frequency while the second stage 332 is configured to reduce frequency components of multi-phase clock signals PI_0, PI_1, PI_2, and PI_3 between approximately 10 and 20 percent above the image frequency. In these embodiments, the frequency response of the first stage 331 may have a notch at approximate 10 to 20 percent below the image frequency, and the frequency response of the second stage 332 may have a notch approximate 10 to 20 percent above image frequency. The placement of two stages of the filters may be interchanged, i.e. the first stage 331 is positioned after the second stage 332 such that

the first stage 331 generates the filtered signals k_0, k_l, k_2, and k_3, according to one embodiment.

[0034] Referring back to **Fig. 1A,** the digital PI 100 further comprises an output buffer 103 (also called logic unit) to buffer the filtered signals k_0, k_l, k_2, and k_3 as final phase-interpolated signals Φ0, Φ1, Φ2, and Φ3, where Φ0 (first phase) has a transition edge in a middle of a phase of a data signal (or received signal which is being sampled), where Φ1 (second phase) has a transition edge at a crossing of a phase of the data signal and a successive phase of the data signal, where Φ2 (third phase) has a transition edge in a middle of the successive phase of the data signal, and where Φ3 (fourth phase) has a transition edge at the end of the phase of the successive phase of the data signal.

[0035] **Fig. 3E** is an implementation of the output buffer 103, according to one embodiment of the invention. In this embodiment, the output buffer 103 is pair of differential output buffers 341 and 342. In one embodiment, the output buffer 103 is a self-biased symmetrical load output buffer circuit. The following description is presented with reference to the buffer 341. The same description applies to the buffer 342. In one embodiment, the differential output buffers 341 and 342 receive as inputs the filtered signals k_0, k_l, k_2, and k_3 from the PPF 102 and generates differential interpolated signals Φ0, Φ1, Φ2, and Φ3.

[0036] In one embodiment, the output buffer 341 comprises two CMOS transistor pairs (Ml, M2, and M3, M4) that are used as the input devices, which extend the input signal to full swing. In one embodiment, additional CMOS transistor pairs (M5, M6, and M7, M8) are used for either current biases or loads. The gates of the bias/load branches may be coupled together as illustrated. In these embodiments, circuits 343 and 344 are symmetric at both left-to-right and top-to-bottom directions. Three feedback loops are provided in the circuit structure, including a left loop by transistors Ml, M2, M5, and M6, a right loop by transistors M3, M4, M7, and M8, and a common mode loop by transistors M5, M6, M7, and M8.

[0037] The embodiment of the output buffer 340 provides higher bias current around the cross point to achieve approximately zero DC bias, high speed switching, and a "soft landing" (e.g., substantially avoiding noise and glitches in the signal). These properties help make the output buffer 340 more robust for various applications (e.g., large power supply range, rail-to-rail signal swings, large transistor size range, etc.,) and scalable for different manufacture process technologies.

[0038] Referring back to **Fig. 1A,** in one embodiment the mixer unit 101 is implemented with programmable multiplexers that provide common mode (CM) rejection for the output signals PI_0, PI_1, PI_2, and PI_3. The mixer unit 101 is described with reference to **Figs. 3A-C** and **Figs. 4A-C.**

[0039] **Fig. 3A** is a single slice of multiplexer 300 based implementations of the mixer 101 while **Fig. 3B** are four slices 310 of the multiplexer-based implementations of the mixer 101, according to one embodiment of the invention. The following description is provided for **Fig. 3A** with reference to **Fig. 3C.** The same description is applicable to the embodiment of **Fig. 3B.**

[0040] The single slice of multiplex 300 comprises at least to 4-to-l multiplexers 301 and 302 which are configured to receive input quadrature clock signals Ck_{1-4} which directly correspond to Clk_0, Clk_90, Clk_180, and Clk_270 signals respectively. The 4-to-l multiplexers 301 and 302 are selectable by four bit input signals S_{1-4} that determine the phase location of the output signals Ckol, Cko2, Cko3, and Cko4 that directly correspond to signals PI_0, PI_1, PI_2, and PI_3 respectively. The output signals Ckol, Cko2, Cko3, and Cko4 are generated by weighted voltage summation of two differential clock signals from among the signals Clk_0, Clk_90, Clk_180, and Clk_270. In such an embodiment, the mixer unit 101 of the PI 100 is implemented in digital form using digital pass-gates. No analog bias voltages are used in these embodiments.

[0041] In one embodiment, a series resistance (R) is added between the output of the 4-to-l multiplexers 301 and 302 and the final output of the multiplexer 300. One reason for adding the series resistance is to filter noise in the signals generated by the 4-to-l multiplexers 301 and 302. In the embodiments discussed herein, the 4-to-l multiplexers 301 and 302 are differential multiplexers such that each 4-to-l multiplexer is operable to generate two output signals Ckol and Cko3 signals which directly correspond to PI_0 and PI_2 respectively.

[0042] **Fig. 3C** is a transistor-level implementation 320 of the 4-to-l multiplexer 301 or 302 of **Figs. 3A-B,** according to one embodiment of the invention. In one embodiment, the circuit of 320 comprises three components including a differential mixer unit 321 and CM rejection units 322 and 323. In one embodiment, the differential mixer unit 321 comprises four pairs of stacked P and N transistors with outputs shorted together with different pairs. Each pair has an identical

structure, according to one embodiment of the invention. So as not to obscure the embodiment of **Fig. 3C,** the structure of only one pair 324 is described. The same explanation is valid for the other three pairs.

[0043] In one embodiment, the pair 324 comprises a pair of stacked P and N transistors M_{1-8} connected together as illustrated in **Fig. 3C.** In one embodiment, each pair within the pair 324 receives a different clock signal from among the quadrature clock signals Ckl, Ck2, Ck3, and Ck4. In one embodiment, each of the four pairs is digitally controlled by select signals SI, S2, S3, and S4 of **Fig. 3A** respectively. The pair 324, for example, is controlled by the select signal SI and its corresponding inverted signal Sl_b. In one embodiment, the output of the first pair (left pair) within the pair (e.g., pair 324) is shorted with the output of the first pair (left pair) of the other remaining three pairs of 321 to generate the final output Ckol (which corresponding to PI_0). In such an embodiment, the output of the second pair (right pair) within the pair (e.g., pair 324) is shorted with the output of the first pair (right pair) of the other remaining three pairs of 321 to generate the final output Cko3 (which corresponds to PI_2).

[0044] In one embodiment, a pair of CM rejection units 322 and 323 is added to the output signals Ckol and Cko3. In one embodiment, the CM rejection unit 322 comprises P-transistors coupled between power supply and source terminals of the P-transistors of the four pairs discussed with reference to 321. In one embodiment, the CM rejection unit 322 provides a virtual power supply node 325 to the differential mixer 321. In one embodiment, the CM rejection unit 322 comprises a pair of P-transistors M9 and M10 with their gates controlled by Ckol and Cko3 signals respectively. In one embodiment, the CM rejection unit 323 comprises N-transistors coupled between ground and source terminals of the N-transistors of the four pairs discussed with reference to 321. In one embodiment, the CM rejection unit 323 provides a virtual ground node 326 to the differential mixer 321. In one embodiment, the CM rejection unit 323 comprises a pair of N-transistors Ml 1 and M12 with their gates controlled by Ckol and Cko3 signals respectively.

[0045] Referring back to **Fig. 3B,** in one embodiment, a bus of 64 bits is used for controlling the four slices 310 of multiplexers 311_{1-4}. In such an embodiment, the output of each of the four bit slices is merged together. For example, Ckol of the multiplexer unit 311_1 is merged with Cko1 of the other three multiplexer units 311_{2-4},

Cko3 of the multiplexer unit 311_1 is merged with Cko3 of the other three multiplexer units $311_{2\text{-}4}$, etc.

[0046] As mentioned above, the output signals Ckol, Cko2, Cko3, and Cko4 from the mixer unit 101 are generated by weighted voltage summation of two differential clock signals from among the signals Clk_0, Clk_90, Clk_180, and Clk_270. For illustrating the operation of the weighted voltage summation for Ckol, assume that each (e.g., 324) of the four pairs in 321 of **Fig. 3C** generate an output signal described as R/N_1, R/N_2, **R/N3,** and R/N_4, where $N_{1\text{-}4}$ are digitally programmed by the logic unit 104.

[0047] In the above example, when $N_1+N_2 = N$ and $N_3=N_4=0$, then the output clock phase of Ckol is given by $(N_2/N)(T/4)$ which generates a phase PI_1 between 0 and 90 degrees, where N=64 (corresponding to the 64 select bits for the four slices of multiplexers 310), and where 'T' is the period of the input clock signal Clk_0 as shown in **Fig.** IB. When any of the $N_{1\text{-}4}$ is equal to zero, it implies infinite output impedance from that branch of the four voltage summation branches—R/N_1, R/N_2, R/N_3, and **R/N4.**

[0048] When $N_2+N_3 = N$ and $N_4=N_1=0$, then the output clock phase of Ckol is given by $(T/4)+(N_3/N)(T/4)$ which generates a phase between 90 and 180 degrees. When $N_3+N_4 = N$ and $N_2=N_3=0$, then the output clock phase of Ckol is given by $((2T)/4)+(N_4/N)(T/4)$ which generates a phase between 180 and 270 degrees. In the embodiments discussed herein, in each multiplexer slice ($311_{1\text{-}4}$), the 4-to-l multiplexer is used to switch the connection of the load resistor (R) to realize the programming of $N_{1\text{-}4}$ as discussed herein.

[0049] **Figs. 4A-C** illustrates the generation of phase-interpolated signals by the mixer unit 101 of the low voltage digital PI 100, according to one embodiment of the invention. **Fig. 4A** illustrates the control settings 400 for C1-C4 that control the four slices of multiplexers 31li^ to generate an output Ckol -4 that are not phase-interpolated, i.e. all input clock signals Clkl-4 (interchangeably referred as $Ck_{1\text{-}4}$) are output as Ckol -4 respectively without any mixing of the signals to generate interpolated signals. The interpolation circle of **Fig. 4A** illustrates an interpolation of zero degrees, i.e. no interpolation, when $N_1=4$, $N_2=N_3=N_4=0$. Corresponding values

of C1-C4 are shown in **Fig. 4A.** A person skilled in the art would appreciate that "CI [3:0]" represents a four bit CI word.

[0050] **Fig. 4B** illustrates the control settings 410 for C1-C4 that control the four slices of multiplexers 31li^ to generate an output Ckol-4 which are phase-interpolated by 45 degrees. The interpolation circle of **Fig. 4B** illustrates an interpolation of 45 degrees when N_1=2, N_2=2, and N_3=N_4=0. Corresponding values of C1-C4 are shown in **Fig. 4B.**

[0051] **Fig. 4C** illustrates the control settings 420 for C1-C4 that control the four slices of multiplexers 31li^ to generate an output Ckol-4 which are phase-interpolated by approximately 140 degrees. The interpolation circle of **Fig. 4C** illustrates an interpolation of approximately 140 degrees when N^O, N_2=l, N_3=3, and N_4=0. Corresponding values of C1-C4 are shown in **Fig. 4C.**

[0052] **Fig. 2** is an I/O receiver unit 200 with the low voltage digital PI 100, according to one embodiment of the invention. In one embodiment, a differential input data data_in from an I/O transmitter (not shown) is sampled by a sampler 201. The sampler 201 is operable to sample the input data_in signal using the interpolated signals Φ0, Φ1, Φ2, and Φ3, where Φ0 (first phase) has a transition edge in a middle of a phase of the data_in signal, where Φ1 (second phase) has a transition edge at a crossing of a phase of the data_in signal and a successive phase of the data signal, where Φ2 (third phase) has a transition edge in a middle of the successive phase of the data_in signal, and where Φ3 (fourth phase) has a transition edge at the end of the phase of the successive phase of the data_in signal.

[0053] In one embodiment, the receiver unit 200 comprises an alignment unit 202 which receives the sampled data_in signals, sampled by Φ0, Φ1, Φ2, and Φ3 and generates output signals which are synchronized to the transmit clock signal domain. The alignment unit 202 is also called the synchronization unit. The output of the alignment unit 202 is then input to the digital control unit 104 of the PI 100, where the digital control unit 104 determines from the aligned signals (output of the alignment unit 202) whether the phases Φ0, Φ1, Φ2, and Φ3 are properly positioned in time, i.e., whether they are phase shifted to sample the data_in signal at the four points discussed above. The digital control unit 104 then selects the appropriate S1-S4 signals, i.e. Cl[3:0], C2[3:0], C3[3:0], and C4[3:0] control signals, by selecting the appropriate N_{1-4} values for the mixer unit 101.

[0054] In one embodiment, the receiver unit 200 comprises a serial-in-serial-out (SIPO) 203 unit that generates the data_out signal which is then processed by other logic units (not shown) of the processor comprising the I/O receiver 200. The I/O receiver can be used as a Mobile Industry Processor Interface (MIPI®) M-PHY (SM) receiver; a Peripheral Component Interconnect Express (PCIe) receiver; a Serial Advanced Technology Attachment (SATA) receiver; a Serial Attached SCSI (SAS) receiver; a Double Data Rate x (DDRx) receiver, were 'x' is an integer, for example, x=4 and above; a High-Definition Multimedia Interface (HDMI) receiver; or a Universal Serial Bus x (USBx) receiver, where 'x' is an integer, for example x=2 and above.

[0055] **Fig. 5** is a method flowchart 500 for generating digital phase-interpolated signals, according to one embodiment of the invention. Although the blocks in the flowchart 500 are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Additionally, one or more actions/blocks can be omitted in various embodiments for generating digital phase-interpolated signals using the low power digital PI 100. The flowchart of **Fig. 5** is illustrated with reference to the embodiments of **Figs. 1-4.**

[0056] At block 501, the mixer 101 generates phase signals (PI_0, PI_1, PI_2, and PI_3) from a series of input signals (quadrature clock signals Clk_0, Clk_90, Clk_180, Clk_270), wherein the phase signals have phases which are digitally controlled by the logic unit 104. The term "controlled" herein refers to selecting the control signals to the multiplexer 300 by the logic unit 104 to move the phase of the PI_0, PI_1, PI_2, and PI_3 signals relative to Clk_0 input signal. At block 502, the PPF 102 generates filtered signals k_0, k_l, k_2, and k_3 by reducing phase error in the phase signals PI_0, PI_1, PI_2, and PI_3. At block 503, the output buffer 103 buffers the filtered signals k_0, k_l, k_2, and k_3 to generate the final phase-interpolated signals $\Phi 0$, $\Phi 1$, $\Phi 2$, and $\Phi 3$.

[0057] **Fig. 6** is a system-level diagram of a smart device comprising a processor including the low voltage PI 100, according to one embodiment of the invention. **Fig. 6** also illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. Computing device 600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device.

It will be understood that certain of the components are shown generally, and not all components of such a device are shown in device 600.

[0058] Device 600 includes processor 610, which performs the primary processing operations of device 600. In one embodiment, the processor 610 includes the digital PI 100 in the receiver 200 as discussed with reference to **Figs. 1-4.**

[0059] Referring back to **Fig. 6,** the processor 610 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting device 600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0060] In one embodiment, device 600 includes audio subsystem 620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into device 600, or connected to device 600. In one embodiment, a user interacts with device 600 by providing audio commands that are received and processed by processor 610.

[0061] Display subsystem 630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device. Display subsystem 630 includes display interface 632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 632 includes logic separate from processor 610 to perform at least some processing related to the display. In one embodiment, display subsystem 630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0062] I/O controller 640 represents hardware devices and software components related to interaction with a user. I/O controller 640 can operate to manage hardware that is part of audio subsystem 620 and/or display subsystem 630. Additionally, I/O controller 640 illustrates a connection point for additional devices that connect to device 600 through which a user might interact with the system. For

example, devices that can be attached to device 600 might include microphone devices, speaker or stereo systems, video systems or other display device, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0063] As mentioned above, I/O controller 640 can interact with audio subsystem 620 and/or display subsystem 630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of device 600. Additionally, audio output can be provided instead of or in addition to display output. In another example, if display subsystem includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 640. There can also be additional buttons or switches on device 600 to provide I/O functions managed by I/O controller 640.

[0064] In one embodiment, the I/O controller 640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in device 600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0065] In one embodiment, device 600 includes power management 650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 660 includes memory devices for storing information in device 600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory 660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of system 600.

[0066] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 660) for storing the computer-executable instructions (e.g., instructions to implement the flowchart of **Fig. 5** and any other processes discussed above). The machine-readable medium (e.g., memory 660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, or other type of machine-readable media suitable for storing electronic or computer-executable instructions. For example,

embodiments of the invention may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0067] Connectivity 670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable device 600 to communicate with external devices. The device could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0068] Connectivity 670 can include multiple different types of connectivity. To generalize, device 600 is illustrated with cellular connectivity 672 and wireless connectivity 674. Cellular connectivity 672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity 674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[0069] Peripheral connections 680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that device 600 could both be a peripheral device ("to" 682) to other computing devices, as well as have peripheral devices ("from" 684) connected to it. Device 600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on device 600. Additionally, a docking connector can allow device 600 to connect to certain peripherals that allow device 600 to control content output, for example, to audiovisual or other systems.

[0070] In addition to a proprietary docking connector or other proprietary connection hardware, device 600 can make peripheral connections 680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware

interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other type.

[0071] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0072] While the invention has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description.

[0073] For example, the PPF 102 may be a single stage PPF comprising only the first stage 331 of PPF 300/102. In such and embodiment, the area of the PPF 102 is reduced. In another embodiment, the PPF 102 includes an LRC passive network comprising a network of resistive elements (R), inductive elements (L) and capacitive elements (C) selected to reduce image frequency that may be present in multi-phase clock signals PI_0, PI_1, PI_2, and PI_3. Furthermore, while the digital PI 100 is discussed with reference to an I/O receiver, it may be used in any circuit architecture where multiple phase output signals are required.

[0074] The embodiments of the invention are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[0075] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:

a digital mixer unit to generate phase signals from a series of input signals, the phase signals having phases which are digitally controlled;

a poly-phase filter, coupled to the digital mixer unit, to generate a filtered signal by reducing phase error in the phase signals; and

an output buffer, coupled to the poly-phase filter, to generate an output signal by buffering the filtered signal.

2. The apparatus of claim 1, wherein the poly-phase filter is a two stage poly-phase filter, the two stages of the poly-phase filter are operable to provide second order reduction in phase error in the phase signals.

3. The apparatus of claim 1, wherein the series of input signals are quadrature clock signals, and wherein the digital mixer is operable to generate the phase signals with phases between phases of the quadrature clock signals.

4. The apparatus of claim 3, wherein the digital mixer comprises a digital differential multiplexer which is operable to select one or more of the quadrature clock signals via digital input signals.

5. The apparatus of claim 4, wherein the digital differential multiplexer comprises P and N transistors controlled by the output of the digital differential multiplexer to provide common mode rejection to the phase signals.

6. The apparatus of claim 4 further comprises a logic unit to generate the digital input signals to cause the digital differential multiplexer to generate the phase signals with at least one or more of:

a first phase with a transition edge in a middle of a phase of a data signal;

a second phase with a transition edge at a crossing of a phase of the data signal and a successive phase of the data signal;

a third phase with a transition edge in a middle of the successive phase of the data signal; and

a fourth phase with a transition edge at the end of the phase of the successive phase of the data signal.

7. The apparatus of claim 1, wherein the poly-phase filter is a single stage poly-phase filter.

8. The apparatus of claim 1, wherein the output buffer is a differential output buffer which is operable to reject common mode from the filtered signal.

9. The apparatus of claim 1, wherein the digital mixer, the poly-phase filter, and the output buffer are positioned in a receiver which is one of:

a Mobile Industry Processor Interface (MIPI®) M-PHY (SM) receiver;

a Peripheral Component Interconnect Express (PCIe) receiver;

a Serial Advanced Technology Attachment (SATA) receiver;

a Serial Attached SCSI (SAS) receiver;

a Double Data Rate x (DDRx) receiver, were 'x' is an integer;

a High-Definition Multimedia Interface (HDMI) receiver; or

a Universal Serial Bus x (USBx) receiver, where 'x' is an integer.

10. The apparatus of claim 9, wherein the MIPI® M-PHY (SM) receiver is operable to receive high-speed (HS) GEAR rate signals.

11. A method comprising:

generating phase signals from a series of input signals, the phase signals having phases which are digitally controlled;

generating a filtered signal by reducing phase error in the phase signals; and

buffering the filtered signal.

12. The method of claim 11, wherein reducing the phase error in the phase signals comprises filtering the phase signals with a poly-phase filter.

13. The method of claim 12, wherein the poly-phase filter is a two stage poly-phase filter, the two stages of the poly-phase filter are operable to provide second order reduction in phase error in the phase signals.

14. The method of claim 11, wherein the series of input signals are quadrature clock signals, and wherein generating the phase signals comprises generating phase signals with phases between phases of the quadrature clock signals.

15. The method of claim 11, wherein generating the phase signals, generating the filtered signals, and buffering the filtered signals are performed by units positioned in a receiver which is one of:

a Mobile Industry Processor Interface (MIPI®) M-PHY (SM) receiver;

a Peripheral Component Interconnect Express (PCIe) receiver;

a Serial Advanced Technology Attachment (SATA) receiver;

a Serial Attached SCSI (SAS) receiver;

a Double Data Rate x (DDRx) receiver, were 'x' is an integer;

a High-Definition Multimedia Interface (HDMI) receiver; or

a Universal Serial Bus x (USBx) receiver, where 'x' is an integer.

16. The method of claim 15, wherein the MIPI® M-PHY (SM) receiver is operable to receive high-speed (HS) GEAR rate signals.

17. A system comprising:

a display unit; and

a receiver, coupled to the display unit, having a digital phase interpolator, the digital phase interpolator including:

a digital mixer unit to generate phase signals from a series of input signals, the phase signals having phases which are digitally controlled;

a poly-phase filter, coupled to the digital mixer unit, to generate a filtered signal by reducing phase error in the phase signals; and

an output buffer, coupled to the poly-phase filter, to generate an output signal by buffering the filtered signal.

18. The system of claim 17, wherein the display unit is a touch pad or a touch screen.

19. The system of claim 17, wherein the poly-phase filter is a two stage poly-phase filter, the two stages of the poly-phase filter are operable to provide second order reduction in phase error in the phase signals.

20. The system of claim 17, wherein the series of input signals are quadrature clock signals, and wherein the digital mixer is operable to generate the phase signals with phases between phases of the quadrature clock signals.

21. The system of claim 20, wherein the digital mixer comprises a digital differential multiplexer which is operable to select one or more of the quadrature clock signals via digital input signals.

22. The system of claim 21, wherein the digital differential multiplexer comprises P and N transistors controlled by the output of the digital differential multiplexer to provide common mode rejection to the phase signals.

23. The system of claim 21 further comprises a logic unit to generate the digital input signals to cause the digital differential multiplexer to generate the phase signals with at least one or more of:

a first phase with a transition edge in a middle of a phase of a data signal;

a second phase with a transition edge at a crossing of a phase of the data signal and a successive phase of the data signal;

a third phase with a transition edge in a middle of the successive phase of the data signal; and

a fourth phase with a transition edge at the end of the phase of the successive phase of the data signal.

24. The system of claim 17, wherein the poly-phase filter is a single stage poly-phase filter.

25. The system of claim 17, wherein the output buffer is a differential output buffer which is operable to reject common mode from the filtered signal.

26. The system of claim 17, wherein the digital mixer, the poly-phase filter, and the output buffer are positioned in the receiver which is one of:

a Mobile Industry Processor Interface (MIPI®) M-PHY$^{(SM)}$ receiver;

a Peripheral Component Interconnect Express (PCIe) receiver;

a Serial Advanced Technology Attachment (SATA) receiver;

a Serial Attached SCSI (SAS) receiver;

a Double Data Rate x (DDRx) receiver, were 'x' is an integer;

a High-Definition Multimedia Interface (HDMI) receiver; or

a Universal Serial Bus x (USBx) receiver, where 'x' is an integer.

27. The system of claim 26, wherein the MIPI® M-PHY$^{(SM)}$ receiver is operable to receive high-speed (HS) GEAR rate signals.

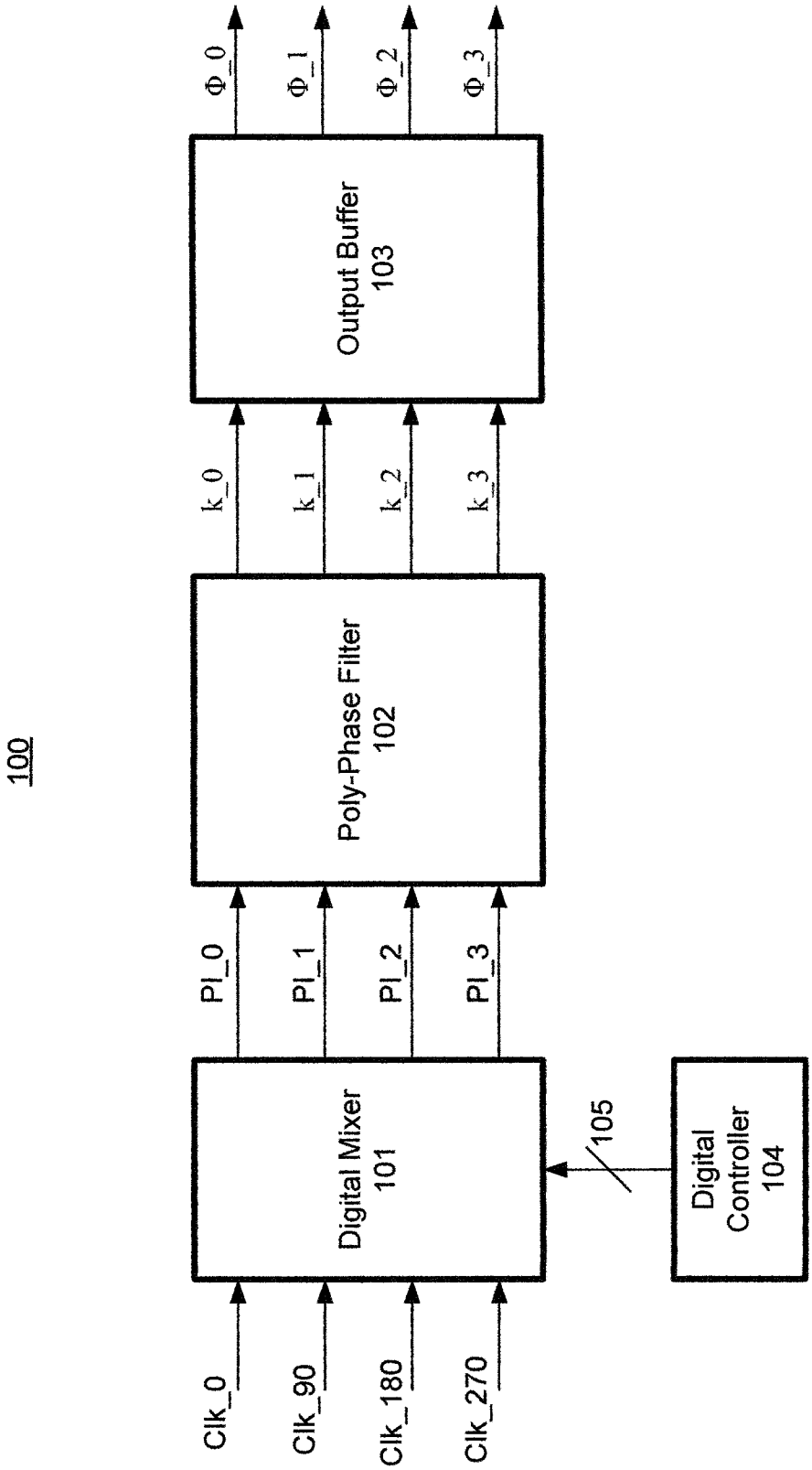

100
Clk_0
Clk_90
Clk_180
Clk_270
Digital Mixer
101
PI_0
PI_1
PI_2
PI_3
105
Digital
Controller
104
Poly-Phase Filter
102
k_0
k_1
k_2
k_3
Output Buffer
103
Φ_0
Φ_1
Φ_2
Φ_3

FIG. 1A

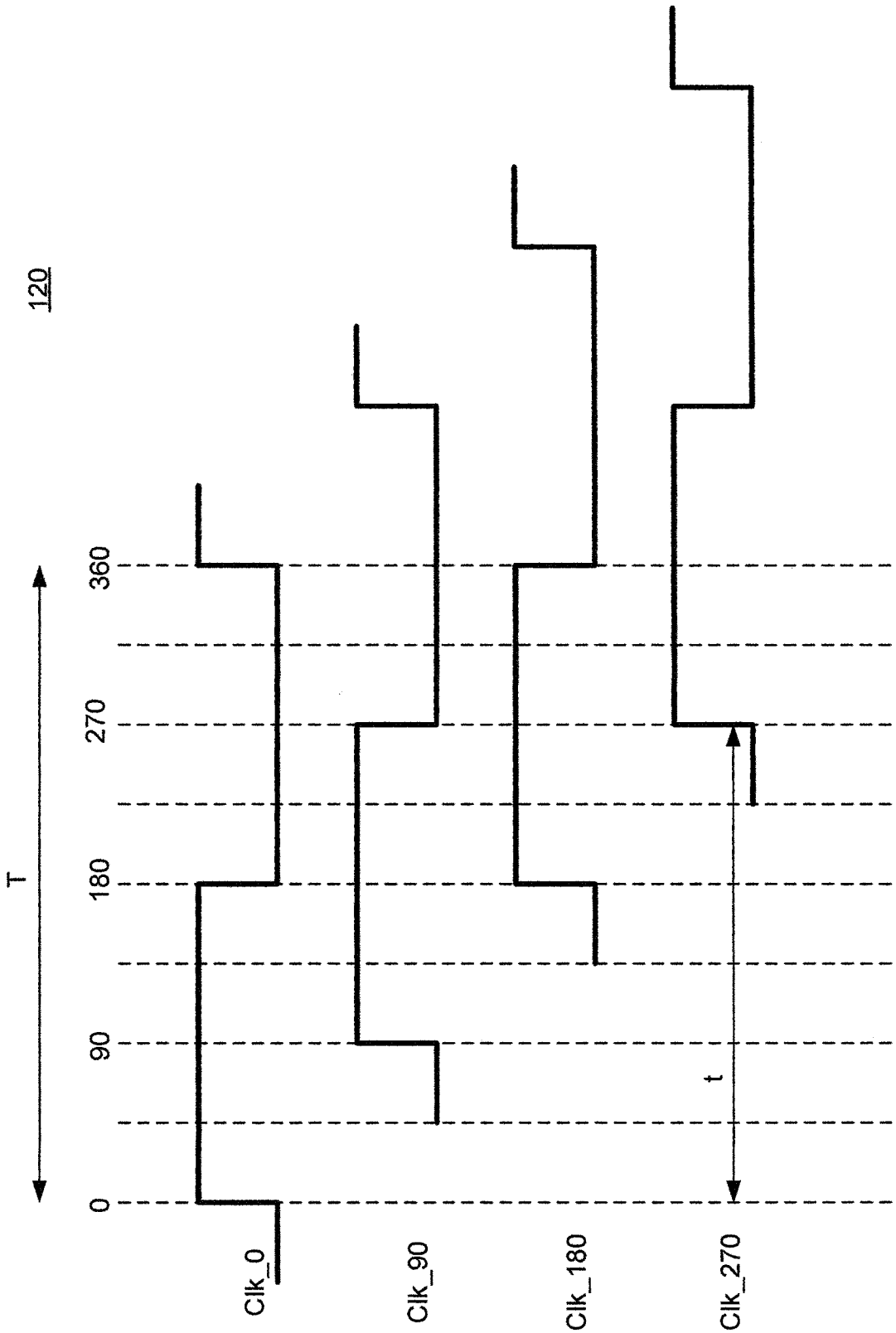


FIG. 1B

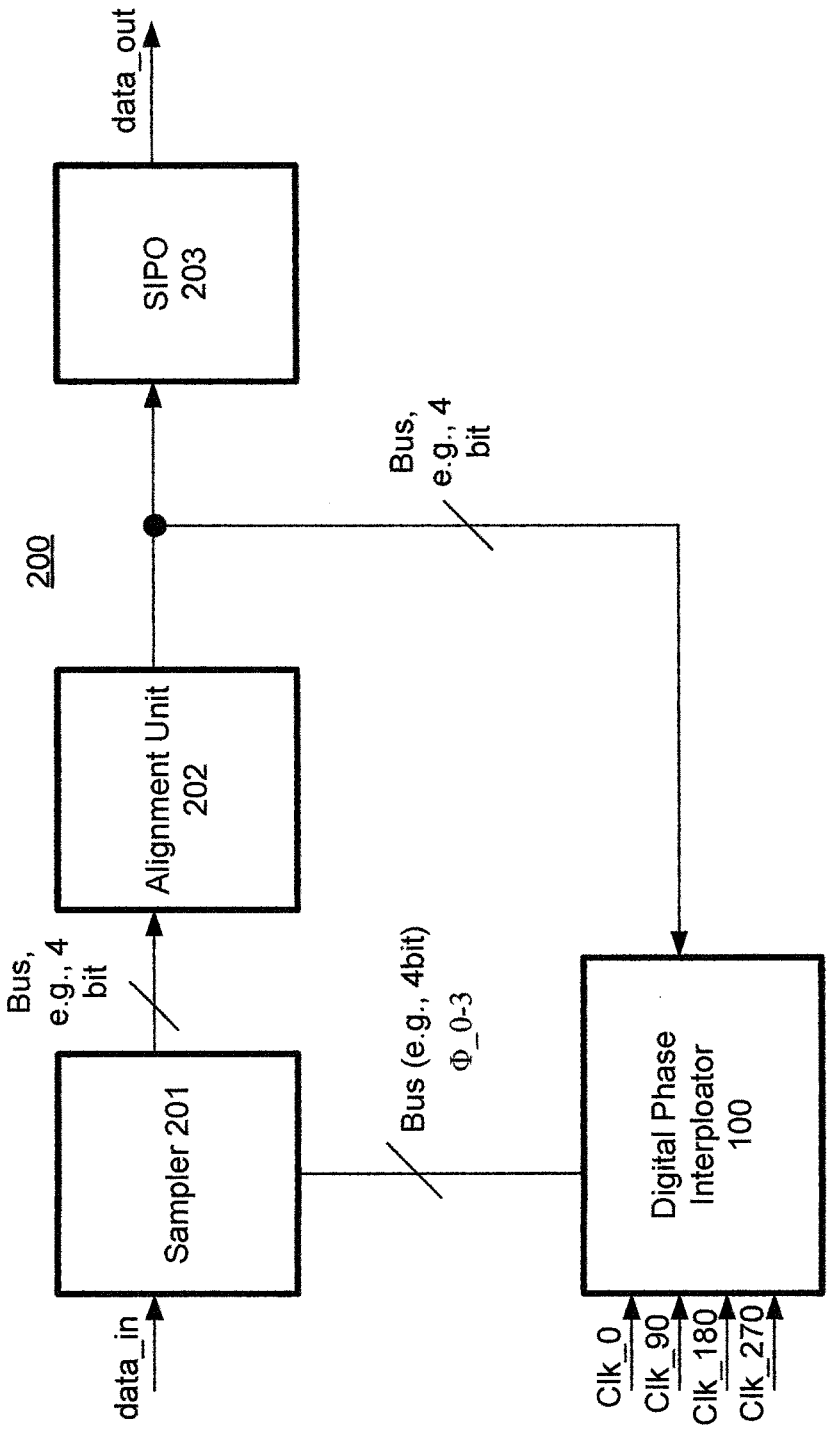

data_out
SIPO
203
Bus,
e.g., 4
bit
200
Alignment Unit
202
Bus,
e.g., 4
bit
Bus (e.g., 4bit)
Φ_0-3
Sampler 201
Digital Phase
Interploator
100
data_in
Clk_0
Clk_90
Clk_180
Clk_270

FIG. 2

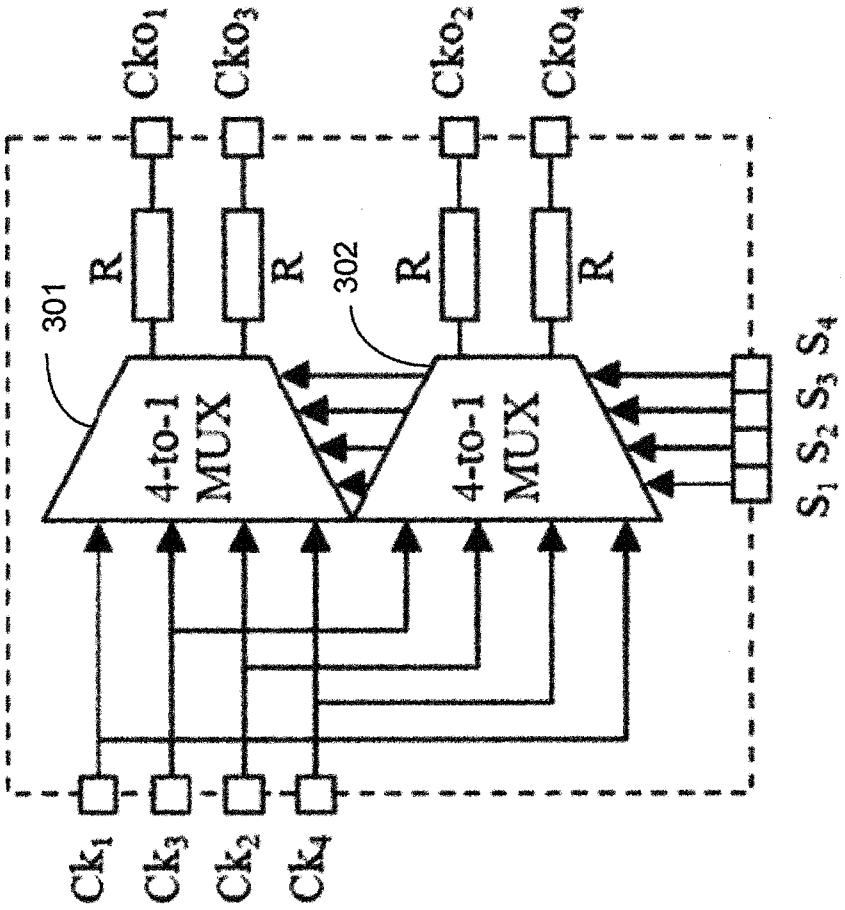

300
Cko1
Cko3
Cko2
Cko4
R
R
R
R
301
302
4-to-1 MUX
4-to-1 MUX
S1 S2 S3 S4
Ck1
Ck3
Ck2
Ck4

FIG. 3A

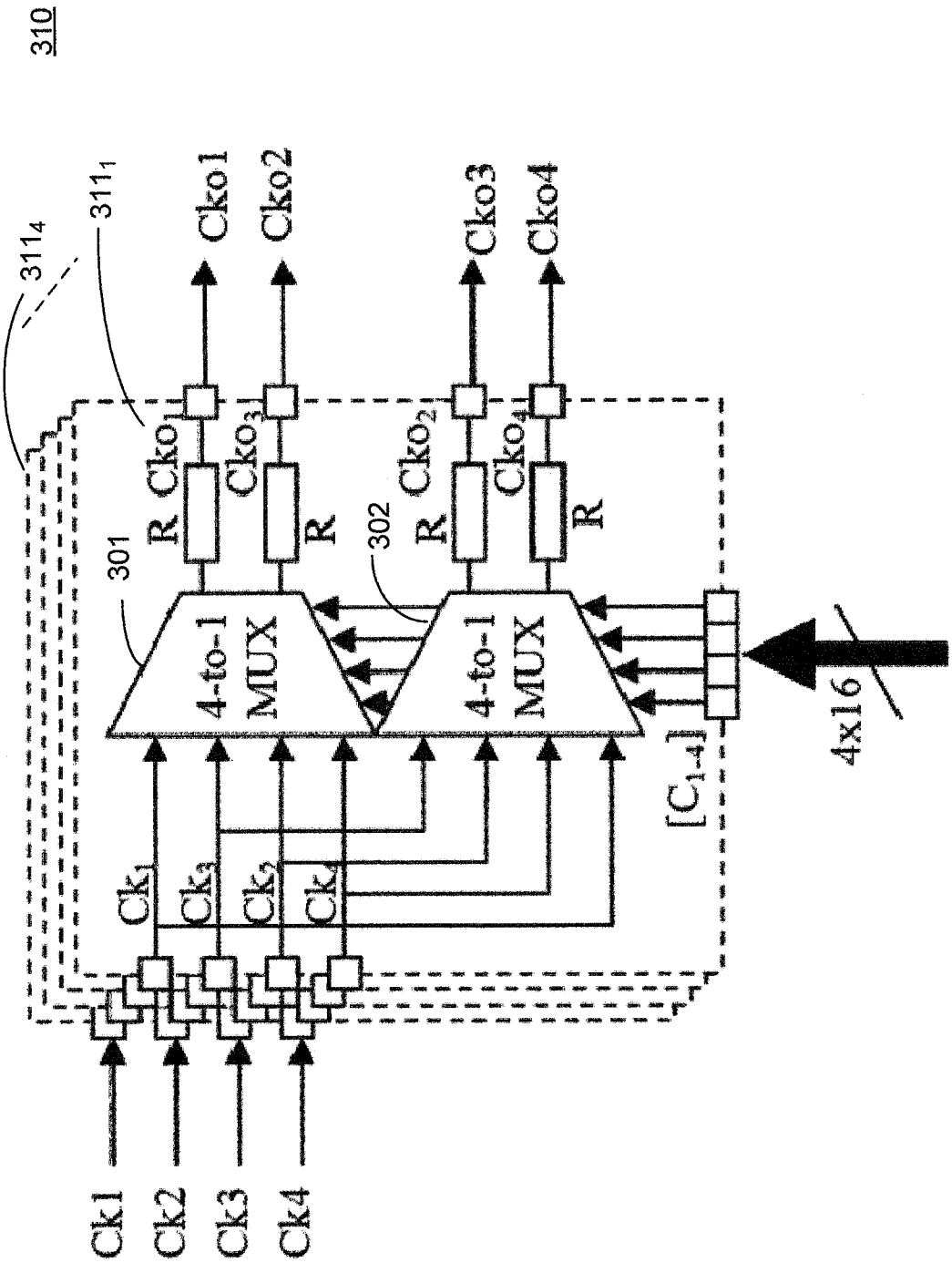

310
311$_4$
311$_1$
Cko1
Cko2
Cko3
Cko4
R
R
R
R
301
302
4-to-1 MUX
4-to-1 MUX
Ck$_1$
Ck$_3$
Ck$_2$
Ck$_4$
[C$_{1-4}$]
4x16
Ck1
Ck2
Ck3
Ck4

FIG. 3B

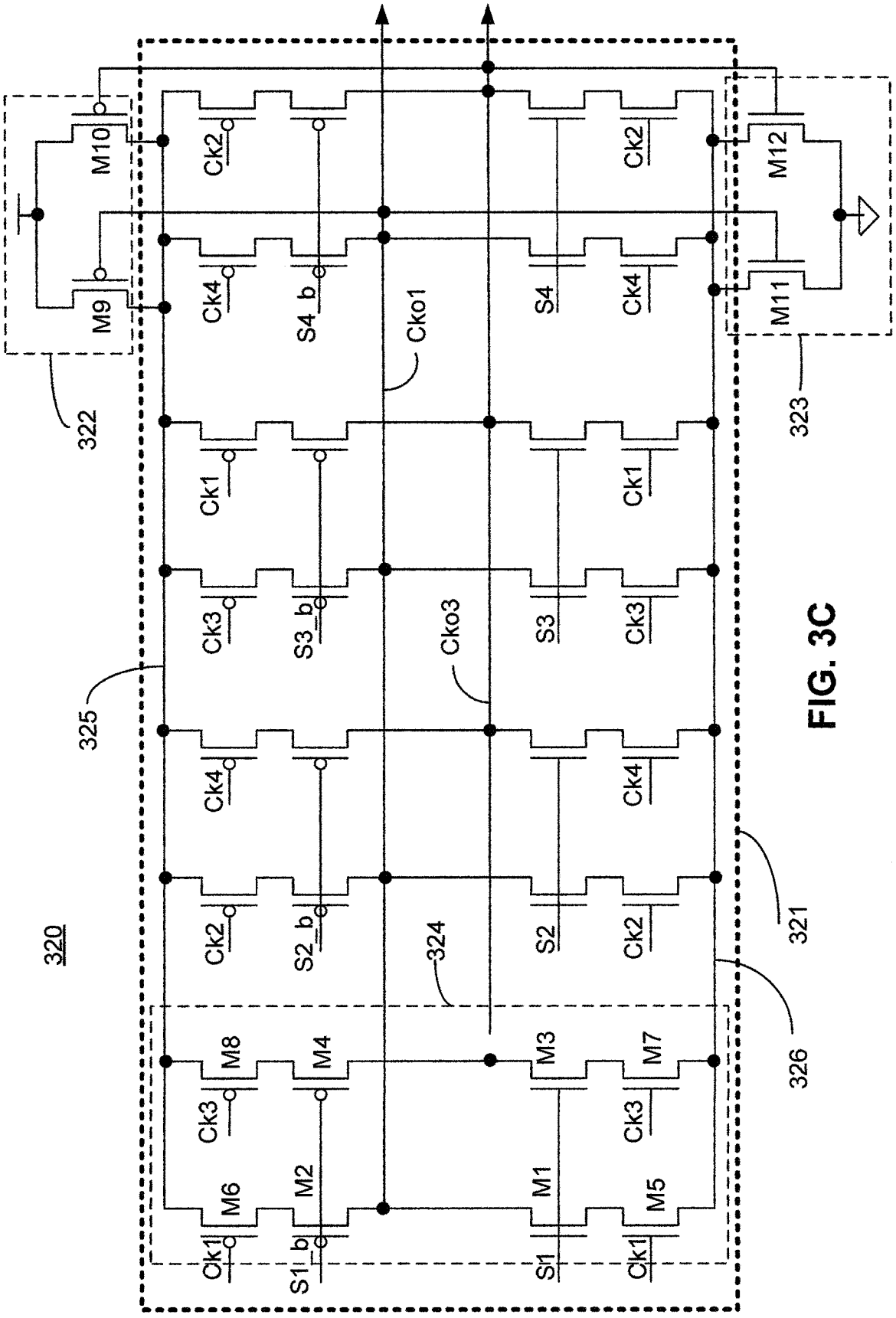

320
322
323
325
326
321
324
M10
M9
M12
M11
M8
M4
M3
M7
M6
M2
M1
M5
Ck2
Ck4
Ck1
Ck3
S4_b
S3_b
S2_b
S1_b
Cko1
Cko3
S4
S3
S2
S1

FIG. 3C

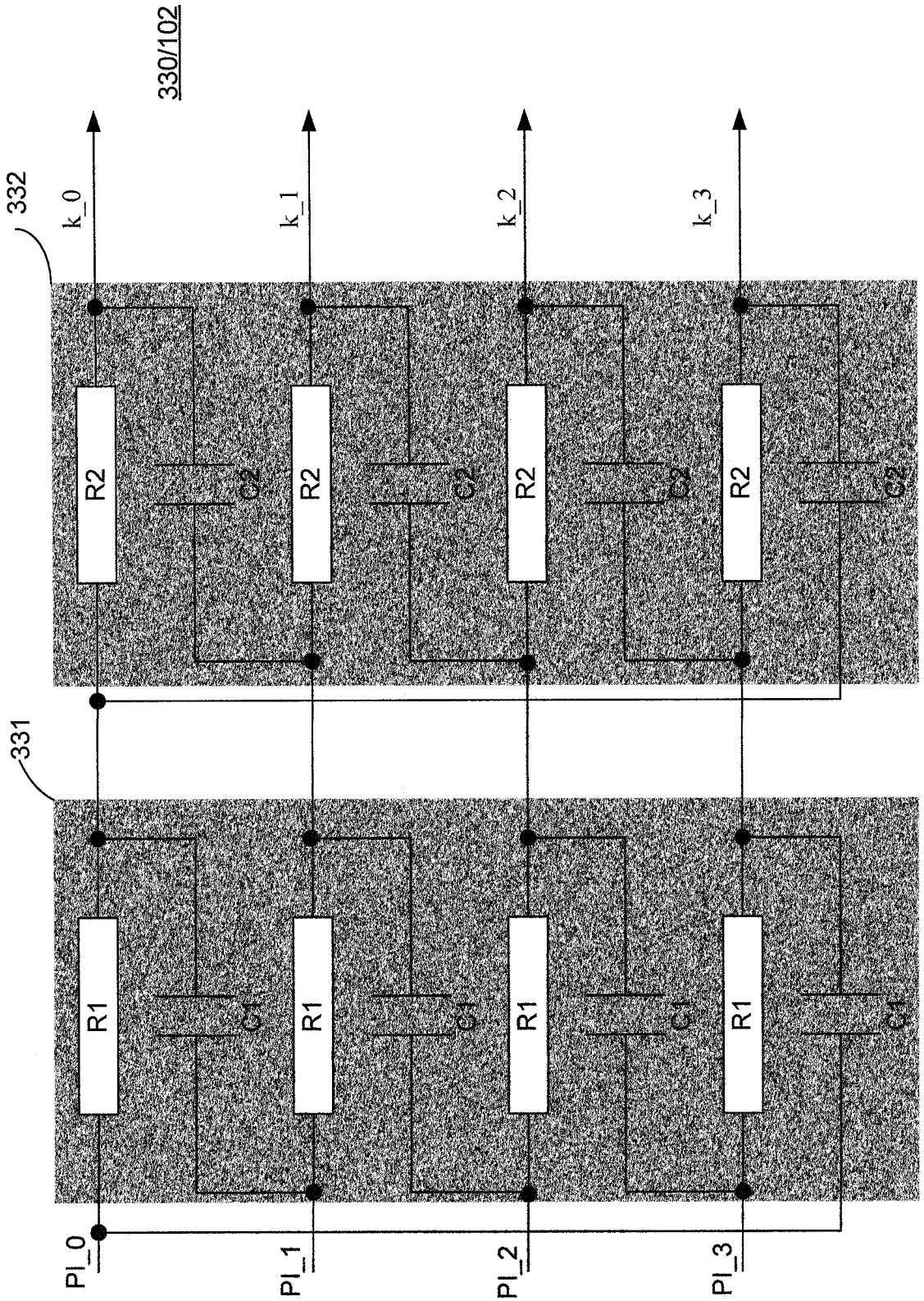


FIG. 3D

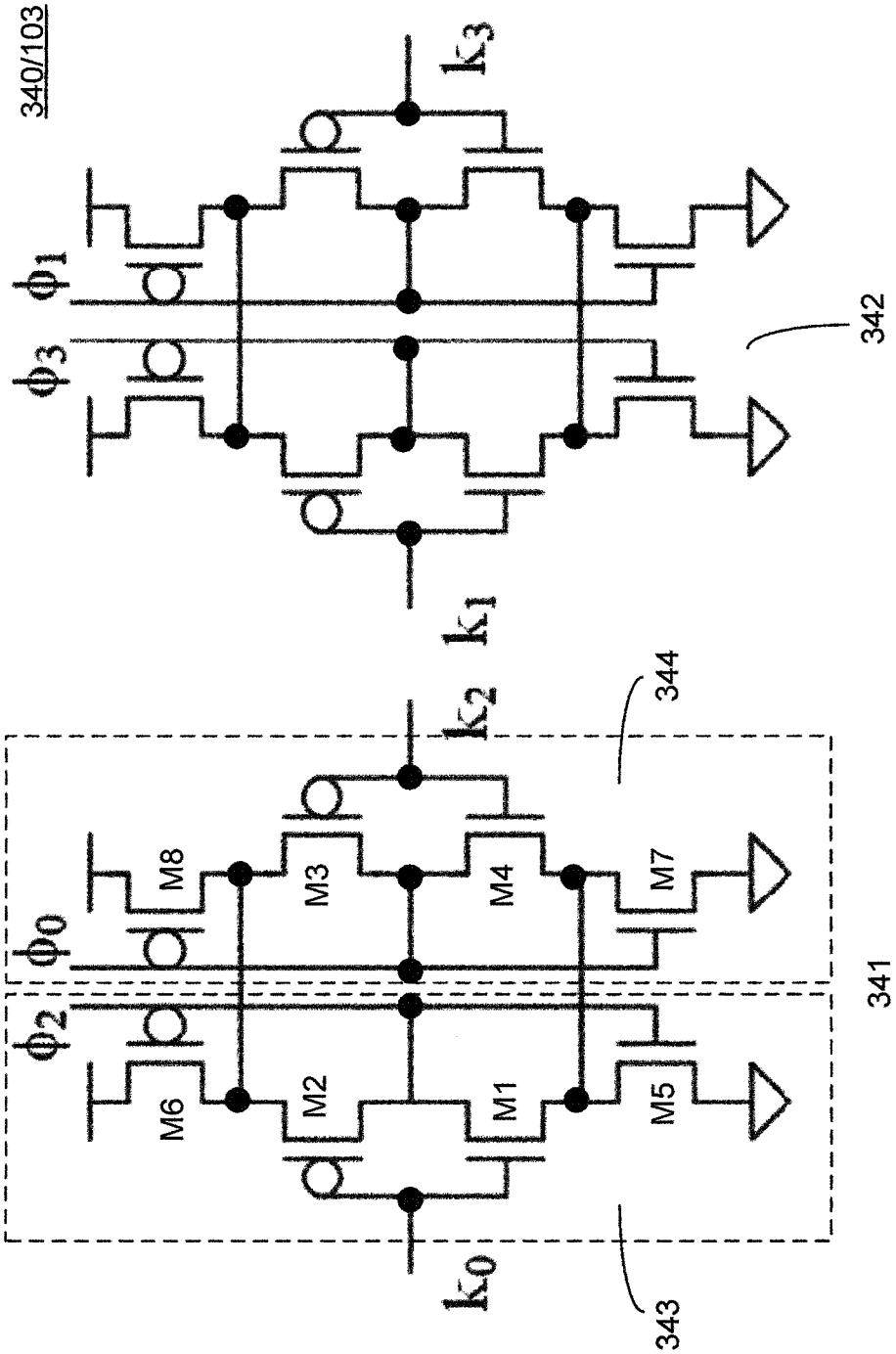
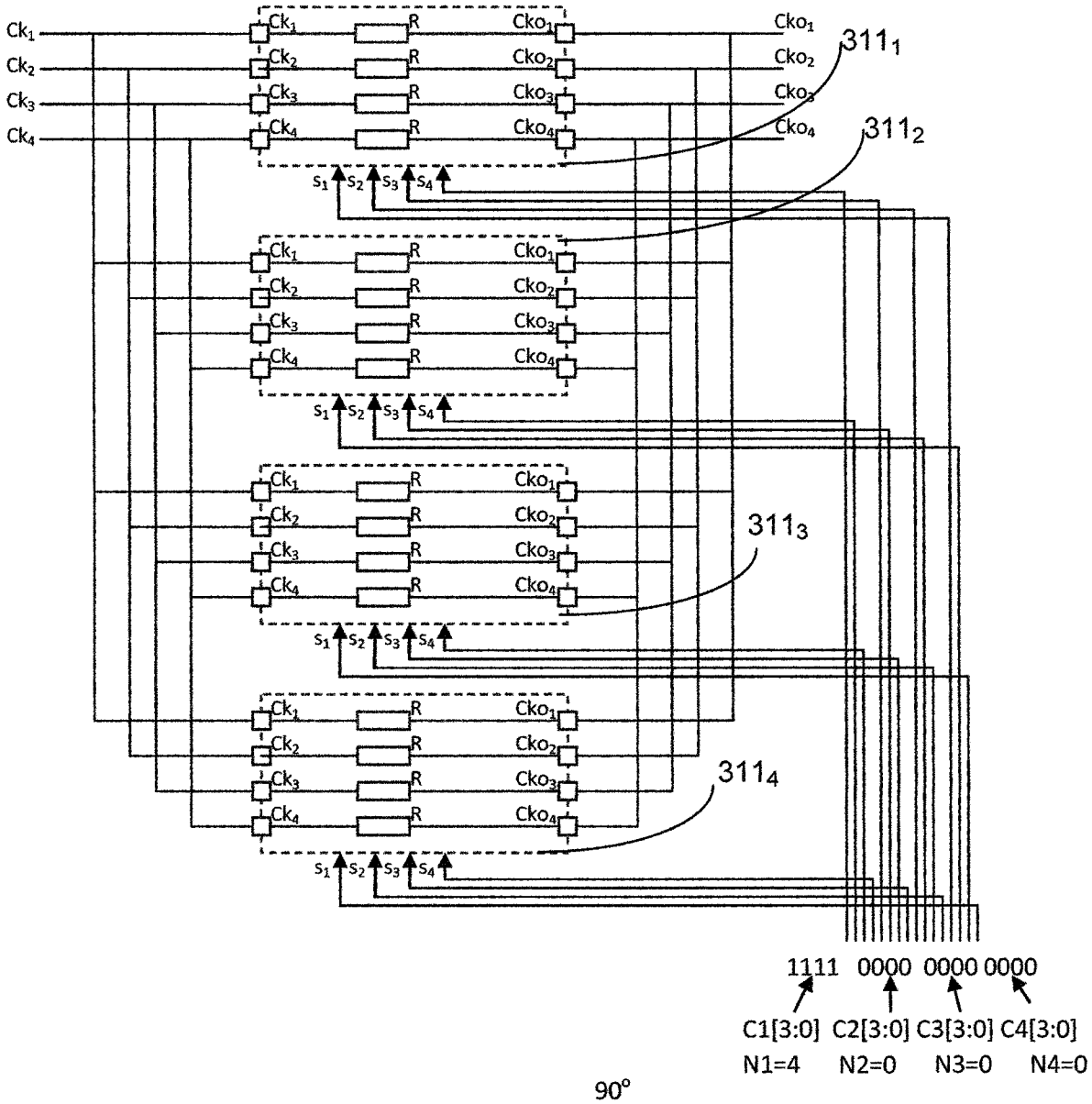

340/103
k_3
ϕ_1
ϕ_3
342
k_1
k_2
344
M8
M3
M4
M7
ϕ_0
ϕ_2
M6
M2
M1
M5
341
k_0
343

FIG. 3E


Ck1
Ck2
Ck3
Ck4
R
Cko1
Cko2
Cko3
Cko4
S1 S2 S3 S4
311 1
311 2
311 3
311 4
1111 0000 0000 0000
C1[3:0] C2[3:0] C3[3:0] C4[3:0]
N1=4 N2=0 N3=0 N4=0

400

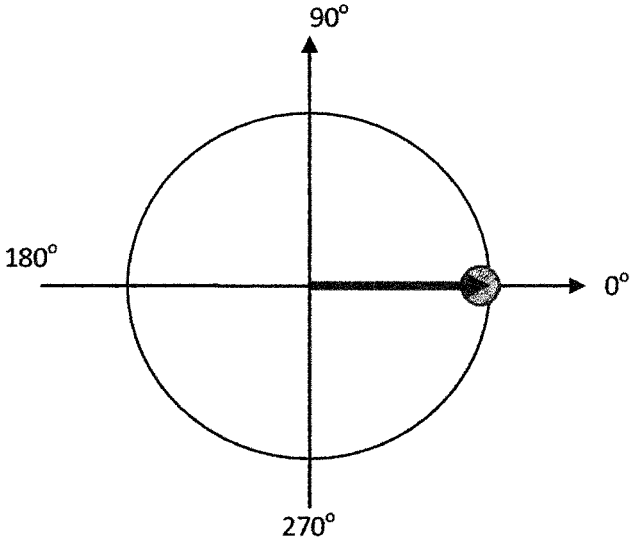
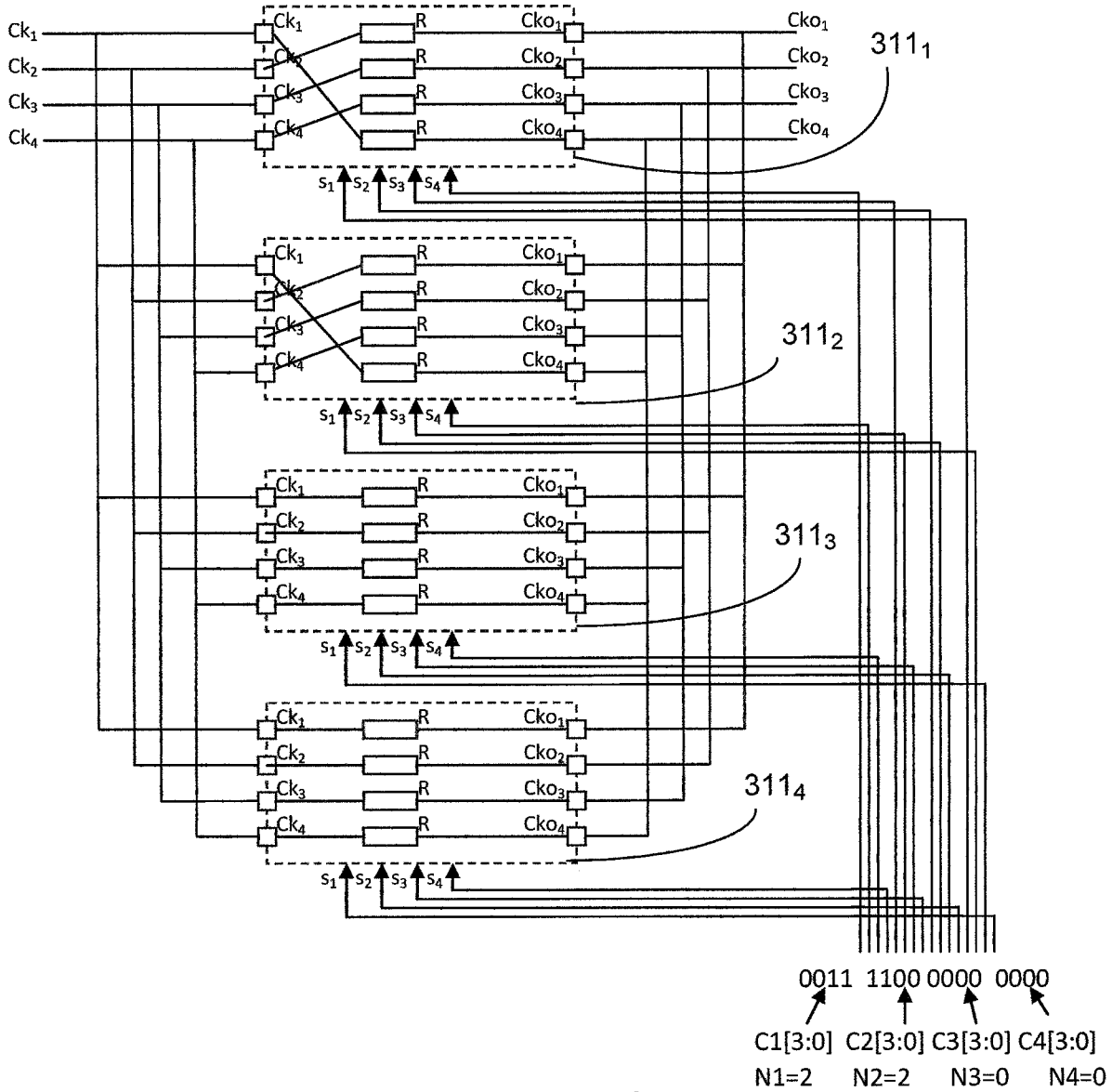

90°
180°
0°
270°

FIG. 4A


Ck1
Ck2
Ck3
Ck4
R
Cko1
Cko2
Cko3
Cko4
s1 s2 s3 s4
311 1
311 2
311 3
311 4
0011 1100 0000 0000
C1[3:0] C2[3:0] C3[3:0] C4[3:0]
N1=2 N2=2 N3=0 N4=0

410

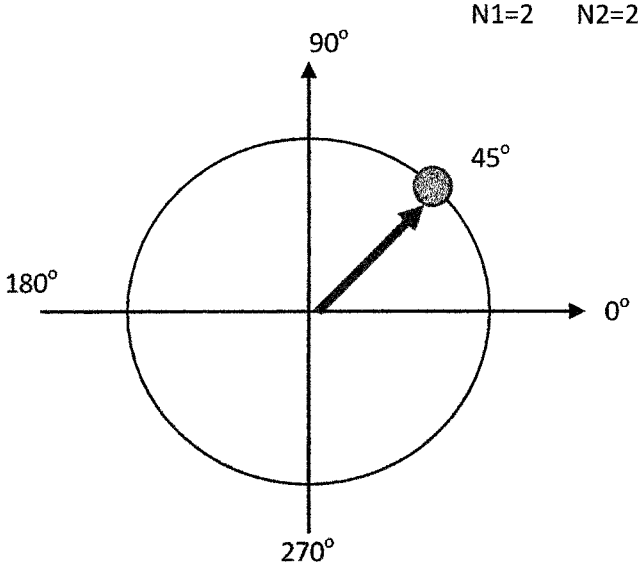

90°
45°
180°
0°
270°

FIG. 4B

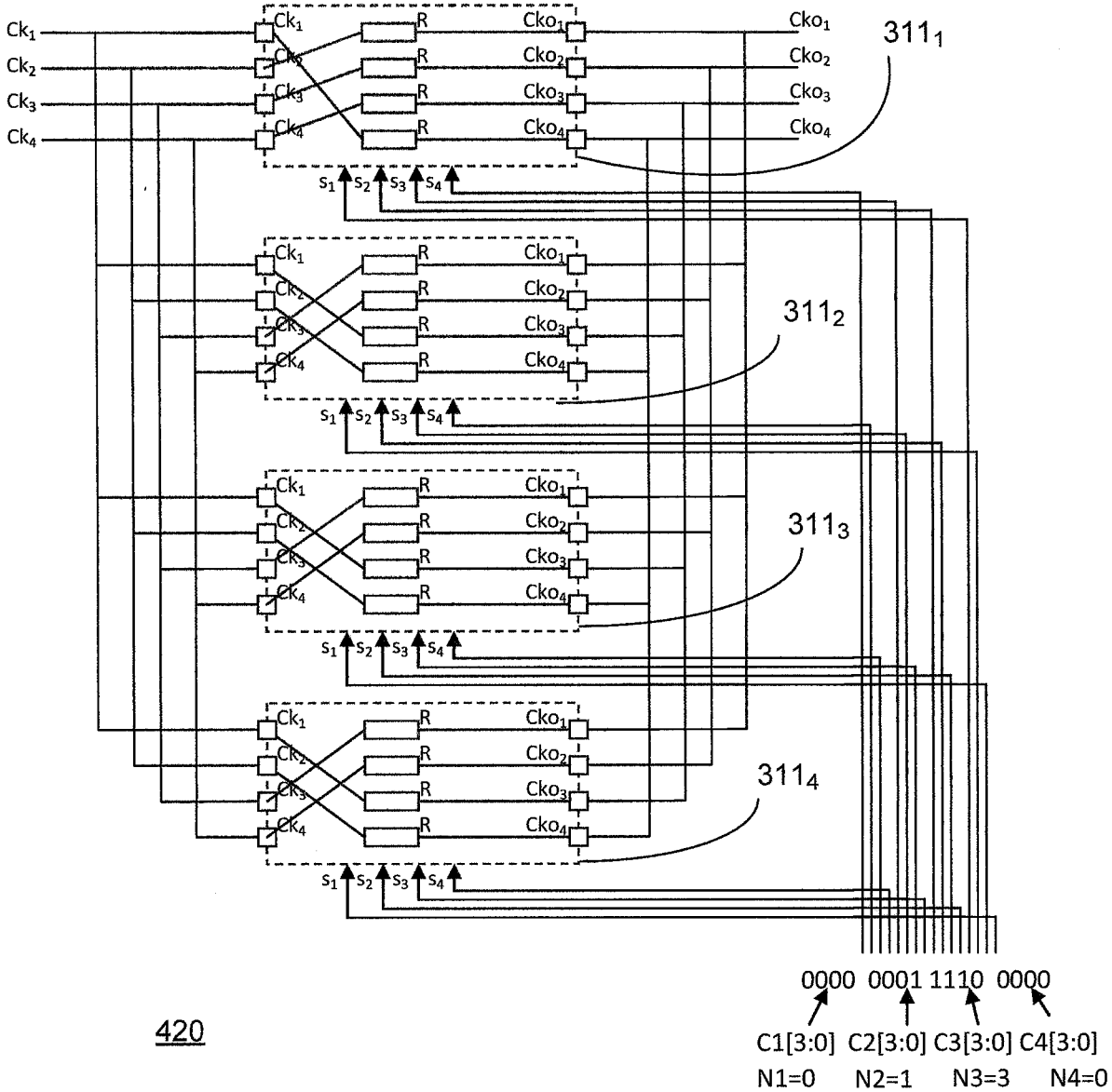
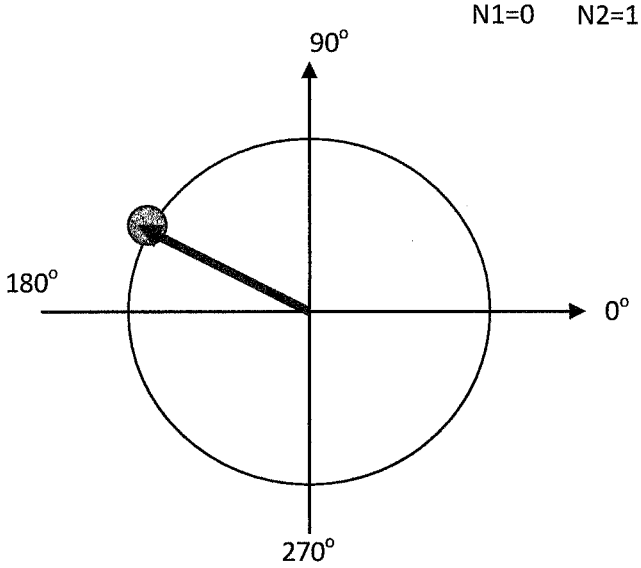

Ck1
Ck2
Ck3
Ck4
R
Cko1
Cko2
Cko3
Cko4
s1 s2 s3 s4
311 1
311 2
311 3
311 4
0000 0001 1110 0000
C1[3:0] C2[3:0] C3[3:0] C4[3:0]
N1=0 N2=1 N3=3 N4=0
420

FIG. 4C


90°
180°
0°
270°

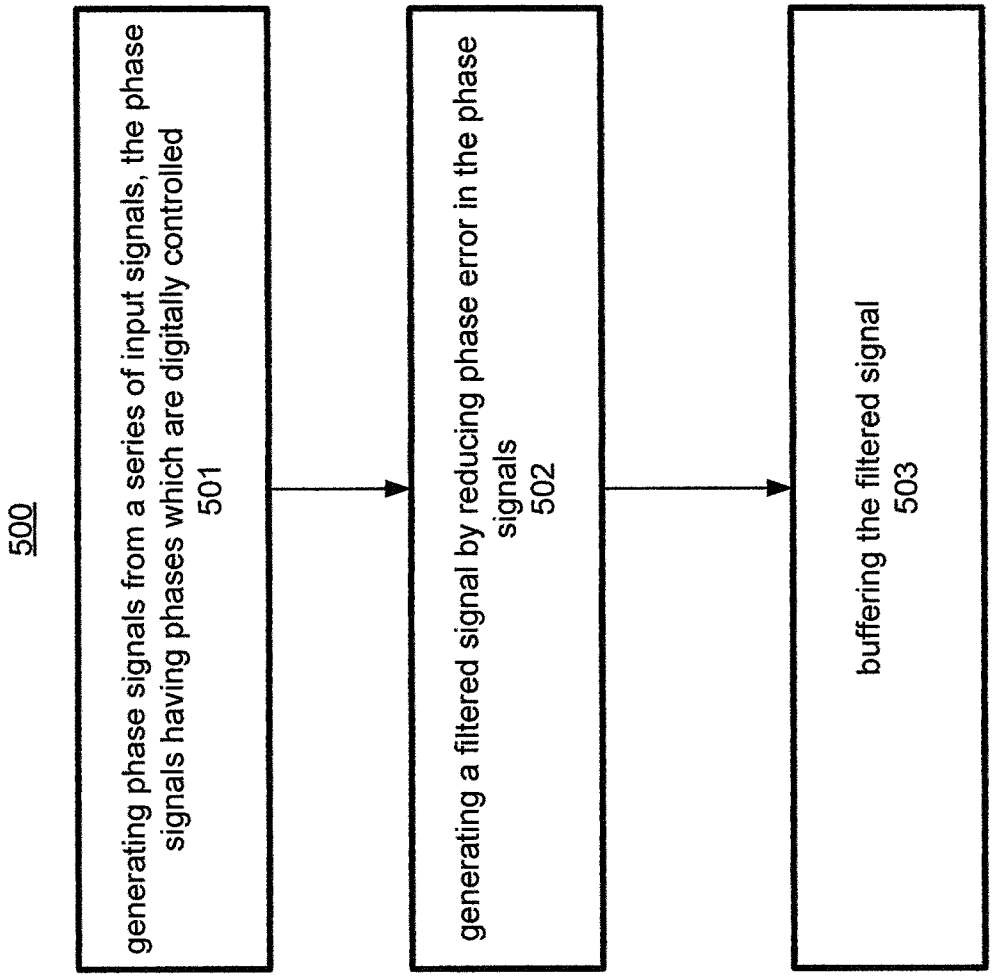

500
generating phase signals from a series of input signals, the phase signals having phases which are digitally controlled
501
generating a filtered signal by reducing phase error in the phase signals
502
buffering the filtered signal
503

FIG. 5

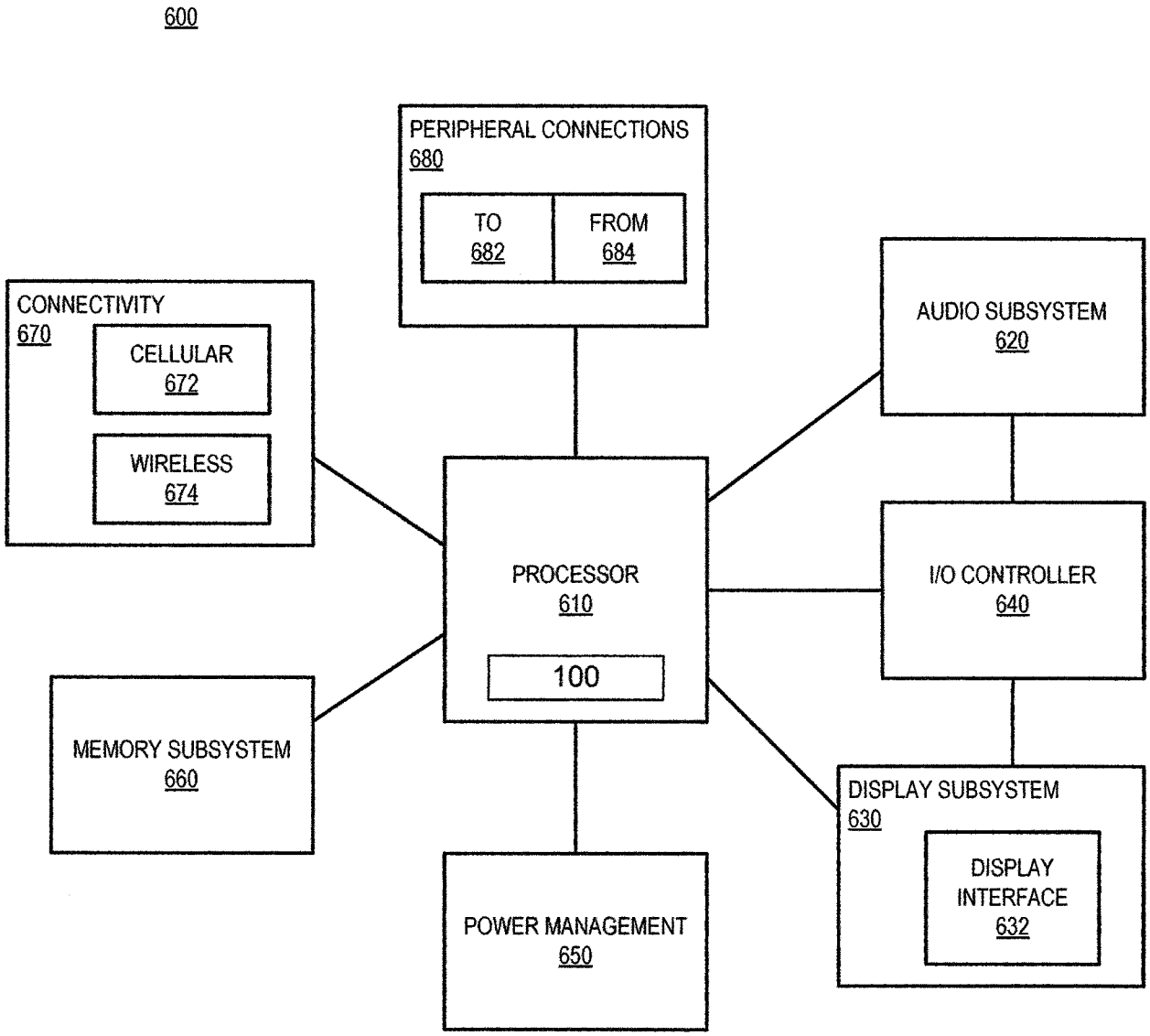

600
PERIPHERAL CONNECTIONS
680
TO
682
FROM
684
CONNECTIVITY
670
CELLULAR
672
WIRELESS
674
AUDIO SUBSYSTEM
620
PROCESSOR
610
100
I/O CONTROLLER
640
MEMORY SUBSYSTEM
660
DISPLAY SUBSYSTEM
630
DISPLAY
INTERFACE
632
POWER MANAGEMENT
650

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/066472

A. CLASSIFICATION OF SUBJECT MATTER

G06F l/00(2006.01)i, H03H 11/16(2006.01)1, H03L 7/00(2006.01)1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/00; H03K 3/00; H04L 27/00; H04L 27/06; A61B 8/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: "MIXER" , "FILTER" , "BUFFER" , "PHASE" , "DIGITAL"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0158358 Al (TSENG CHUN-CHIEH et al.) 30 June 2011 See abstract, paragraphs [0006]-[0045] and figure 2	1,11-12
Y	========== See abstract, paragraphs [0006]-[0045] and figure 2	17
Y	US 2004-0158149 Al (GLEN MCLAUGHLIN et al.) 12 August 2004 See abstract, paragraphs [0024]-[0038] and figures 1 and 4A	17
A	US 2009-0201064 Al (KIM KYU-HY0UN et al.) 13 August 2009 See abstract, paragraphs [0040]-[0065] and figure 1	1-27
A	US 7733984 B2 (BAUMGARTNER STEVEN JOHN et al.) 08 June 2010 See abstract, column 4 line 13 - column 5 line 29 and figure 1	1-27

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 AUGUST 2012 (28.08.2012)	**30 AUGUST 2012 (30.08.2012)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US201 1/066472

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