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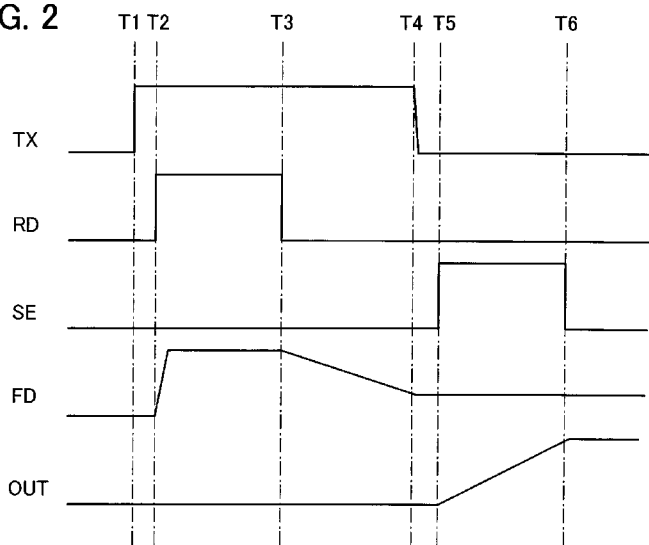
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FIG. 2



(57) Abstract: This invention has for purpose to provide a photosensor that is small in size and can obtain high-contrast image data and to provide a semiconductor device including the photosensor. In the photosensor including a light-receiving element, a transistor serving as a switching element, and a charge retention node electrically connected to the light-receiving element through the transistor, the reduction in charge held in the charge retention node is suppressed by extending the fall time of the input waveform of a driving pulse supplied to the transistor to turn off the transistor.

DESCRIPTION

**METHOD FOR DRIVING PHOTSENSOR, METHOD FOR DRIVING
SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, AND
ELECTRONIC DEVICE**

TECHNICAL FIELD

[0001]

The present invention relates to a method for driving a photosensor. Further,
the present invention relates to a semiconductor device and a method for driving the
semiconductor device.

BACKGROUND ART

[0002]

Digital cameras and mobile phones that include solid-state imaging elements
and thus have an imaging function have high added value. The reduction in size and
power consumption as well as the increase in definition has been required for solid-state
imaging elements in recent years. Photosensors are used as solid-state imaging
elements.

[0003]

A photosensor using an amplification function of a MOS transistor, called a
complementary metal oxide semiconductor (CMOS) sensor, can be fabricated through a
general CMOS process. Thus, fabrication costs of a solid-state imaging device
including a CMOS sensor in each pixel can be low, and a semiconductor display device
including a CMOS sensor and a display element formed over one substrate can be
provided. Further, the drive voltage of a CMOS sensor is lower than that of a charge
coupled device (CCD) sensor, so that power consumption of the solid-state imaging
device can be kept low.

[0004]

Patent Document 1 discloses an imaging device including a CMOS sensor.

[Reference]

[0005]

Patent Document 1: Japanese Published Patent Application No. 2009-141717

DISCLOSURE OF INVENTION

[0006]

5 Development of a photosensor that is small in size and can obtain high-contrast image data with less noise than output signals has been desired.

[0007]

 In view of the foregoing problem, an object of one embodiment of the present invention is to provide a method for driving a photosensor that is small in size and can
10 obtain high-contrast image data. Another object of one embodiment of the present invention is to provide a semiconductor device that includes the photosensor, is small in size, and can obtain high-contrast image data.

[0008]

 A photosensor includes at least a light-receiving element, a transistor which is a
15 switching element, and a charge retention node that is electrically connected to the light-receiving element through the transistor. The light-receiving element generates a current corresponding to the amount of received light. The transistor controls switching between accumulation and retention of charge in the charge retention node. The charge retention node holds charge that varies in accordance with the amount of
20 light received by the light-receiving element.

[0009]

 An example of the operation of a photosensor will be described with reference to FIGS. 1A and 1B. FIG. 1A illustrates an example of the circuit configuration of a photosensor 100.

25 [0010]

 A photodiode 101 which is a light-receiving element generates a current corresponding to the amount of light entering the i-layer. A charge retention node FD holds charge that varies depending on the amount of light received by the photodiode 101. A transistor 102 which is an amplifier element converts a voltage of the charge
30 retention node FD into a current between a wiring OUT and a wiring VR in accordance with the potential of the charge retention node FD. A transistor 103 which is a switching element controls accumulation of charge in the charge retention node FD by

the photodiode 101. A transistor 105 controls an output of the photosensor 100.

[0011]

Note that FIG. 1A shows the case where the photodiode 101 is a PIN junction photodiode. There is no limitation on the photodiode used in one embodiment of the present invention, and a PN junction photodiode or the like can be used.

[0012]

In FIG. 1A, a wiring TX is a signal line for controlling the transistor 103. A wiring SE is a signal line for controlling the transistor 105. A wiring RD is a signal line for controlling initialization of the potential of the charge retention node FD. The wiring OUT is an output wiring for outputting a signal corresponding to charge accumulation in the photodiode 101. The wiring VR is a power supply wiring.

[0013]

Specifically, in the photosensor 100, a first terminal of the transistor 103 is connected to the cathode of the photodiode 101, and a second terminal of the transistor 103 is connected to a gate electrode of the transistor 102. A first terminal of the transistor 102 is connected to the wiring VR supplied with a high-level power supply potential VDD. A second terminal of the transistor 102 is connected to a first terminal of the transistor 105. A second terminal of the transistor 105 is connected to the wiring OUT. A gate electrode of the transistor 105 is connected to the wiring SE, and the wiring SE is supplied with the potential of a signal for controlling the switching of the transistor 105.

[0014]

The "source electrode" and "drain electrode" of a transistor interchange with each other depending on the polarity of the transistor or the levels of potentials applied to the electrodes. In general, in an n-channel transistor, an electrode supplied with a lower potential is called a source electrode, and an electrode supplied with a higher potential is called a drain electrode. Further, in a p-channel transistor, an electrode supplied with a lower potential is called a drain electrode, and an electrode supplied with a higher potential is called a source electrode. In this specification, one of a source electrode and a drain electrode is referred to as a first terminal and the other is referred to as a second terminal to describe a connection relation between a photodiode and a transistor included in a photosensor.

[0015]

In FIG. 1A, a node where the second terminal of the transistor 103 and the gate electrode of the transistor 102 are connected to each other is represented as the charge retention node FD. The potential of the output signal is determined by the amount of charge accumulated in the charge retention node FD. In order to hold charge in the charge retention node FD more reliably, a storage capacitor may be connected to the charge retention node FD.

[0016]

Note that the configuration of a photosensor to which one embodiment of the present invention can be applied is not limited to the above configuration.

[0017]

FIG. 1B illustrates an example of a timing chart of a variety of potentials applied to the wirings in the photosensor 100 illustrated in FIG. 1A.

[0018]

Note that in the timing chart in FIG. 1B, for easy understanding of the operation of the photosensor 100, it is assumed that the wiring TX, the wiring SE, and the wiring RD are supplied with a high-level potential and a low-level potential. Specifically, it is assumed that the wiring TX is supplied with a high-level potential HTX and a low-level potential LTX; the wiring SE, a high-level potential HSE and a low-level potential LSE; and the wiring RD, a high-level potential HRD and a low-level potential LRD.

[0019]

First, at a time T1, the potential of the wiring TX is switched from the potential LTX to the potential HTX. When the potential of the wiring TX changes to the potential HTX, the transistor 103 is turned on. Note that at the time T1, the wiring SE is supplied with the potential LSE, and the wiring RD is supplied with the potential LRD.

[0020]

Next, at a time T2, the potential of the wiring RD is switched from the potential LRD to the potential HRD. At the time T2, the potential of the wiring TX is kept at the potential HTX, and the potential of the wiring SE is kept at the potential LSE. Accordingly, the potential HRD of the wiring RD is supplied to the charge retention node FD, so that the amount of charge held in the charge retention node FD is reset and

charge for setting the charge retention node FD to an initial state is held.

[0021]

Then, at a time T3, the potential of the wiring RD is switched from the potential HRD to the potential LRD. The potential of the charge retention node FD is kept at the potential HRD until shortly before the time T3. Thus, when the potential of the wiring RD changes to the potential LRD, a reverse bias voltage is applied to the photodiode 101. Then, when light enters the photodiode 101 while a reverse bias voltage is applied to the photodiode 101, a current flows from the cathode toward the anode of the photodiode 101. The value of the current varies according to the intensity of light. In other words, as the intensity of light entering the photodiode 101 is higher, the value of the current is higher and the amount of charge leaking from the charge retention node FD is larger. On the other hand, as the intensity of light entering the photodiode 101 is lower, the value of the current is lower and the amount of charge leaking from the charge retention node FD is smaller. Consequently, the higher the intensity of light becomes, the larger the amount of change in the potential of the charge retention node FD becomes; the lower the intensity of light becomes, the smaller the amount of change becomes.

[0022]

Then, at a time T4, when the potential of the wiring TX is switched from the potential HTX to the potential LTX, the transistor 103 is turned off. Accordingly, the movement of charge from the charge retention node FD to the photodiode 101 is stopped, so that the potential of the charge retention node FD is determined.

[0023]

Next, at a time T5, when the potential of the wiring SE is switched from the potential LSE to the potential HSE, the transistor 105 is turned on. Thus, a signal is output from the wiring VR to the wiring OUT in accordance with the potential of the charge retention node FD.

[0024]

Next, at a time T6, when the potential of the wiring SE is switched from the potential HSE to the potential LSE, the movement of charge from the wiring VR to the wiring OUT is stopped and the potential of the wiring OUT is determined. The potential of the wiring OUT corresponds to the potential of the output signal of the

photosensor 100.

[0025]

The above-described series of operations can be classified into a reset operation, an accumulation operation, and a read operation. In other words, the operation from the time T2 to the time T3 corresponds to the reset operation; the operation from the time T3 to the time T4, the accumulation operation; and the operation from the time T5 to the time T6, the read operation. Image data can be obtained by performing the reset operation, the accumulation operation, and the read operation.

[0026]

However, image data obtained through the above series of operations have a problem of low contrast.

[0027]

In view of the above, the present inventors focused attention on parasitic capacitance generated between the gate and drain and the gate and source of the transistor 103.

[0028]

When the gate potential of the transistor 103 with parasitic capacitance suddenly changes from a high potential to a low potential, the potential of the charge retention node FD is decreased (clock feedthrough occurs) at the time T4 at which the accumulation operation ends.

[0029]

Therefore, in FIG. 1B, the potential of the charge retention node FD is decreased from a potential shown by a dotted line to a potential shown by a solid line, and the potential of the wiring OUT is decreased from a potential shown by a dotted line to a potential shown by a solid line.

[0030]

The potential of the charge retention node FD is decreased by clock feedthrough; therefore, the potential of the charge retention node FD is decreased even when the intensity of light entering the photodiode 101 is not high. Consequently, the range of light intensity corresponding to change in the potential of the wiring OUT (the potential of the output signal of the photosensor 100) is narrowed, and the image contrast of obtained image data is lowered.

[0031]

The foregoing problem is caused by the fact that the potential of the wiring TX suddenly changes from the potential HTX to the potential LTX at the time T4 among the series of operations. For that reason, the fall of the pulse signal of the wiring TX needs to be made gentle, thereby suppressing change in the potential of the charge retention node FD (clock feedthrough) due to parasitic capacitance of the transistor 103. Thus, high-contrast image data can be obtained. However, if the fall of the pulse signal of the wiring TX is too gentle, clock feedthrough occurs.

[0032]

In view of the above, one embodiment of the present invention is a method for driving a photosensor including a light-receiving element, a transistor serving as a switching element, and a charge retention node electrically connected to the light-receiving element through the transistor. The reduction in charge held in the charge retention node is suppressed by extending the fall time of the input waveform of a driving pulse that is supplied to the transistor to turn off the transistor.

[0033]

In the method for driving a photosensor according to one embodiment of the present invention, a channel formation region of the transistor, which is a switching element, preferably contains an oxide semiconductor. The transistor in which an oxide semiconductor is used for the channel formation region has an extremely low off-state current and high withstand voltage. Therefore, the use of the transistor as a switching element can prevent leakage of charge accumulated during a charge retention period.

[0034]

One embodiment of the present invention is a method for driving a semiconductor device that includes a photosensor including a light-receiving element, a transistor serving as a switching element, and a charge retention node electrically connected to the light-receiving element through the transistor; and a capacitor electrically connected to a signal line configured to control the transistor. The reduction in charge held in the charge retention node is suppressed by extending, by the capacitor, the fall time of the input waveform of a driving pulse supplied to the transistor to turn off the transistor.

[0035]

In the method for driving a semiconductor device according to one embodiment of the present invention, a channel formation region of the transistor, which is a switching element, preferably contains an oxide semiconductor.

[0036]

5 Another embodiment of the present invention is a semiconductor device that includes a photosensor including a light-receiving element, a transistor, and a charge retention node electrically connected to the light-receiving element through the transistor; and a capacitor electrically connected to a signal line configured to control the transistor. The reduction in charge held in the charge retention node is suppressed
10 by extending, by the capacitor, the fall time of the input waveform of a driving pulse supplied to the transistor to turn off the transistor.

[0037]

In the semiconductor device according to one embodiment of the present invention, a channel formation region of the transistor preferably contains an oxide
15 semiconductor. In the semiconductor device, the transistor functions as a switching element. The transistor in which an oxide semiconductor is used for the channel formation region has an extremely low off-state current and high withstand voltage. Therefore, the use of the transistor as a switching element can prevent leakage of charge accumulated during a charge retention period.

20 [0038]

One embodiment of the present invention is an electronic device including the semiconductor device.

[0039]

Note that in this specification, the term "connection" means electrical
25 connection and corresponds to a state in which current, voltage, or a potential can be supplied or transmitted. Therefore, a state of connection means not only a state of direct connection but also a state of indirect connection through a circuit element such as a wiring, a resistor, a diode, or a transistor, in which current, voltage, or a potential can be supplied or transmitted.

30 [0040]

In addition, even when different components are connected to each other in a circuit diagram, there is actually a case where one conductive film has functions of a

plurality of components, such as a case where part of a wiring serves as an electrode. The term "connection" in this specification also includes in its category such a case where one conductive film has functions of a plurality of components.

[0041]

5 According to one embodiment of the present invention, it is possible to provide a method for driving a photosensor that is small in size and can obtain high-contrast image data. Moreover, according to one embodiment of the present invention, it is possible to provide a semiconductor device that includes the photosensor, is small in size, and can obtain high-contrast image data.

10

BRIEF DESCRIPTION OF DRAWINGS

[0042]

In the accompanying drawings:

15 FIGS. 1A and 1B are an example of a circuit diagram and a timing chart of a photosensor;

FIG. 2 is a timing chart of a photosensor;

FIGS. 3A and 3B are each an example of a circuit diagram of a photosensor;

FIG. 4 is a timing chart of a photosensor;

20 FIGS. 5A to 5C illustrate an example of a method for fabricating a photosensor;

FIGS. 6A to 6D each illustrate an example of the structure of a transistor;

FIGS. 7A to 7E each illustrate an example of an electronic device;

FIG. 8 is a circuit diagram of a photosensor in Example 1;

FIGS. 9A and 9B are graphs showing calculation results in Example 1;

25 FIG. 10 is a graph showing calculation results in Example 1;

FIGS. 11A and 11B each illustrate a waveform of an input to a wiring TX in a photosensor in Example 2;

FIGS. 12A and 12B are histograms showing experiment results in Example 2;

FIGS. 13A and 13B are each a circuit diagram of a photosensor in Example 2;

30 FIG. 14 shows a photosensor reading circuit in Example 2;

FIGS. 15A to 15D show experiment results in Example 2;

FIGS. 16A to 16E each illustrate a crystal structure of an oxide material;

FIGS. 17A to 17C illustrate a crystal structure of an oxide material;

FIGS. 18A to 18C illustrate a crystal structure of an oxide material;

FIG. 19 shows gate voltage dependence of mobility obtained by calculation;

FIGS. 20A to 20C show gate voltage dependence of drain current and mobility,
5 obtained by calculation;

FIGS. 21A to 21C show gate voltage dependence of drain current and mobility,
obtained by calculation;

FIGS. 22A to 22C show gate voltage dependence of drain current and mobility,
obtained by calculation;

10 FIGS. 23A and 23B show cross-sectional structures of transistors used in
calculation;

FIGS. 24A to 24C show results of characteristics of a transistor;

FIGS. 25A and 25B show results of characteristics of a transistor;

FIGS. 26A and 26B show results of characteristics of a transistor;

15 FIG. 27 shows XRD spectra of transistors;

FIG. 28 shows results of characteristics of a transistor;

FIG. 29 shows results of characteristics of a transistor;

FIGS. 30A and 30B show results of characteristics of a transistor;

FIGS. 31A and 31B illustrate a structure of a transistor; and

20 FIGS. 32A and 32B illustrate a structure of a transistor.

BEST MODE FOR CARRYING OUT THE INVENTION

[0043]

Embodiments of the present invention will be hereinafter described in detail
25 with reference to the accompanying drawings. Note that the present invention is not
limited to the following description and it is easily understood by those skilled in the art
that the mode and details can be variously changed without departing from the spirit and
scope of the present invention. Therefore, the present invention should not be
construed as being limited to the description of the embodiments below.

30 [0044]

(Embodiment 1)

In this embodiment, a method for driving a photosensor according to one

embodiment of the present invention will be described. FIG. 1A and FIGS. 3A and 3B illustrate circuit configurations of photosensors used in this embodiment. FIG. 2 and FIG. 4 illustrate examples of timing charts of various potentials applied to the photosensors illustrated in FIG. 1A and FIGS. 3A and 3B.

5 [0045]

A photosensor to which the method for driving a photosensor according to one embodiment of the present invention can be applied includes at least a light-receiving element, a transistor which is a switching element, and a charge retention node that is electrically connected to the light-receiving element through the transistor. The light-receiving element generates a current corresponding to the amount of received light. The transistor controls switching between accumulation and retention of charge in the charge retention node. The charge retention node holds charge that varies in accordance with the amount of light received by the light-receiving element.

[0046]

15 An example of a photosensor to which the method for driving a photosensor according to one embodiment of the present invention can be applied is the photosensor 100 illustrated in FIG. 1A. The configuration and the driving method of the photosensor 100 are as described above, and the timing chart in FIG. 2 can be applied.

[0047]

20 Note that in the timing chart in FIG. 2, for easy understanding of the operation of the photosensor 100, it is assumed that the wiring TX, the wiring SE, and the wiring RD are supplied with a high-level potential and a low-level potential. Specifically, it is assumed that the wiring TX is supplied with the high-level potential HTX and the low-level potential LTX; the wiring SE, the high-level potential HSE and the low-level potential LSE; and the wiring RD, the high-level potential HRD and the low-level potential LRD.

25 [0048]

When the gate potential of the transistor 103 with parasitic capacitance suddenly changes from a high potential to a low potential in the photosensor 100, clock feedthrough occurs. Specifically, the potential of the charge retention node FD is decreased at the time T4 at which the accumulation operation ends.

30 [0049]

The timing chart in such a case is shown in FIG. 1B. In FIG. 1B, the potential of the charge retention node FD is decreased from the potential shown by the dotted line to the potential shown by the solid line, and the potential of the wiring OUT is decreased from the potential shown by the dotted line to the potential shown by the solid line. In such a manner, the image contrast of obtained image data is lowered when clock feedthrough occurs.

[0050]

One of methods for suppressing clock feedthrough is increasing capacitance by an increase in size of the transistor 102. With this method, the size of the photosensor itself is also increased, which means the reduction in size of the photosensor is difficult to achieve and thus it is not preferable to employ this method.

[0051]

In view of the above, in the method for driving a photosensor according to one embodiment of the present invention, the fall of the pulse signal of the wiring TX at the time T4 in the timing chart is made gentle as illustrated in FIG. 2. The fall of the pulse signal can be made gentler than conventional one by extending the fall time of the input waveform of the wiring TX. Thus, change in the potential of the charge retention node FD (clock feedthrough) due to parasitic capacitance of the transistor 103 can be suppressed. Consequently, high-contrast image data can be obtained. Moreover, the reduction in size of the photosensor can be achieved.

[0052]

However, if the fall of the pulse signal of the wiring TX is too gentle, clock feedthrough occurs. The maximum length of the fall time varies depending on the configuration of the circuit and the like; therefore, the fall time can be determined as appropriate in consideration of such features. For example, the fall time of the input waveform of a driving pulse supplied to the transistor 103, which is described later in Example 1, is set longer than 0 seconds and shorter than 200 nanoseconds.

[0053]

In addition, by providing a capacitor electrically connected to the wiring TX in a semiconductor device including the photosensor in this embodiment, the fall time of the input waveform of a driving pulse supplied to the transistor 103 can be extended and the reduction in charge held in the charge retention node FD can be suppressed. For

example, the capacitor may have a capacitance of several microfarads (μF). The upper limit of the capacitance varies depending on the configuration of the circuit and the like; therefore, the capacitance is determined as appropriate in consideration of such features.
[0054]

5 Note that FIG. 1A illustrates the configuration of the photosensor that includes only one transistor 103 functioning as a switching element; however, the present invention is not limited to this configuration. Although the configuration in which one transistor functions as one switching element is described in one embodiment of the present invention, a plurality of transistors may function as one switching element. In
10 the case where a plurality of transistors function as one switching element, the plurality of transistors may be connected to each other in parallel, in series, or in combination of parallel connection and series connection.
[0055]

 In this specification, the state where transistors are connected to each other in
15 series means, for example, a state where only one of a first terminal and a second terminal of a first transistor is connected to only one of a first terminal and a second terminal of a second transistor. Further, the state in which transistors are connected to each other in parallel means a state in which the first terminal of the first transistor is connected to the first terminal of the second transistor and the second terminal of the
20 first transistor is connected to the second terminal of the second transistor.
[0056]

 Note that in FIG. 1A, the transistor 103 has a gate electrode on one side of the active layer. In the case where the transistor 103 has a pair of gate electrodes with the active layer therebetween, a signal for controlling switching is supplied to one of the
25 gate electrodes, and the other of the gate electrodes may be in a floating state (i.e., electrically insulated) or supplied with a potential. In the latter case, potentials with the same level may be applied to the pair of electrodes, or a fixed potential such as a ground potential may be applied only to the other of the gate electrodes. By controlling the level of a potential supplied to the other of the gate electrodes, the
30 threshold voltage of the transistor 103 can be controlled.
[0057]

 There is no limitation on a semiconductor material used for the active layer in

the transistor included in the photosensor of this embodiment. Examples of semiconductor materials are amorphous, microcrystalline, polycrystalline, or single crystal silicon semiconductors, germanium semiconductors, compound semiconductors, and oxide semiconductors.

5 [0058]

In particular, a channel formation region of the transistor 103, which functions as a switching element, preferably contains a semiconductor that has a wider band gap than a silicon semiconductor and has a lower intrinsic carrier density than silicon. For example, a compound semiconductor such as silicon carbide (SiC) or gallium nitride (GaN) or an oxide semiconductor of metal oxide such as zinc oxide (ZnO) can be used. Among the above, an oxide semiconductor has an advantage of high mass productivity because the oxide semiconductor can be formed by sputtering or a wet process (e.g., printing). In addition, the deposition temperature of the oxide semiconductor is as low as 300 °C to 500 °C (the glass transition temperature or lower, approximately 700 °C at the maximum), whereas the process temperature of silicon carbide and that of gallium nitride are approximately 1500 °C and approximately 1100 °C, respectively. Therefore, the oxide semiconductor can be formed over a glass substrate which is inexpensively available. Further, a larger substrate can be used. Consequently, among the wide band gap semiconductors, the oxide semiconductor particularly has an advantage of high mass productivity. Further, in the case where an oxide semiconductor with high crystallinity is to be obtained in order to improve the performance (e.g., field-effect mobility) of a transistor, the oxide semiconductor with crystallinity can be easily obtained by heat treatment at 250 °C to 800 °C.

[0059]

25 When the channel formation region contains such a semiconductor material having the above characteristics, the transistor 103 can have an extremely low off-state current and high withstand voltage. Further, the use of the transistor 103 as a switching element can prevent leakage of charge accumulated during a charge retention period.

30 [0060]

Unless otherwise specified, in the case of an n-channel transistor, an off-state

current in this specification is a current that flows between a source electrode and a drain electrode when the potential of the drain electrode is higher than that of the source electrode and that of a gate electrode while the voltage between the gate electrode and the source electrode is less than or equal to zero. Further, in the case of a p-channel transistor, an off-state current in this specification is a current that flows between a source electrode and a drain electrode when the potential of the drain electrode is lower than that of the source electrode or that of a gate electrode while the potential between the gate electrode and the source is greater than or equal to zero.

[0061]

In one embodiment of the present invention, the photosensor can be driven with a rolling shutter. Moreover, the photosensor can also be driven with a global shutter.

[0062]

In a solid-state imaging device to which the method for driving a photosensor according to one embodiment of the present invention is applied, an image can be captured using external light and also by using light from a backlight instead of external light as in a contact area sensor, for example. In the case of using a backlight in one embodiment of the present invention, color image data may be obtained by field sequential driving (FS operation) of the backlight. By the FS operation, color image data can be obtained by additive color mixing using plural pieces of image data corresponding to a plurality of colors.

[0063]

Another example of a photosensor to which the method for driving a photosensor according to one embodiment of the present invention can be applied is a photosensor 110 illustrated in FIG. 3A. Like the photosensor 100, the photosensor 110 includes the photodiode 101 which is a light-receiving element, the transistor 102 which is an amplifier element, the transistor 103 which is a switching element, and the transistor 105 that controls an output of the photosensor. The photosensor 110 also includes a transistor 107 that has a function of resetting the amount of charge accumulated in the charge retention node FD.

[0064]

Specifically, in the photosensor 110, a first terminal of the transistor 103 is

connected to the cathode of the photodiode 101, and a second terminal of the transistor 103 is connected to a gate electrode of the transistor 102 and a first terminal of the transistor 107. A first terminal of the transistor 102 and a second terminal of the transistor 107 are connected to the wiring VR supplied with the high-level power supply potential VDD. A gate electrode of the transistor 107 is connected to a wiring RS, and the wiring RS is supplied with a potential of a signal for controlling the switching of the transistor 107. A second terminal of the transistor 102 is connected to a first terminal of the transistor 105. A second terminal of the transistor 105 is connected to the wiring OUT. A gate electrode of the transistor 105 is connected to the wiring SE, and the wiring SE is supplied with the potential of a signal for controlling the switching of the transistor 105.

[0065]

In FIG. 3A, a node where the second terminal of the transistor 103, the first terminal of the transistor 107, and the gate electrode of the transistor 102 are connected to each other is represented as the charge retention node FD. The potential of the output signal is determined by the amount of charge accumulated in the charge retention node FD. In order to hold charge in the charge retention node FD more reliably, a capacitor may be connected to the charge retention node FD.

[0066]

Next, an example of the operation of the photosensor 110 in FIG. 3A will be described. FIG. 4 illustrates a timing chart of various potentials supplied to the photosensor 110 in FIG. 3A, as an example.

[0067]

Note that in the timing chart in FIG. 4, for easy understanding of the operation of the photosensor 110, it is assumed that the wiring TX, the wiring SE, and the wiring RS are supplied with a high-level potential and a low-level potential. Specifically, it is assumed that the wiring TX is supplied with the high-level potential HTX and the low-level potential LTX; the wiring SE, the high-level potential HSE and the low-level potential LSE; and the wiring RS, a high-level potential HRS and a low-level potential LRS. The wiring RD is supplied with a low-level power supply potential VSS.

[0068]

First, at a time T1, the potential of the wiring TX is switched from the potential

LTX to the potential HTX. When the potential of the wiring TX changes to the potential HTX, the transistor 103 is turned on. At the time T1, the wiring SE is supplied with the potential LSE, and the wiring RS is supplied with the potential LRS.

[0069]

5 Next, at a time T2, the potential of the wiring RS is switched from the potential LRS to the potential HRS. When the potential of the wiring RS changes to the potential HRS, the transistor 107 is turned on. At the time T2, the potential of the wiring TX is kept at the potential HTX, and the potential of the wiring SE is kept at the potential LSE. Accordingly, the node FD is supplied with the power supply potential
10 VDD, so that the amount of charge held in the node FD is reset. Further, a reverse bias voltage is applied to the photodiode 101.

[0070]

 Then, at a time T3, the potential of the wiring RS is switched from the potential HRS to the potential LRS. The potential of the charge retention node FD remains at
15 the power supply potential VDD until shortly before the time T3. Thus, even after the potential of the wiring RS changes to the potential LRS, a reverse bias voltage continues to be applied to the photodiode 101. Then, when light enters the photodiode 101 in that state, a current flows from the cathode toward the anode of the photodiode 101. The value of the current varies depending on the intensity of light. In other words, as
20 the intensity of light entering the photodiode 101 increases, the value of the current increases and the amount of charge leaking from the charge retention node FD also increases. In contrast, as the intensity of light entering the photodiode 101 decreases, the value of the current decreases and the amount of charge leaking from the charge retention node FD also decreases. Thus, the higher the intensity of light becomes, the
25 larger the amount of change in the potential of the charge retention node FD becomes; the lower the intensity of light becomes, the smaller the amount of change becomes.

[0071]

 Then, at a time T4, when the potential of the wiring TX is switched from the potential HTX to the potential LTX, the transistor 103 is turned off. Accordingly, the
30 movement of charge from the charge retention node FD to the photodiode 101 is stopped, so that the potential of the charge retention node FD is determined.

[0072]

Here, the fall of the pulse signal at the time when the potential of the wiring TX is switched from the potential HTX to the potential LTX is made gentle in the method for driving a photosensor according to one embodiment of the present invention. The fall of the pulse signal can be made gentler than conventional one by extending the fall time of the input waveform of the wiring TX. Thus, change in the potential of the charge retention node FD (clock feedthrough) due to parasitic capacitance of the transistor 103 can be suppressed. Consequently, high-contrast image data can be obtained.

[0073]

Next, at a time T5, when the potential of the wiring SE is switched from the potential LSE to the potential HSE, the transistor 105 is turned on. Then, charge is moved from the wiring VR to the wiring OUT in accordance with the potential of the charge retention node FD.

[0074]

Next, at a time T6, when the potential of the wiring SE is switched from the potential HSE to the potential LSE, the movement of charge from the wiring VR to the wiring OUT is stopped and the potential of the wiring OUT is determined. The potential of the wiring OUT corresponds to the potential of the output signal of the photosensor 110. Moreover, the potential of the output signal contains data of a captured image of an object.

[0075]

The above series of operations can be classified into a reset operation, an accumulation operation, and a read operation. In other words, the operation from the time T1 to the time T3 corresponds to the reset operation; the operation from the time T3 to the time T4, the accumulation operation; and the operation from the time T5 to the time T6, the read operation. Image data can be obtained by performing the reset operation, the accumulation operation, and the read operation.

[0076]

Next, the configuration of a photosensor 111, which is different from the photosensors illustrated in FIG. 1A and FIG. 3A, will be described with reference to FIG. 3B.

[0077]

Like the photosensor 110, the photosensor 111 in FIG. 3B includes the photodiode 101 which is a light-receiving element, the transistor 102 which is an amplifier element, the transistor 103 which is a switching element, the transistor 105 that controls an output of the photosensor, and the transistor 107 that has a function of resetting the amount of charge accumulated in the charge retention node FD.

[0078]

Specifically, in the photosensor 111, a first terminal of the transistor 103 is connected to the cathode of the photodiode 101, and a second terminal of the transistor 103 is connected to a gate electrode of the transistor 102 and a first terminal of the transistor 107. A first terminal of the transistor 102 is connected to a second terminal of the transistor 105, and the second terminal of the transistor 102 is connected to the wiring OUT. A first terminal of the transistor 105 and a second terminal of the transistor 107 are connected to the wiring VR supplied with the high-level power supply potential VDD. A gate electrode of the transistor 107 is connected to the wiring RS, and the wiring RS is supplied with a potential of a signal for controlling the switching of the transistor 107. A gate electrode of the transistor 105 is connected to the wiring SE, and the wiring SE is supplied with the potential of a signal for controlling the switching of the transistor 105.

[0079]

In FIG. 3B, a node where the second terminal of the transistor 103, the first terminal of the transistor 107, and the gate electrode of the transistor 102 are connected to each other is represented as the charge retention node FD. The potential of the output signal is determined by the amount of charge accumulated in the charge retention node FD. In order to hold charge in the charge retention node FD more reliably, a capacitor may be connected to the charge retention node FD.

[0080]

For the operation of the photosensor 111, the timing chart in FIG. 4 can be referred to.

[0081]

In the method for driving a photosensor according to one embodiment of the present invention, the fall of the pulse signal of the wiring TX at the time T4 in the timing charts in FIG. 2 and FIG. 4 is made gentle. Thus, change in the potential of the

charge retention node FD (clock feedthrough) due to parasitic capacitance of the transistor 103 can be suppressed. Consequently, high-contrast image data can be obtained.

[0082]

5 As described above, one embodiment of the present invention is a method for driving a photosensor including a light-receiving element, a transistor serving as a switching element, and a charge retention node electrically connected to the light-receiving element through the transistor. The reduction in charge held in the charge retention node is suppressed by extending the fall time of the input waveform of
10 a driving pulse that is supplied to the transistor to turn off the transistor. A photosensor that is small in size and can obtain high-contrast image data can be provided as a result.

[0083]

This embodiment can be implemented in combination with any of the other embodiments.

15 [0084]

(Embodiment 2)

In this embodiment, an example of a method for fabricating a photosensor to which one embodiment of the present invention can be applied will be described with reference to FIGS. 5A to 5C.

20 [0085]

As a semiconductor material for a transistor used in one embodiment of the present invention, an oxide semiconductor, germanium, silicon, silicon germanium, single crystal silicon carbide, or the like may be used. For example, a transistor including silicon can be formed using a single crystal semiconductor substrate such as a
25 silicon wafer, a silicon thin film formed by SOI, a silicon thin film formed by vapor deposition, or the like.

[0086]

In this embodiment, a transistor including silicon as a semiconductor material and a transistor including an oxide semiconductor as a semiconductor material are used.

30 [0087]

An oxide semiconductor used in this embodiment is an i-type (intrinsic) oxide semiconductor or a substantially i-type (intrinsic) oxide semiconductor. The i-type

(intrinsic) or substantially i-type oxide semiconductor is obtained in such a manner that hydrogen, which functions as an impurity imparting n-type conductivity, is removed, and the oxide semiconductor is purified so as to contain as few impurities that are not main components of the oxide semiconductor as possible.

5 [0088]

Note that the purified oxide semiconductor includes extremely few carriers, and the carrier concentration is lower than $1 \times 10^{14} / \text{cm}^3$, preferably lower than $1 \times 10^{12} / \text{cm}^3$, further preferably lower than $1 \times 10^{11} / \text{cm}^3$. Such few carriers enable a current in the off state (off-state current) to be sufficiently low.

10 [0089]

Specifically, in the transistor including the oxide semiconductor layer, the leakage current density (off-state current density) per micrometer of a channel width between the source and the drain in the off state can be $100 \text{ zA}/\mu\text{m}$ ($1 \times 10^{-19} \text{ A}/\mu\text{m}$) or less, preferably $10 \text{ zA}/\mu\text{m}$ ($1 \times 10^{-20} \text{ A}/\mu\text{m}$) or less, and further preferably $1 \text{ zA}/\mu\text{m}$ ($1 \times 10^{-21} \text{ A}/\mu\text{m}$) or less with a source-drain voltage of 3.5 V at ambient temperature (e.g., 25 °C).

[0090]

In the transistor including a purified oxide semiconductor layer, the temperature dependence of on-state current is hardly observed, and off-state current remains extremely low at high temperature.

20 [0091]

Steps for fabricating a photosensor that includes a transistor 705 including silicon as a semiconductor material and a transistor 724 including an oxide semiconductor as a semiconductor material, to which one embodiment of the present invention can be applied, will be described below with reference to FIGS. 5A to 5C.

25 [0092]

First, as illustrated in FIG. 5A, a photodiode 704 and the n-channel transistor 705 are formed over an insulating surface of a substrate 700 by a known CMOS fabrication method. In this embodiment, the case where the photodiode 704 and the n-channel transistor 705 are formed with a single crystal semiconductor film that is separated from a single crystal semiconductor substrate is given as an example.

[0093]

A specific example of a method for forming the single crystal semiconductor film will be briefly described. First, an ion beam including ions that are accelerated by an electric field enters the single crystal semiconductor substrate, and a fragile layer which is weakened by local disorder of the crystal structure is formed in a region at a certain depth from the surface of the semiconductor substrate. The depth at which the fragile layer is formed can be adjusted by the acceleration energy of the ion beam and the angle at which the ion beam enters. Then, the semiconductor substrate and the substrate 700 over which an insulating film 701 is formed are attached to each other so that the insulating film 701 is sandwiched therebetween. After the semiconductor substrate and the substrate 700 overlap with each other, a pressure of about 1 N/cm² to 500 N/cm², preferably about 11 N/cm² to 20 N/cm² is applied to part of the semiconductor substrate and the substrate 700 to attach the substrates. When the pressure is applied, bonding between the semiconductor substrate and the insulating film 701 starts from the portion to which the pressure is applied, which results in bonding of the entire surface where the semiconductor substrate and the insulating film 701 are in close contact with each other. Next, heat treatment is performed, whereby very small voids that exist in the fragile layer are combined, so that the very small voids increase in volume. As a result, the single crystal semiconductor film which is part of the semiconductor substrate is separated from the semiconductor substrate along the fragile layer. The heat treatment is performed at a temperature not exceeding the strain point of the substrate 700. Then, the single crystal semiconductor film is processed into a desired shape by etching or the like, so that an island-shaped semiconductor film 702 and an island-shaped semiconductor film 703 can be formed.

[0094]

The photodiode 704 is formed using the island-shaped semiconductor film 702 over the insulating film 701. The n-channel transistor 705 is formed using the island-shaped semiconductor film 703 over the insulating film 701. The photodiode 704 is a lateral junction type photodiode in which a region 727 having p-type conductivity, a region 728 having i-type conductivity, and a region 729 having n-type conductivity are formed in the island-shaped semiconductor film 702. The n-channel transistor 705 includes a gate electrode 707 and also includes an insulating film 708

between the island-shaped semiconductor film 703 and the gate electrode 707.

[0095]

Note that the region 728 having i-type conductivity refers to a region of the semiconductor film which contains an impurity imparting p-type or n-type conductivity at a concentration of $1 \times 10^{20} \text{ cm}^{-3}$ or less and has photoconductivity 100 or more times as high as dark conductivity. The region 728 having i-type conductivity includes, in its category, a region that contains an impurity element belonging to Group 13 or Group 15 of the periodic table. An i-type semiconductor has weak n-type electric conductivity when an impurity element for controlling valence electrons is not added intentionally. Therefore, the region 728 having i-type conductivity includes, in its category, a region to which an impurity element imparting p-type conductivity is added intentionally or unintentionally at the same time as or after the film formation.

[0096]

Although there is no particular limitation on the substrate 700, the substrate 700 is preferably a substrate that has an insulating surface and has barrier properties with respect to impurities including a hydrogen atom (e.g., water vapor, a hydrogen gas, and a hydrogen ion). If heat treatment is performed in a later step, the substrate 700 needs to have heat resistance at least high enough to withstand the heat treatment.

[0097]

For example, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like, a quartz substrate, a sapphire substrate, or a ceramic substrate may be used. Alternatively, a metal substrate containing stainless steel or a semiconductor substrate having an insulating film formed on its surface may be used. A flexible substrate formed using a synthetic resin such as plastics generally tends to have a lower upper temperature limit than the above substrates; such a substrate can be used as long as it can withstand processing temperature in the fabrication process. Note that the surface of the substrate 700 may be planarized by polishing such as CMP.

[0098]

Note that although the case where the photodiode 704 and the n-channel transistor 705 are formed using the single crystal semiconductor film is described as an example in this embodiment, the present invention is not limited to this structure. For example, a polycrystalline or microcrystalline semiconductor film that is formed over

the insulating film 701 by vapor deposition may be used. Alternatively, the above semiconductor film may be crystallized with a known technique. Examples of the known technique of crystallization are a laser crystallization method using a laser beam and a crystallization method using a catalytic element. Alternatively, it is possible to use a crystallization method using a catalytic element and a laser crystallization method in combination. In the case of using a heat-resistant substrate such as a quartz substrate, it is possible to combine any of the following crystallization methods: a thermal crystallization method using an electrically heated oven, a lamp annealing crystallization method using infrared light, a crystallization method using a catalytic element, and a high-temperature annealing method at approximately 950 °C.

[0099]

After a conductive film is formed over the insulating film 708, the conductive film is processed into a desired shape by etching or the like, whereby a wiring 711 is formed together with the gate electrode 707.

[0100]

Next, an insulating film 712 is formed so as to cover the photodiode 704, the n-channel transistor 705, and the wiring 711. Note that although the case where a single-layer insulating film is used as the insulating film 712 is described as an example in this embodiment, the insulating film 712 is not necessarily a single-layer film and may be a stack including two or more insulating films.

[0101]

The insulating film 712 is formed using a material that can withstand a temperature of heat treatment in a later fabrication step. Specifically, it is preferable to use silicon oxide, silicon nitride, silicon nitride oxide, silicon oxynitride, aluminum nitride, aluminum oxide, or the like for the insulating film 712.

[0102]

Note that in this specification, oxynitride refers to a material containing a higher quantity of oxygen than that of nitrogen, and nitride oxide refers to a material containing a higher quantity of nitrogen than that of oxygen.

[0103]

A surface of the insulating film 712 may be planarized by CMP or the like.

[0104]

Next, a gate electrode 713 is formed over the insulating film 712 (FIG. 5A).

[0105]

The gate electrode 713 can be formed with a single-layer structure or a stacked structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, neodymium, or scandium; an alloy material that contains any of these metals as a main component; or conductive oxide. Note that aluminum or copper can also be used as the metal material if it can withstand the temperature of heat treatment performed in a later step. Aluminum and copper are preferably used in combination with a refractory metal material so as to avoid problems of heat resistance and corrosion. As the refractory metal material, molybdenum, titanium, chromium, tantalum, tungsten, neodymium, scandium, or the like can be used.

[0106]

Alternatively, the gate electrode 713 may have a structure in which a copper film is stacked over an alloy film of copper, magnesium, and aluminum. By using the alloy film of copper, magnesium, and aluminum, the adhesion between the gate electrode 713 and the insulating film 712 can be increased.

[0107]

Next, a gate insulating layer 714 is formed over the gate electrode 713. The gate insulating layer 714 can be formed by plasma CVD, sputtering, or the like. The gate insulating layer 714 can be formed with a single-layer structure or a stacked structure using one or more selected from a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, an aluminum nitride oxide film, a hafnium oxide film, a tantalum oxide film, a gallium oxide film, and the like.

[0108]

For the oxide semiconductor in this embodiment, an oxide semiconductor that is made to be an i-type semiconductor or a substantially i-type semiconductor (a purified oxide semiconductor) by removing an impurity is used. Such a purified oxide semiconductor is highly sensitive to an interface state and interface charge; therefore, the interface between the oxide semiconductor layer and the gate insulating layer is important. For that reason, the gate insulating layer that is to be in contact with the purified oxide semiconductor needs to have high quality.

[0109]

For example, high-density plasma-enhanced CVD using microwaves (e.g., a frequency of 2.45 GHz) is preferable because a dense high-quality insulating film having high withstand voltage can be formed. When the purified oxide semiconductor and the high-quality gate insulating film are in close contact with each other, the interface state density can be reduced and favorable interface characteristics can be obtained.

[0110]

Needless to say, a different film formation method such as sputtering or plasma CVD can be used as long as a high-quality insulating film can be formed as the gate insulating layer 714. Alternatively, it is possible to form an insulating film whose film quality and characteristics of the interface with the oxide semiconductor are improved by heat treatment performed after deposition. In any case, any insulating film can be used as long as it has a reduced interface state density with the oxide semiconductor and can form a favorable interface as well as having a favorable film quality as the gate insulating layer.

[0111]

Note that the gate insulating layer 714 is in contact with the oxide semiconductor formed later. Hydrogen contained in the oxide semiconductor adversely affects characteristics of the transistor; therefore, it is preferable that the gate insulating layer 714 do not contain hydrogen, a hydroxyl group, and moisture. In order that the gate insulating layer 714 contains as little hydrogen, a hydroxyl group, and moisture as possible, impurities adsorbed on the substrate 700, such as moisture or hydrogen, are preferably eliminated and removed by preheating the substrate 700, over which the gate electrode 713 is formed, in a preheating chamber of a sputtering apparatus as a pretreatment for film formation. The temperature for the preheating is 100 °C to 400 °C, preferably 150 °C to 300 °C. As an exhaustion unit provided in the preheating chamber, a cryopump is preferably used. Note that this preheating treatment can be omitted.

[0112]

Next, an oxide semiconductor film having a thickness of 2 nm to 200 nm, preferably 3 nm to 50 nm, further preferably 3 nm to 20 nm is formed over the gate

insulating layer 714. The oxide semiconductor film can be formed, for example, by sputtering in a rare gas (e.g., argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas (e.g., argon) and oxygen.

[0113]

5 Note that before the oxide semiconductor film is formed by sputtering, dust attached to a surface of the gate insulating layer 714 is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which an RF power source is used for application of voltage to a substrate side in an argon atmosphere to generate plasma in the vicinity of
10 the substrate to modify a surface. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, or the like may be used. Alternatively, an argon atmosphere to which oxygen, nitrous oxide, or the like is added may be used. Further alternatively, an argon atmosphere to which chlorine, carbon tetrafluoride, or the like is added may be used.

15 [0114]

 An oxide semiconductor used for the oxide semiconductor film preferably contains at least indium (In) or zinc (Zn). In particular, In and Zn are preferably contained. As a stabilizer for reducing variation in electric characteristics of a transistor using the oxide semiconductor, gallium (Ga) is preferably additionally
20 contained. Tin (Sn) is preferably contained as a stabilizer. Hafnium (Hf) is preferably contained as a stabilizer. Aluminum (Al) is preferably contained as a stabilizer.

[0115]

 As another stabilizer, one or plural kinds of lanthanoid such as lanthanum (La),
25 cerium (Ce), praseodymium (Pr), neodymium (Nd), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Tm), ytterbium (Yb), and lutetium (Lu) may be contained.

[0116]

 As the oxide semiconductor, any of the following oxides can be used, for
30 example: indium oxide; tin oxide; zinc oxide; oxides of two metal elements such as In-Zn-based oxide, Sn-Zn-based oxide, Al-Zn-based oxide, Zn-Mg-based oxide, Sn-Mg-based oxide, In-Mg-based oxide, and In-Ga-based oxide; oxides of three metal

elements such as In-Ga-Zn-based oxide (also referred to as IGZO), In-Al-Zn-based oxide, In-Sn-Zn-based oxide, Sn-Ga-Zn-based oxide, Al-Ga-Zn-based oxide, Sn-Al-Zn-based oxide, In-Hf-Zn-based oxide, In-La-Zn-based oxide, In-Ce-Zn-based oxide, In-Pr-Zn-based oxide, In-Nd-Zn-based oxide, In-Sm-Zn-based oxide, In-Eu-Zn-based oxide, In-Gd-Zn-based oxide, In-Tb-Zn-based oxide, In-Dy-Zn-based oxide, In-Ho-Zn-based oxide, In-Er-Zn-based oxide, In-Tm-Zn-based oxide, In-Yb-Zn-based oxide, and In-Lu-Zn-based oxide; and oxides of four metal elements such as In-Sn-Ga-Zn-based oxide, In-Hf-Ga-Zn-based oxide, In-Al-Ga-Zn-based oxide, In-Sn-Al-Zn-based oxide, In-Sn-Hf-Zn-based oxide, and In-Hf-Al-Zn-based oxide.

10 [0117]

Note that here, for example, an In-Ga-Zn-based oxide means an oxide containing In, Ga, and Zn as its main component, and there is no particular limitation on the ratio of In, Ga, and Zn. The In-Ga-Zn-based oxide may contain a metal element other than the In, Ga, and Zn.

15 [0118]

Alternatively, the oxide semiconductor film can be formed using an oxide semiconductor obtained by adding SiO₂ to any of the above metal oxides.

[0119]

Moreover, the oxide semiconductor film can be formed using an oxide semiconductor represented by the chemical formula $\text{InMO}_3(\text{ZnO})_m$ ($m > 0$). Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co.

[0120]

For example, it is possible to use an In-Ga-Zn-based oxide with an atomic ratio of In:Ga:Zn = 1:1:1 (=1/3:1/3:1/3) or In:Ga:Zn = 2:2:1 (= 2/5:2/5:1/5), or an oxide whose composition is in the neighborhood of the above compositions. Alternatively, it is possible to use an In-Sn-Zn-based oxide with an atomic ratio of In:Sn:Zn = 1:1:1 (= 1/3:1/3:1/3), In:Sn:Zn = 2:1:3 (= 1/3:1/6:1/2), or In:Sn:Zn = 2:1:5 (= 1/4:1/8:5/8), or an oxide whose composition is in the neighborhood of the above compositions.

[0121]

Without limitation to the above, an oxide semiconductor with an appropriate composition ratio can be used in accordance with desired semiconductor characteristics

(e.g., mobility, threshold voltage, and variation). In order to obtain needed semiconductor characteristics, an oxide semiconductor preferably has appropriate carrier concentration, impurity concentration, defect density, atomic ratio of a metal element to oxygen, interatomic distance, density, or the like.

5 [0122]

For example, high mobility is relatively easy to obtain with an In-Sn-Zn-based oxide. Even when an In-Ga-Zn-based oxide is used, the mobility can be increased by a reduction in bulk defect density.

[0123]

10 Note that the case where the composition of an oxide having an atomic ratio of In:Ga:Zn = $a:b:c$ ($a+b+c = 1$) is in the neighborhood of the composition of an oxide having an atomic ratio of In:Ga:Zn = $A:B:C$ ($A+B+C = 1$) means that a , b , and c satisfy the following relation: $(a-A)^2 + (b-B)^2 + (c-C)^2 \leq r^2$, where r is 0.05, for example. The same can be applied to other oxides.

15 [0124]

The oxide semiconductor may be single crystal or non-single-crystal. A non-single-crystal oxide semiconductor may be amorphous or polycrystalline. Further, the oxide semiconductor may have an amorphous structure including a portion having crystallinity or a non-amorphous structure.

20 [0125]

In an oxide semiconductor in an amorphous state, a flat surface can be obtained with relative ease. When a transistor is formed using the oxide semiconductor in an amorphous state, interface scattering can be reduced, and relatively high mobility can be obtained with relative ease.

25 [0126]

In an oxide semiconductor having crystallinity, defects in the bulk can be further reduced. When a surface flatness is improved, mobility higher than that of an oxide semiconductor in an amorphous state can be obtained. In order to improve the surface flatness, the oxide semiconductor is preferably formed on a flat surface.

30 Specifically, it is preferable that the oxide semiconductor be formed on a surface with an average surface roughness (R_a) of 1 nm or less, preferably 0.3 nm or less, further

preferably 0.1 nm or less.

[0127]

Note that R_a is obtained by expanding centerline average roughness, which is defined by JIS B 0601, into three dimensions so as to be applicable to a surface.

5 Moreover, R_a can be expressed as average value of the absolute values of deviations from a reference surface to a specific surface and is defined by Formula 1.

[0128]

[Formula 1]

$$Ra = \frac{1}{S_0} \int_{y_1}^{y_2} \int_{x_1}^{x_2} |f(x, y) - Z_0| dx dy$$

10 [0129]

Note that in Formula 1, S_0 represents the area of a measurement surface (a rectangular region defined by four points represented by the coordinates (x_1, y_1) , (x_1, y_2) , (x_2, y_1) , and (x_2, y_2)), and Z_0 represents average height of the measurement surface. Further, R_a can be measured with an atomic force microscope (AFM).

15 [0130]

Here, as an oxide semiconductor having crystallinity, an oxide including a crystal with c-axis alignment (also referred to as a c-axis aligned crystal (CAAC)), which has a triangular or hexagonal atomic arrangement when seen from the direction of an a-b plane, a surface, or an interface, will be described. In the crystal, metal
20 atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner along the c-axis, and the direction of the a-axis or the b-axis is varied in the a-b plane (the crystal rotates around the c-axis).

[0131]

In a broad sense, an oxide including CAAC means a non-single-crystal oxide
25 including a phase that has a triangular, hexagonal, regular triangular, or regular hexagonal atomic arrangement when seen from the direction perpendicular to the a-b plane and in which metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis direction.

30 [0132]

The CAAC is not a single crystal, but this does not mean that the CAAC is composed of only an amorphous component. Although the CAAC includes a crystallized portion (crystalline portion), a boundary between one crystalline portion and another crystalline portion is not clear in some cases.

5 [0133]

In the case where oxygen is included in the CAAC, nitrogen may be substituted for part of oxygen included in the CAAC. The c-axes of individual crystalline portions included in the CAAC may be aligned in one direction (e.g., a direction perpendicular to a surface of a substrate over which the CAAC is formed or a surface of the CAAC).
10 Alternatively, the normals of the a-b planes of the individual crystalline portions included in the CAAC may be aligned in one direction (e.g., a direction perpendicular to a surface of a substrate over which the CAAC is formed or a surface of the CAAC).

[0134]

The CAAC becomes a conductor, a semiconductor, or an insulator depending
15 on its composition or the like. The CAAC transmits or does not transmit visible light depending on its composition or the like.

[0135]

An example of such a CAAC is a crystal which is formed into a film shape and has a triangular or hexagonal atomic arrangement when observed from the direction
20 perpendicular to a surface of the film or a surface of a supporting substrate, and in which metal atoms are arranged in a layered manner or metal atoms and oxygen atoms (or nitrogen atoms) are arranged in a layered manner when a cross section of the film is observed.

[0136]

25 Examples of a crystal structure of the CAAC will be described in detail with reference to FIGS. 16A to 16E, FIGS. 17A to 17C, and FIGS. 18A to 18C. In FIGS. 16A to 16E, FIGS. 17A to 17C, and FIGS. 18A to 18C, the vertical direction corresponds to the c-axis direction and a plane perpendicular to the c-axis direction corresponds to the a-b plane, unless otherwise specified. In the case where the
30 expressions "an upper half" and "a lower half" are simply used, they refer to an upper half above the a-b plane and a lower half below the a-b plane (an upper half and a lower half with respect to the a-b plane). Furthermore, in FIGS. 16A to 16E, O surrounded

by a circle represents tetracoordinate O and O surrounded by a double circle represents tricoordinate O.

[0137]

FIG. 16A illustrates a structure including one hexacoordinate In atom and six
5 tetracoordinate oxygen (hereinafter referred to as tetracoordinate O) atoms proximate to the In atom. Here, a structure including one metal atom and oxygen atoms proximate thereto is referred to as a small group. The structure in FIG. 16A is actually an octahedral structure, but is illustrated as a planar structure for simplicity. Note that three tetracoordinate O atoms exist in each of an upper half and a lower half in FIG. 16A.
10 In the small group illustrated in FIG. 16A, electric charge is 0.

[0138]

FIG. 16B illustrates a structure including one pentacoordinate Ga atom, three
tricoordinate oxygen (hereinafter referred to as tricoordinate O) atoms proximate to the Ga atom, and two tetracoordinate O atoms proximate to the Ga atom. All the
15 tricoordinate O atoms exist on the a-b plane. One tetracoordinate O atom exists in each of an upper half and a lower half in FIG. 16B. An In atom can also have the structure illustrated in FIG. 16B because an In atom can have five ligands. In the small group illustrated in FIG. 16B, electric charge is 0.

[0139]

FIG. 16C illustrates a structure including one tetracoordinate Zn atom and four
20 tetracoordinate O atoms proximate to the Zn atom. In FIG. 16C, one tetracoordinate O atom exists in an upper half and three tetracoordinate O atoms exist in a lower half. Alternatively, three tetracoordinate O atoms may exist in the upper half and one tetracoordinate O atom may exist in the lower half in FIG. 16C. In the small group
25 illustrated in FIG. 16C, electric charge is 0.

[0140]

FIG. 16D illustrates a structure including one hexacoordinate Sn atom and six
tetracoordinate O atoms proximate to the Sn atom. In FIG. 16D, three tetracoordinate
O atoms exist in each of an upper half and a lower half. In the small group illustrated
30 in FIG. 16D, electric charge is +1.

[0141]

FIG. 16E illustrates a small group including two Zn atoms. In FIG. 16E, one

tetracoordinate O atom exists in each of an upper half and a lower half. In the small group illustrated in FIG. 16E, electric charge is -1 .

[0142]

Here, a plurality of small groups form a medium group, and a plurality of medium groups form a large group (also referred to as a unit cell).

[0143]

Now, a rule of bonding between the small groups will be described. The three O atoms in the upper half with respect to the hexacoordinate In atom in FIG. 16A each have three proximate In atoms in the downward direction, and the three O atoms in the lower half each have three proximate In atoms in the upward direction. The one O atom in the upper half with respect to the pentacoordinate Ga atom in FIG. 16B has one proximate Ga atom in the downward direction, and the one O atom in the lower half has one proximate Ga atom in the upward direction. The one O atom in the upper half with respect to the tetracoordinate Zn atom in FIG. 16C has one proximate Zn atom in the downward direction, and the three O atoms in the lower half each have three proximate Zn atoms in the upward direction. In this manner, the number of the tetracoordinate O atoms proximate to and above the metal atom is equal to the number of the metal atoms proximate to and below each of the tetracoordinate O atoms. Similarly, the number of the tetracoordinate O atoms proximate to and below the metal atom is equal to the number of the metal atoms proximate to and above each of the tetracoordinate O atoms. Since O atoms contributing the bonding between the small groups are the tetracoordinate O atoms, the sum of the number of the metal atoms proximate to and below the O atom and the number of the metal atoms proximate to and above the O atom is 4. Accordingly, when the sum of the number of tetracoordinate O atoms above a metal atom and the number of tetracoordinate O atoms below another metal atom is 4, the two kinds of small groups including the metal atoms can be bonded. For example, in the case where the hexacoordinate metal (In or Sn) atom is bonded through three tetracoordinate O atoms in the lower half, it is bonded to the pentacoordinate metal (Ga or In) atom or the tetracoordinate metal (Zn) atom.

[0144]

A metal atom having the above coordination number is bonded to another metal atom having the above coordination number through a tetracoordinate O atom in

the c-axis direction. In addition to the above, a medium group can be formed in a different manner by combining a plurality of small groups so that the total electric charge of the layered structure is 0.

[0145]

FIG. 17A illustrates a model of a medium group included in a layered structure of an In-Sn-Zn-O-based material. FIG. 17B illustrates a large group including three medium groups. FIG. 17C illustrates an atomic arrangement in the case where the layered structure in FIG. 17B is observed from the c-axis direction.

[0146]

In FIG. 17A, for simplicity, a tricoordinate O atom is omitted and tetracoordinate O atoms are shown by a circle; the number in the circle shows the number of tetracoordinate O atoms. For example, three tetracoordinate O atoms existing in each of an upper half and a lower half with respect to a Sn atom are denoted by circled 3. Similarly, in FIG. 17A, one tetracoordinate O atom existing in each of an upper half and a lower half with respect to an In atom is denoted by circled 1. FIG. 17A also illustrates a Zn atom proximate to one tetracoordinate O atom in a lower half and three tetracoordinate O atoms in an upper half, and a Zn atom proximate to one tetracoordinate O atom in an upper half and three tetracoordinate O atoms in a lower half.

[0147]

In the medium group included in the layered structure of the In-Sn-Zn-O-based material in FIG. 17A, in the order starting from the top, a Sn atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half is bonded to an In atom proximate to one tetracoordinate O atom in each of an upper half and a lower half, the In atom is bonded to a Zn atom proximate to three tetracoordinate O atoms in an upper half, the Zn atom is bonded to an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the Zn atom, the In atom is bonded to a small group that includes two Zn atoms and is proximate to one tetracoordinate O atom in an upper half, and the small group is bonded to a Sn atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the small group. A plurality of such medium groups are bonded,

so that a large group is formed.

[0148]

Here, electric charge for one bond of a tricoordinate O atom and electric charge for one bond of a tetracoordinate O atom can be assumed to be -0.667 and -0.5 , respectively. For example, electric charge of a (hexacoordinate or pentacoordinate) In atom, electric charge of a (tetracoordinate) Zn atom, and electric charge of a (pentacoordinate or hexacoordinate) Sn atom are $+3$, $+2$, and $+4$, respectively. Accordingly, electric charge in a small group including a Sn atom is $+1$. Therefore, electric charge of -1 , which cancels $+1$, is needed to form a layered structure including a Sn atom. As a structure having electric charge of -1 , the small group including two Zn atoms as illustrated in FIG. 16E can be given. For example, with one small group including two Zn atoms, electric charge of one small group including a Sn atom can be cancelled, so that the total electric charge of the layered structure can be 0.

[0149]

When the large group illustrated in FIG. 17B is repeated, an In-Sn-Zn-O-based crystal ($\text{In}_2\text{SnZn}_3\text{O}_8$) can be obtained. Note that a layered structure of the obtained In-Sn-Zn-O-based crystal can be expressed as a composition formula, $\text{In}_2\text{SnZn}_2\text{O}_7(\text{ZnO})_m$ (m is 0 or a natural number).

[0150]

The above-described rule also applies to the following oxides: oxide of four metal elements, such as In-Sn-Ga-Zn-based oxide; oxide of three metal elements, such as In-Ga-Zn-based oxide (also referred to as IGZO), In-Al-Zn-based oxide, Sn-Ga-Zn-based oxide, Al-Ga-Zn-based oxide, Sn-Al-Zn-based oxide, In-Hf-Zn-based oxide, In-La-Zn-based oxide, In-Ce-Zn-based oxide, In-Pr-Zn-based oxide, In-Nd-Zn-based oxide, In-Sm-Zn-based oxide, In-Eu-Zn-based oxide, In-Gd-Zn-based oxide, In-Tb-Zn-based oxide, In-Dy-Zn-based oxide, In-Ho-Zn-based oxide, In-Er-Zn-based oxide, In-Tm-Zn-based oxide, In-Yb-Zn-based oxide, and In-Lu-Zn-based oxide; oxide of two metal elements, such as In-Zn-based oxide, Sn-Zn-based oxide, Al-Zn-based oxide, Zn-Mg-based oxide, Sn-Mg-based oxide, In-Mg-based oxide, and In-Ga-based oxide.

[0151]

As an example, FIG. 18A illustrates a model of a medium group included in a layered structure of an In-Ga-Zn-O-based material.

[0152]

In the medium group included in the layered structure of the In-Ga-Zn-O-based material in FIG. 18A, in the order starting from the top, an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half is bonded to a Zn atom proximate to one tetracoordinate O atom in an upper half, the Zn atom is bonded to a Ga atom proximate to one tetracoordinate O atom in each of an upper half and a lower half through three tetracoordinate O atoms in a lower half with respect to the Zn atom, and the Ga atom is bonded to an In atom proximate to three tetracoordinate O atoms in each of an upper half and a lower half through one tetracoordinate O atom in a lower half with respect to the Ga atom. A plurality of such medium groups are bonded, so that a large group is formed.

[0153]

FIG. 18B illustrates a large group including three medium groups. FIG. 18C illustrates an atomic arrangement in the case where the layered structure in FIG. 18B is observed from the c-axis direction.

[0154]

Here, since electric charge of a (hexacoordinate or pentacoordinate) In atom, electric charge of a (tetracoordinate) Zn atom, and electric charge of a (pentacoordinate) Ga atom are +3, +2, +3, respectively, electric charge of a small group including any of an In atom, a Zn atom, and a Ga atom is 0. As a result, the total electric charge of a medium group having a combination of such small groups is always 0.

[0155]

In order to form the layered structure of the In-Ga-Zn-O-based material, a large group can be formed using not only the medium group illustrated in FIG. 18A but also a medium group in which the arrangement of the In atom, the Ga atom, and the Zn atom is different from that in FIG. 18A.

[0156]

As a target used for forming the oxide semiconductor film by sputtering, an oxide target containing In_2O_3 , Ga_2O_3 , and ZnO at a composition ratio of 1:1:1 [molar ratio] is used, for example, and an In-Ga-Zn-O film is formed. Without limitation to

the material and the composition of the above target, an oxide target containing In_2O_3 , Ga_2O_3 , and ZnO at a composition ratio of 1:1:2 [molar ratio] or a composition ratio of 1:1:4 [molar ratio] may be used, for example.

[0157]

5 The filling rate of the oxide target is 90 % to 100 %, preferably 95 % to 99.9 %. With use of the metal oxide target with high filling rate, a dense oxide semiconductor film can be formed. Moreover, the purity of the target is preferably higher than or equal to 99.99 %. In particular, it is preferable that impurities in the target, for example, an alkali metal such as Li or Na and an alkaline earth metal such as Ca be

10 reduced.

[0158]

It is preferable that a high-purity gas from which impurities such as hydrogen, water, hydroxyl group, or hydride have been removed be used as a sputtering gas used for forming the oxide semiconductor film. Specifically, a high-purity gas with a dew

15 point of $-60\text{ }^\circ\text{C}$ or lower is preferable.

[0159]

The substrate is held in a deposition chamber kept under reduced pressure, and the substrate temperature is set at $100\text{ }^\circ\text{C}$ to $600\text{ }^\circ\text{C}$, preferably $200\text{ }^\circ\text{C}$ to $400\text{ }^\circ\text{C}$. By forming the oxide semiconductor film while the substrate is heated, the concentration of

20 impurities included in the formed oxide semiconductor film can be reduced. In addition, damage by sputtering can be reduced. Then, a sputtering gas from which hydrogen and moisture have been removed is introduced into the deposition chamber while moisture remaining therein is removed, and the oxide semiconductor film is formed with the use of the above target.

25 [0160]

In order to remove moisture remaining in the deposition chamber, an entrapment vacuum pump such as a cryopump, an ion pump, or a titanium sublimation pump is preferably used. The evacuation unit may be a turbo pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a

30 hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O) (preferably, a compound containing a carbon atom as well), and the like are removed,

whereby the concentration of impurities in the oxide semiconductor film formed in the deposition chamber can be reduced.

[0161]

The atmosphere for sputtering may be a rare gas (typically argon) atmosphere,
5 an oxygen atmosphere, or a mixed atmosphere containing a rare gas and oxygen.

[0162]

As one example of the deposition conditions, the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct-current (DC) power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the proportion of the oxygen
10 flow rate is 100 %). Note that a pulsed direct-current (DC) power source is preferable because dust generated in deposition can be reduced and the film thickness can be made uniform.

[0163]

When the leakage rate of the treatment chamber of the sputtering apparatus is
15 set at 1×10^{-10} Pa·m³/s or less, entry of impurities such as an alkali metal or hydride into the oxide semiconductor film that is being deposited by sputtering can be reduced. Moreover, with the use of an entrapment vacuum pump as an exhaustion system, counter flow of impurities such as an alkali metal, a hydrogen atom, a hydrogen molecule, water, hydroxyl, or hydride from the exhaustion system can be reduced.

20 [0164]

Note that impurities, for example, an alkali metal such as Li or Na and an alkaline earth metal such as Ca included in the oxide semiconductor film are preferably reduced. Specifically, as for the concentrations of such impurities contained in the oxide semiconductor film measured by SIMS, the concentrations of Li and K are
25 preferably 5×10^{15} cm⁻³ or lower, further preferably 1×10^{15} cm⁻³ or lower.

[0165]

An alkali metal and an alkaline earth metal are adverse impurities for the oxide semiconductor and are preferably contained as little as possible. Specifically, when an insulating film in contact with the oxide semiconductor is an oxide, Na, among the
30 alkali metals, diffuses into the oxide and becomes Na⁺. In addition, Na cuts a bond between metal and oxygen or enters the bond in the oxide semiconductor, which causes

deterioration of transistor characteristics (e.g., normally-on state of the transistor (a negative shift of the threshold voltage) or the decrease in mobility) and variations in the characteristics. Such problems are significant especially in the case where the hydrogen concentration in the oxide semiconductor is extremely low. Therefore, the concentration of an alkali metal strongly needs to be the above value when the hydrogen concentration in the oxide semiconductor is $5 \times 10^{19} \text{ cm}^{-3}$ or lower, particularly $5 \times 10^{18} \text{ cm}^{-3}$ or lower.

[0166]

Next, the oxide semiconductor film is processed (patterned) into a desired shape by etching or the like, whereby an island-shaped oxide semiconductor layer 715 is formed over the gate insulating layer 714 so as to overlap with the gate electrode 713 (see FIG. 5B).

[0167]

A resist mask used for forming the island-shaped oxide semiconductor layer 715 may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, fabrication costs can be reduced.

[0168]

Note that etching for forming the island-shaped oxide semiconductor layer 715 may be wet etching, dry etching, or both dry etching and wet etching. As an etching gas for dry etching, a gas containing chlorine (a chlorine-based gas such as chlorine (Cl_2), boron trichloride (BCl_3), silicon tetrachloride (SiCl_4), or carbon tetrachloride (CCl_4)) is preferably used. Moreover, a gas containing fluorine (a fluorine-based gas such as carbon tetrafluoride (CF_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), or trifluoromethane (CHF_3)), hydrogen bromide (HBr), oxygen (O_2), any of these gases to which a rare gas such as helium (He) or argon (Ar) is added, or the like can be used.

[0169]

As the dry etching method, parallel plate RIE (reactive ion etching) or ICP (inductively coupled plasma) etching can be used. In order to etch the films into desired shapes, the etching conditions (e.g., the amount of power applied to a coil-shaped electrode, the amount of power applied to an electrode on the substrate side, and the temperature of the electrode on the substrate side) are adjusted as appropriate.

[0170]

As an etchant used for wet etching, a mixed solution of phosphoric acid, acetic acid, and nitric acid can be used, for example. In addition, ITO07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0171]

5 Next, the oxide semiconductor layer is subjected to first heat treatment. With the first heat treatment, dehydration or dehydrogenation of the oxide semiconductor layer can be conducted. The temperature of the first heat treatment is 150 °C to 650 °C, preferably 200 °C to 500 °C. For example, the first heat treatment may be performed at 500 °C for 3 to 6 minutes. When rapid thermal annealing (RTA) is used
10 for the heat treatment, dehydration or dehydrogenation can be performed in a short time; therefore, the treatment can be conducted even at a temperature higher than the strain point of the glass substrate.

[0172]

 Here, the substrate is put in an electric furnace which is one of heat treatment
15 apparatuses and heat treatment is performed on the oxide semiconductor layer at 450 °C for one hour in a nitrogen atmosphere. Then, water or hydrogen is prevented from entering the oxide semiconductor layer without exposure to the air; thus, the oxide semiconductor layer 715 is obtained.

[0173]

20 Note that a heat treatment apparatus is not limited to an electrical furnace and may be an apparatus for heating an object by heat conduction or heat radiation from a heating element such as a resistance heating element. For example, an RTA apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used. An LRTA apparatus is an apparatus for
25 heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the high-temperature gas, an inert gas which does not react with an object by heat treatment, for example,
30 nitrogen or a rare gas such as argon is used.

[0174]

Note that it is preferable that in the first heat treatment, moisture, hydrogen, or the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. The purity of nitrogen or the rare gas such as helium, neon, or argon which is introduced into a heat treatment apparatus is preferably 6N (99.9999 %) or higher, further preferably 7N (99.99999 %) or higher (i.e., the impurity concentration is preferably 1 ppm or lower, further preferably 0.1 ppm or lower).

[0175]

In addition, after the oxide semiconductor layer is heated by the first heat treatment, a high-purity oxygen gas, a high-purity N₂O gas, or ultra dry air (with a moisture content of 20 ppm (−55 °C by conversion into a dew point) or less, preferably 1 ppm or less, further preferably 10 ppb or less, in the case where measurement is performed with the use of a dew point meter of a cavity ring down laser spectroscopy (CRDS) system) may be introduced into the same furnace. It is preferable that water, hydrogen, and the like be not contained in the oxygen gas or the N₂O gas. Alternatively, the purity of the oxygen gas or the N₂O gas which is introduced into the heat treatment apparatus is preferably 6N or higher, further preferably 7N or higher (i.e., the impurity concentration of the oxygen gas or the N₂O gas is preferably 1 ppm or lower, more preferably 0.1 ppm or lower). Oxygen which is the main component of the oxide semiconductor and has been reduced at the same time as the step for removing impurities by dehydration or dehydrogenation is supplied by the effect of the oxygen gas or the N₂O gas, so that the oxide semiconductor layer can be a high-purity and electrically i-type (intrinsic) oxide semiconductor layer.

[0176]

In addition, the first heat treatment for the oxide semiconductor layer can be performed on the oxide semiconductor film which has not been processed into the island-shaped oxide semiconductor layer. In that case, the substrate is taken out from the heat apparatus after the first heat treatment, and then a photolithography process is performed.

[0177]

Note that the first heat treatment may be performed at either of the following timings without limitation to the above-described timing as long as it is performed after

the oxide semiconductor layer is formed: after a source electrode layer and a drain electrode layer are formed over the oxide semiconductor layer; and after an insulating layer is formed over the source electrode layer and the drain electrode layer.

[0178]

5 Through the above steps, the concentration of hydrogen in the island-shaped oxide semiconductor layer can be reduced. The above heat treatment can be performed at any time as long as it is performed after the oxide semiconductor layer is formed.

[0179]

10 Alternatively, an oxide semiconductor film having a crystal region that is c-axis-aligned perpendicularly to a surface of the film may be formed by performing two deposition steps and two heat treatments. For example, a first oxide semiconductor film with a thickness 3 nm to 15 nm is formed and then first heat treatment is performed at temperatures ranging from 450 °C to 850 °C, preferably from
15 550 °C to 750 °C in an atmosphere of nitrogen, oxygen, a rare gas, or dry air (e.g., an oxygen atmosphere, a nitrogen atmosphere, a mixed atmosphere of oxygen and argon, a mixed atmosphere of nitrogen and argon, or a mixed atmosphere of oxygen, nitrogen, and argon). Thus, the first oxide semiconductor film that has a crystal region (including plate-like crystals) in a region including its surface is formed. Then, a
20 second oxide semiconductor film that is thicker than the first oxide semiconductor film is formed and then second heat treatment is performed at temperatures ranging from 450 °C to 850 °C, preferably from 600 °C to 700 °C. Thus, crystal growth proceeds upward with the use of the first oxide semiconductor film as a seed of the crystal growth, and the entire second oxide semiconductor film is crystallized as a result. In such a
25 manner, an oxide semiconductor layer having a thick crystal region may be formed.

[0180]

 Moreover, an oxide semiconductor layer having a crystal region that is c-axis-aligned perpendicularly to a surface of the film may be formed by depositing an oxide semiconductor layer while the substrate is heated to a temperature at which the
30 oxide semiconductor is c-axis-aligned. With such a film formation method, the process can be shortened. The temperature for heating the substrate is set as

appropriate in accordance with other film formation conditions which differ depending on a film formation apparatus; for example, the substrate temperature during the film formation with a sputtering apparatus is set in the range of 150 °C to 450 °C.

[0181]

5 Next, the insulating film 708, the insulating film 712, and the gate insulating layer 714 are partly etched, whereby contact holes reaching the island-shaped semiconductor film 702, the island-shaped semiconductor film 703, and the wiring 711 are formed. Note that the contact holes may be formed before the first heat treatment is performed.

10 [0182]

 Then, a conductive film is formed so as to cover the oxide semiconductor layer 715 by sputtering or vacuum evaporation. After that, the conductive film is patterned by etching or the like, so that conductive films 716 to 721 each of which functions as a source electrode, a drain electrode, or a wiring are formed.

15 [0183]

 Note that the conductive films 716 and 717 are in contact with the island-shaped semiconductor film 702. The conductive films 718 and 719 are in contact with the island-shaped semiconductor film 703. The conductive film 720 is in contact with the wiring 711 and the oxide semiconductor layer 715. The conductive

20 film 721 is in contact with the oxide semiconductor layer 715.

[0184]

 As a material for the conductive film to be the conductive films 716 to 721, a metal film containing an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten, an alloy film or a metal nitride film containing any

25 of the above elements as its component (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film), or the like can be used. When a metal film of aluminum, copper, or the like is used, a film of a refractory metal such as molybdenum, titanium, chromium, tantalum, tungsten, neodymium, scandium, or yttrium or a metal nitride film thereof (e.g., a titanium nitride film, a molybdenum nitride film, or a

30 tungsten nitride film) may be provided in contact with the metal film in order to solve problems of heat resistance and corrosion.

[0185]

The conductive film may have a single-layer structure or a stacked structure including two or more layers. For example, the conductive film may have a single-layer structure of an aluminum film containing silicon; a two-layer structure of an aluminum film and a titanium film stacked thereover; or a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order.

[0186]

Alternatively, the conductive film may have a structure in which a copper film is stacked over an alloy film of copper, magnesium, and aluminum. By using the alloy film of copper, magnesium, and aluminum, the adhesion between the conductive film and the insulating film can be increased.

[0187]

The conductive film to be the conductive films 716 to 721 may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide, tin oxide, zinc oxide, indium tin oxide, indium zinc oxide, or the metal oxide material to which silicon or silicon oxide is added can be used.

[0188]

In the case where heat treatment is performed after formation of the conductive film, the conductive film preferably has heat resistance high enough to withstand the heat treatment.

[0189]

Note that the materials and etching conditions are adjusted as appropriate so that the oxide semiconductor layer 715 is not removed as much as possible in etching of the conductive film. Depending on etching conditions, an exposed portion of the oxide semiconductor layer 715 is partly etched and thus a groove (a recessed portion) is formed in some cases.

[0190]

In order to reduce the number of photomasks and steps in a photolithography process, etching may be performed with the use of a resist mask formed using a multi-tone mask which is a light-exposure mask through which light is transmitted so as to have a plurality of intensities. A resist mask formed with the use of a multi-tone mask has a plurality of thicknesses and further can be changed in shape by etching; therefore, the resist mask can be used in a plurality of etching steps for processing films

into different patterns. That is, a resist mask corresponding to at least two kinds of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also reduced, whereby the process can be simplified.

5 [0191]

Next, plasma treatment using a gas such as N_2O , N_2 , or Ar is performed. Through this plasma treatment, water or the like adsorbed on an exposed surface of the oxide semiconductor layer is removed. Plasma treatment may be performed using a mixture gas of oxygen and argon.

10 [0192]

After the plasma treatment, an insulating film 722 is formed so as to cover the conductive films 716 to 721 and the oxide semiconductor layer 715 (see FIG. 5C).

[0193]

The insulating film 722 preferably contains as little impurities such as moisture, hydrogen, and oxygen as possible. The insulating film 722 may be a single-layer insulating film or a stack of a plurality of insulating films. If hydrogen is contained in the insulating film 722, hydrogen might enter the oxide semiconductor layer or extract oxygen from the oxide semiconductor layer, thereby causing reduction in resistance of a back channel portion of the oxide semiconductor layer (making the back channel portion have n-type conductivity), which might result in formation of parasitic channel. Therefore, it is important that a film formation method in which hydrogen is not used be employed in order to form the insulating film 722 containing as little hydrogen as possible.

[0194]

25 A material with high barrier properties is preferably used for the insulating film 722. For example, as an insulating film with high barrier properties, a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, an aluminum nitride oxide film, an aluminum oxide film, a gallium oxide film, or the like can be used. By using the insulating film with high barrier properties, impurities such as moisture or hydrogen
30 can be prevented from entering the island-shaped oxide semiconductor layer, the gate insulating layer, or the interface between the island-shaped oxide semiconductor layer and another insulating layer and the vicinity thereof.

[0195]

For example, an insulating film having a structure in which a 100-nm-thick aluminum oxide film formed by sputtering is stacked over a 200-nm-thick gallium oxide film formed by sputtering may be formed. The substrate temperature at the time of deposition is in the range of room temperature to 300 °C. Further, the insulating film preferably contains much oxygen that exceeds the stoichiometric proportion, further preferably contains oxygen more than 1 time and less than two times the stoichiometric proportion. When the insulating film contains excessive oxygen in the above manner, oxygen is supplied to the interface with the island-shaped oxide semiconductor film; thus, oxygen vacancies can be reduced.

[0196]

After the insulating film 722 is formed, heat treatment may be performed. The heat treatment is performed at preferably 200 °C to 400 °C (e.g., 250 °C to 350 °C) in a nitrogen atmosphere, an atmosphere of ultra-dry air, or a rare gas (e.g., argon or helium) atmosphere. The water content in the gas is preferably 20 ppm or less, more preferably 1 ppm or less, further preferably 10 ppb or less. In this embodiment, for example, heat treatment is performed at 250 °C for one hour in a nitrogen atmosphere. Alternatively, RTA treatment for a short time at a high temperature may be performed before the formation of the conductive films 716 to 721, in a manner similar to that of the previous heat treatment performed on the oxide semiconductor film for reduction of moisture or hydrogen. Even when oxygen defects are generated in the oxide semiconductor layer 715 because of the previous heat treatment performed on the oxide semiconductor film, by performing heat treatment after the insulating film 722 containing oxygen is provided, oxygen is supplied to the oxide semiconductor layer 715 from the insulating film 722. By supplying oxygen to the oxide semiconductor layer 715, oxygen defects that serve as donors can be reduced in the oxide semiconductor layer 715 and the stoichiometric proportion can be satisfied. The oxide semiconductor layer 715 preferably contains much oxygen that exceeds the stoichiometric proportion. As a result, the oxide semiconductor layer 715 can be made to be substantially i-type and variation in electrical characteristics of the transistor due to oxygen vacancy can be reduced; thus, the electrical characteristics can be improved. There is no particular

limitation on the timing of this heat treatment as long as it is after the formation of the insulating film 722. When this heat treatment doubles as another step such as heat treatment for formation of a resin film or heat treatment for reduction of the resistance of a transparent conductive film, the oxide semiconductor layer 715 can be made to be substantially i-type without increase in the number of steps.

[0197]

Further, oxygen vacancies that serves as donors in the oxide semiconductor layer 715 may be reduced by performing heat treatment on the oxide semiconductor layer 715 in an oxygen atmosphere so that oxygen is added to the oxide semiconductor.

The heat treatment is performed at a temperature of, for example, higher than or equal to 100 °C and lower than 350 °C, preferably higher than or equal to 150 °C and lower than 250 °C. It is preferable that an oxygen gas used for the heat treatment under an oxygen atmosphere do not include water, hydrogen, or the like. The purity of oxygen gas which is introduced into a heat treatment apparatus is preferably 6N (99.9999 %) or higher, further preferably 7N (99.99999 %) or higher (i.e., the impurity concentration in the oxygen is preferably 1 ppm or lower, further preferably 0.1 ppm or lower).

[0198]

Alternatively, an ion implantation method, an ion doping method, or the like may be employed to add oxygen to the oxide semiconductor layer 715 so that oxygen vacancies serving as donors are reduced. For example, oxygen which is made into a plasma state with a microwave at 2.45 GHz may be added to the oxide semiconductor layer 715.

[0199]

Note that a backgate electrode may be formed in a position overlapping with the oxide semiconductor layer 715 by forming a conductive film over the insulating film 722 and patterning the conductive film. In the case where the backgate electrode is formed, an insulating film is preferably formed to cover the backgate electrode. The backgate electrode can be formed using a material and a structure similar to those of the gate electrode 713 or the conductive films 716 to 721.

[0200]

The thickness of the backgate electrode is 10 nm to 400 nm, preferably 100 nm

to 200 nm. For example, the backgate electrode may be formed in a such a manner that a conductive film in which a titanium film, an aluminum film, and a titanium film are stacked is formed, a resist mask is formed by photolithography or the like, and unnecessary portions are removed by etching so that the conductive film is processed
5 (patterned) into a desired shape.

[0201]

Through the above steps, the transistor 724 is formed.

[0202]

Note that there is no particular limitation on the structure of a transistor in the
10 present invention. FIGS. 6A to 6D illustrate other structure examples of transistors including an oxide semiconductor. Note that the same portions as the transistor 724 and portions having functions similar to those of the transistor 724 can be formed in the above manner, and steps same as or similar to those of the transistor 724 can be performed in the above manner; therefore, the description is not repeated in this
15 embodiment. In addition, the detailed description of the same portions is omitted.

[0203]

A transistor 620 illustrated in FIG. 6A is an example of a bottom-gate transistor in which a gate is formed below (on the substrate side in relation to) a semiconductor layer.

20 [0204]

The transistor 620 has a bottom-gate structure and includes a gate electrode layer 601, a gate insulating layer 602 over the gate electrode layer 601, a source electrode layer 605a and a drain electrode layer 605b which are a pair of electrode layers formed over the gate insulating layer 602, and an island-shaped oxide
25 semiconductor layer 603 that is in contact with the source electrode layer 605a, the drain electrode layer 605b, and the gate insulating layer 602 and overlaps with the gate electrode layer 601.

[0205]

A transistor 630 illustrated in FIG. 6B has an example of a bottom-gate
30 structure in which a channel protective layer is provided on the backchannel side in relation to an oxide semiconductor layer (the side opposite to a gate electrode). With the channel protective layer, damage to the oxide semiconductor layer at the time of

etching a source electrode and a drain electrode can be suppressed.

[0206]

The transistor 630 has a channel protective bottom-gate structure and includes a gate electrode layer 601, a gate insulating layer 602 over the gate electrode layer 601, an island-shaped oxide semiconductor layer 603 that overlaps the gate electrode layer 601 with the gate insulating layer 602 placed therebetween, a channel protective layer 627 that is in contact with the oxide semiconductor layer 603 and overlaps with a region of the oxide semiconductor layer 603 where a channel is formed, and a source electrode layer 605a and a drain electrode layer 605b which are a pair of electrode layers formed over the oxide semiconductor layer 603.

[0207]

A transistor 640 illustrated in FIG. 6C is an example of a top-gate transistor.

[0208]

The transistor 640 is a top-gate transistor including a base insulating layer 637, an island-shaped oxide semiconductor layer 603 over the base insulating layer 637, a source electrode layer 605a and a drain electrode layer 605b which are a pair of electrode layers in contact with the oxide semiconductor layer 603, a gate insulating layer 602 that is in contact with a channel formation region in the oxide semiconductor layer 603 between the source electrode layer 605a and the drain electrode layer 605b, and a gate electrode layer 601 that is over the gate insulating layer 602 and overlaps with the channel formation region in the oxide semiconductor layer 603.

[0209]

Note that the transistor 640 may include a source wiring layer 636a and a drain wiring layer 636b that are connected to the source electrode layer 605a and the drain electrode layer 605b, respectively, through contact holes formed in the gate insulating layer 602.

[0210]

A transistor 650 illustrated in FIG. 6D is an example of a top-gate transistor having a structure different from that of the transistor 640.

[0211]

The transistor 650 is a top-gate transistor including a base insulating layer 637; a source electrode layer 605a and a drain electrode layer 605b which are a pair of

electrode layers over the base insulating layer 637; an oxide semiconductor layer 603 that fills a gap between the source electrode layer 605a and the drain electrode layer 605b; a gate insulating layer 602 over the source electrode layer 605a, the drain electrode layer 605b, and the oxide semiconductor layer 603; and a gate electrode layer 601 that is over the gate insulating layer 602 and overlaps with a region of the oxide semiconductor layer 603 where a channel is formed.

[0212]

Note that like the transistor 640, the transistor 650 may include a source wiring layer and a drain wiring layer that are connected to the source electrode layer 605a and the drain electrode layer 605b, respectively, through contact holes formed in the gate insulating layer 602.

[0213]

Although not illustrated, in a top-gate transistor such as the transistor 640 or the transistor 650, a second gate electrode layer (also referred to as a backgate electrode layer) may be formed between the substrate and the base insulating layer so as to overlap with the channel formation region in the oxide semiconductor layer 603. In this case, one of the two gate electrode layers may be referred to as a first gate electrode layer and the other may be referred to as a backgate electrode. The first gate electrode layer and the backgate electrode layer can be electrically connected to each other so as to function as one electrode.

[0214]

By changing the potential of the backgate electrode layer, the threshold voltage of the transistor can be changed. The backgate electrode layer may be in a floating state (i.e., electrically insulated), or may be supplied with a potential or a fixed potential such as a ground potential or a common potential. By controlling the level of a potential applied to the backgate electrode layer, the threshold voltage of the transistor can be controlled.

[0215]

In a top-gate structure, when the oxide semiconductor layer 603 is covered with the backgate electrode layer, light from the backgate electrode layer side can be prevented from entering the oxide semiconductor layer 603. Thus, photodegradation of the oxide semiconductor layer 603 can be prevented, and deterioration in

characteristics of the transistor, such as a shift of the threshold voltage, can be prevented.

[0216]

Note that an insulating film to be the insulating layer in contact with the oxide semiconductor layer 603 (which corresponds to the gate insulating layer 602, the insulating layer 607, the channel protective layer 627, and the base insulating layer 637 in this embodiment) is preferably formed using an insulating material containing a Group 13 element and oxygen. Many of oxide insulating materials contain elements of Group 13, and an insulating material containing a Group 13 element is compatible with an oxide semiconductor layer. Consequently, when an insulating material containing a Group 13 element is used for the insulating layer in contact with the oxide semiconductor layer, the state of the interface between the oxide semiconductor layer and the insulating layer can be kept favorable.

[0217]

An insulating material containing a Group 13 element refers to an insulating material containing one or plural kinds of Group 13 elements. Examples of the insulating material containing a Group 13 element are gallium oxide, aluminum oxide, aluminum gallium oxide, and gallium aluminum oxide. Here, aluminum gallium oxide refers to a material in which the aluminum content is higher than that the gallium content in atomic percent (at.%), and gallium aluminum oxide refers to a material in which the gallium content is higher than the aluminum content in atomic percent (at.%).

[0218]

For example, when a material containing gallium oxide is used for the insulating layer that is in contact with an oxide semiconductor layer containing gallium, characteristics at the interface between the oxide semiconductor layer and the insulating layer can be kept favorable. For example, when the oxide semiconductor layer and an insulating layer containing gallium oxide are provided in contact with each other, pile up of hydrogen at the interface between the oxide semiconductor layer and the insulating layer can be reduced. Note that a similar effect can be obtained in the case where an element in the same group as a constituent element of the oxide semiconductor layer is used for the insulating layer. For example, it is effective to form an insulating

layer with the use of a material containing aluminum oxide. Note that water is not likely to permeate an aluminum oxide; therefore, it is preferable to use a material containing aluminum oxide in terms of preventing entry of water to the oxide semiconductor layer.

5 [0219]

The insulating layer in contact with the oxide semiconductor layer 603 is preferably made to contain oxygen in a proportion higher than that in the stoichiometric composition by heat treatment in an oxygen atmosphere or by oxygen doping. Oxygen doping refers to addition of oxygen into a bulk. Note that the term "bulk" is used in
10 order to clarify that oxygen is added not only to a surface of a thin film but also to the inside of the thin film. In addition, "oxygen doping" includes oxygen plasma doping by which oxygen plasma is added to a bulk. The oxygen doping may be performed by an ion implantation method or an ion doping method.

[0220]

15 For example, in the case where an insulating film containing gallium oxide is used for the insulating layer in contact with the oxide semiconductor layer 603, the composition of gallium oxide can be set to be Ga_2O_x ($x = 3 + \alpha$, where $0 < \alpha < 1$) by heat treatment in an oxygen atmosphere or by oxygen doping.

[0221]

20 In the case where an insulating film containing aluminum oxide is used for the insulating layer in contact with the oxide semiconductor layer 603, the composition of aluminum oxide can be set to be Al_2O_x ($x = 3 + \alpha$, where $0 < \alpha < 1$) by heat treatment in an oxygen atmosphere or by oxygen doping.

[0222]

25 For example, in the case where an insulating film containing gallium aluminum oxide (aluminum gallium oxide) is used for the insulating layer in contact with the oxide semiconductor layer 603, the composition of gallium aluminum oxide (aluminum gallium oxide) can be set to be $\text{Ga}_x\text{Al}_{2-x}\text{O}_{3+\alpha}$ ($0 < x < 2$, $0 < \alpha < 1$) by heat treatment in an oxygen atmosphere or by oxygen doping.

30 [0223]

By oxygen doping, an insulating film that includes a region where the

proportion of oxygen is higher than that in the stoichiometric composition can be formed. When the insulating layer including such a region is in contact with the oxide semiconductor layer, oxygen that exists excessively in the insulating layer is supplied to the oxide semiconductor layer, and oxygen vacancies in the oxide semiconductor layer or at the interface between the oxide semiconductor layer and the insulating layer are reduced. Thus, the oxide semiconductor layer can be an i-type or substantially i-type oxide semiconductor.

[0224]

The insulating layer including a region where the proportion of oxygen is higher than that in the stoichiometric composition may be used as either the insulating layer placed above the oxide semiconductor layer 603 or the insulating layer placed below the oxide semiconductor layer 603 of the insulating layers in contact with the oxide semiconductor layer 603; it is preferably used as both of the insulating layers in contact with the oxide semiconductor layer 603. The above-described effect can be enhanced with a structure where the insulating layers that include a region where the proportion of oxygen is higher than that in the stoichiometric composition are used as insulating layers placed above and below the insulating layers in contact with the oxide semiconductor layer 603 so that the oxide semiconductor layer 603 is sandwiched therebetween.

[0225]

The insulating layers placed above and below the oxide semiconductor layer 603 may contain the same constituent element or different constituent elements. For example, both of the insulating layers placed above and below the oxide semiconductor layer 603 may be formed using gallium oxide whose composition is Ga_2O_x ($x = 3 + \alpha$, where $0 < \alpha < 1$). Alternatively, one of these insulating layers may be formed using gallium oxide whose composition is Ga_2O_x ($x = 3 + \alpha$, where $0 < \alpha < 1$) and the other thereof may be formed using aluminum oxide whose composition is Al_2O_x ($x = 3 + \alpha$, where $0 < \alpha < 1$).

[0226]

The insulating layer in contact with the oxide semiconductor layer 603 may be a stack of insulating films each of which includes a region where the proportion of

oxygen is higher than that in the stoichiometric composition. For example, the insulating layer placed above the oxide semiconductor layer 603 may be formed as follows: gallium oxide whose composition is Ga_2O_x ($x = 3 + \alpha$, where $0 < \alpha < 1$) is formed and gallium aluminum oxide (aluminum gallium oxide) whose composition is $\text{Ga}_x\text{Al}_{2-x}\text{O}_{3+\alpha}$ ($0 < x < 2$, $0 < \alpha < 1$) is formed thereover. Note that it is possible that the insulating layer placed below the oxide semiconductor layer 603, or both of the insulating layers placed above and below the oxide semiconductor layer 603 may be a stack of insulating films each of which includes a region where the proportion of oxygen is higher than that in the stoichiometric composition.

10 [0227]

Any of the above transistors can have an extremely low off-state current. With the use of such a transistor, the photosensor to which one embodiment of the present invention can be applied can be fabricated. Further, by using the photosensor to which one embodiment of the present invention is applied, a solid-state imaging device and a semiconductor display device with low power consumption can be provided.

15 [0228]

This embodiment can be implemented in combination with any of the other embodiments as appropriate.

20 [0229]

(Embodiment 3)

The actually measured field-effect mobility of an insulated gate transistor can be lower than its original mobility because of a variety of reasons; this phenomenon occurs not only in the case of using a transistor whose channel is formed in an oxide semiconductor layer. One of the reasons that reduce the mobility is a defect inside a semiconductor or a defect at an interface between the semiconductor and an insulating film. When a Levinson model is used, the field-effect mobility that is based on the assumption that no defect exists inside the semiconductor can be calculated theoretically.

25 [0230]

Assuming that the original mobility of a semiconductor is μ_0 and a potential

barrier (such as a grain boundary) exists in the semiconductor, the measured field-effect mobility μ can be expressed as the following Formula 2.

[0231]

[Formula 2]

$$5 \quad \mu = \mu_0 \exp\left(-\frac{E}{kT}\right)$$

[0232]

In Formula 2, E represents the height of the potential barrier, k represents the Boltzmann constant, and T represents the absolute temperature. When the potential barrier is assumed to be attributed to a defect, the height E of the potential barrier is expressed as the following Formula 3 according to the Levinson model.

[0233]

[Formula 3]

$$E = \frac{e^2 N^2}{8\epsilon n} = \frac{e^3 N^2 t}{8\epsilon C_{ox} V_g}$$

[0234]

In Formula 3, e represents the elementary charge, N represents the average defect density per unit area in a channel, ϵ represents the permittivity of the semiconductor, n represents the number of carriers per unit area in the channel, C_{ox} represents the capacitance per unit area, V_g represents the gate voltage, and t represents the thickness of the channel. Note that in the case where the thickness of the semiconductor layer is less than or equal to 30 nm, the thickness of the channel may be regarded as being the same as the thickness of the semiconductor layer. The drain current I_d in a linear region is expressed as the following Formula 4.

[0235]

[Formula 4]

$$25 \quad I_d = \frac{W \mu V_g V_d C_{ox}}{L} \exp\left(-\frac{E}{kT}\right)$$

[0236]

In Formula 4, L represents the channel length and W represents the channel width, and L and W are each 10 μm . In addition, V_d represents the drain voltage.

When dividing both sides of Formula 4 by V_g and then taking logarithms of both sides, the following Formula 5 is obtained.

[0237]

[Formula 5]

$$5 \quad \ln\left(\frac{I_d}{V_g}\right) = \ln\left(\frac{W \mu V_d C_{ox}}{L}\right) - \frac{E}{kT} = \ln\left(\frac{W \mu V_d C_{ox}}{L}\right) - \frac{e^3 N^2 t}{8kT \varepsilon C_{ox} V_g}$$

[0238]

The right side of Formula 5 is a function of V_g . From Formula 5, it is found that the defect density N can be obtained from the slope of a line in a graph that is obtained by plotting actual measured values with $\ln(I_d/V_g)$ as the ordinate and $1/V_g$ as the abscissa. That is, the defect density can be evaluated from the I_d - V_g characteristics of the transistor. The defect density N of an oxide semiconductor in which the ratio of indium (In), tin (Sn), and zinc (Zn) is 1:1:1 is approximately $1 \times 10^{12} / \text{cm}^2$.

[0239]

On the basis of the defect density obtained in this manner, μ_0 can be calculated to be $120 \text{ cm}^2/\text{Vs}$ from Formula 2 and Formula 3. The measured mobility of an In-Sn-Zn oxide including a defect is approximately $40 \text{ cm}^2/\text{Vs}$. However, assuming that no defect exists inside an oxide semiconductor and at the interface between the oxide semiconductor and an insulating film, the mobility μ_0 of the oxide semiconductor is expected to be $120 \text{ cm}^2/\text{Vs}$.

20 [0240]

Note that even when no defect exists inside a semiconductor, scattering at an interface between a channel and a gate insulating layer adversely affects the transport properties of the transistor. In other words, the mobility μ_1 at a position that is distance x away from the interface between the channel and the gate insulating layer can be expressed as the following Formula 6.

[0241]

[Formula 6]

$$\frac{1}{\mu_1} = \frac{1}{\mu_0} + \frac{D}{B} \exp\left(-\frac{x}{G}\right)$$

[0242]

In Formula 6, D represents the electric field in the gate direction, and B and G are constants. B and G can be obtained from actual measurement results; according to the above measurement results, B is 4.75×10^7 (cm/s) and G is 10 (nm) (the depth to which the influence of interface scattering reaches). When D is increased (i.e., when the gate voltage is increased), the second term of Formula 6 is increased and accordingly the mobility μ_1 is decreased.

[0243]

FIG. 19 shows calculation results of the mobility μ_2 of a transistor whose channel is formed using an ideal oxide semiconductor without a defect inside the semiconductor. In FIG. 19, the horizontal axis indicates gate voltage V_G (unit: V) and the vertical axis indicates mobility μ_2 (unit: cm^2/Vs). For the calculation, device simulation software Sentaurus Device manufactured by Synopsys, Inc. was used, and the band gap, the electron affinity, the relative permittivity, and the thickness of the oxide semiconductor were assumed to be 2.8 eV, 4.7 eV, 15, and 15 nm, respectively. These values were obtained by measurement of a thin film that was formed by sputtering.

[0244]

Further, the work functions of a gate, a source, and a drain were assumed to be 5.5 eV, 4.6 eV, and 4.6 eV, respectively. The thickness of a gate insulating layer was assumed to be 100 nm, and the relative permittivity thereof was assumed to be 4.1. The channel length and the channel width were each assumed to be 10 μm , and the drain voltage V_d was assumed to be 0.1 V.

[0245]

As shown in FIG. 19, the mobility μ_2 has a peak of more than 100 cm^2/Vs at a gate voltage V_G of slightly over 1 V, and is decreased as the gate voltage becomes higher because the influence of interface scattering is increased. Note that in order to reduce interface scattering, it is preferable that a surface of the semiconductor layer be flat at the atomic level (atomic layer flatness).

[0246]

Calculation results of characteristics of minute transistors formed using an

oxide semiconductor having such a mobility are shown in FIGS. 20A to 20C, FIGS. 21A to 21C, and FIGS. 22A to 22C. FIGS. 23A and 23B illustrate cross-sectional structures of the transistors used for the calculation. The transistors illustrated in FIGS. 23A and 23B each include a semiconductor region 1030a and a semiconductor region 1030c that have n⁺-type conductivity in an oxide semiconductor layer. The resistivity of the semiconductor regions 1030a and 1030c is $2 \times 10^{-3} \Omega\text{cm}$.

[0247]

The transistor in FIG. 23A is formed over a base insulating layer 1010 and an embedded insulator 1020 that is embedded in the base insulating layer 1010 and formed of aluminum oxide. The transistor includes the semiconductor region 1030a, the semiconductor region 1030c, an intrinsic semiconductor region 1030b that is placed between the semiconductor regions 1030a and 1030c and serves as a channel formation region, and a gate 1050. The width of the gate 1050 is 33 nm.

[0248]

A gate insulating layer 1040 is formed between the gate 1050 and the semiconductor region 1030b. A sidewall insulator 1060a and a sidewall insulator 1060b are formed on both side surfaces of the gate 1050, and an insulator 1070 is formed over the gate 1050 so as to prevent a short circuit between the gate 1050 and another wiring. The sidewall insulator has a width of 5 nm. A source 1080a and a drain 1080b are provided in contact with the semiconductor region 1030a and the semiconductor region 1030c, respectively. Note that the channel width of this transistor is 40 nm.

[0249]

The transistor in FIG. 23B is the same as the transistor in FIG. 23A in that it is formed over the base insulating layer 1010 and the embedded insulator 1020 formed of aluminum oxide and that it includes the semiconductor region 1030a, the semiconductor region 1030c, the intrinsic semiconductor region 1030b provided therebetween, the gate 1050 having a width of 33 nm, the gate insulating layer 1040, the sidewall insulator 1060a, the sidewall insulator 1060b, the insulator 1070, the source 1080a, and the drain 1080b.

[0250]

The difference between the transistor in FIG. 23A and the transistor in FIG. 23B is the conductivity type of semiconductor regions under the sidewall insulators 1060a and 1060b. In the transistor in FIG. 23A, the semiconductor regions under the sidewall insulator 1060a and the sidewall insulator 1060b are part of the semiconductor region 1030a having n⁺-type conductivity and part of the semiconductor region 1030c having n⁺-type conductivity, whereas in the transistor in FIG. 23B, the semiconductor regions under the sidewall insulator 1060a and the sidewall insulator 1060b are part of the intrinsic semiconductor region 1030b. In other words, in FIG. 23B, there is a region with a width L_{off} , in which the gate 1050 does not overlap with the semiconductor region 1030a (the semiconductor region 1030c). This region is called an offset region, and the width L_{off} is called an offset length. As is seen from the drawing, the offset length is equal to the width of the sidewall insulator 1060a (the sidewall insulator 1060b).

[0251]

The other parameters used in calculation are as described above. For the calculation, device simulation software Sentaurus Device manufactured by Synopsys, Inc. was used. FIGS. 20A to 20C show the gate voltage (V_g : a potential difference between the gate and the source) dependence of the drain current (I_d , a solid line) and the mobility (μ , a dotted line) of the transistor having the structure illustrated in FIG. 23A. The drain current I_d is obtained by calculation under the assumption that the drain voltage (a potential difference between the drain and the source) is +1 V, and the mobility μ is obtained by calculation under the assumption that the drain voltage is +0.1 V. In FIGS. 20A to 20C, the horizontal axis indicates gate voltage V_g (unit: V) and the vertical axis indicates drain current I_d (unit: A) and mobility μ (unit: cm²/Vs).

[0252]

FIG. 20A shows the gate voltage dependence of the transistor in the case where the thickness t of the gate insulating layer is 15 nm, FIG. 20B shows that of the transistor in the case where the thickness t of the gate insulating layer is 10 nm, and FIG. 20C shows that of the transistor in the case where the thickness t of the gate insulating layer is 5 nm. As the gate insulating layer is thinner, the drain current I_d in the off state (the off-state current) in particular is significantly decreased. In contrast, there is no

noticeable change in the peak value of the mobility μ and the drain current I_d in the on state (the on-state current). The graphs show that the drain current I_d exceeds 10 μA at a gate voltage V_g of around 1 V.

[0253]

5 FIGS. 21A to 21C show the gate voltage V_g dependence of the drain current I_d (a solid line) and the mobility μ (a dotted line) of the transistor having the structure in FIG. 23B and an offset length L_{off} of 5 nm. The drain current I_d is obtained by calculation under the assumption that the drain voltage is +1 V and the mobility μ is obtained by calculation under the assumption that the drain voltage is +0.1 V. FIG. 10 21A shows the gate voltage dependence of the transistor in the case where the thickness t of the gate insulating layer is 15 nm, FIG. 21B shows that of the transistor in the case where the thickness t of the gate insulating layer is 10 nm, and FIG. 21C shows that of the transistor in the case where the thickness t of the gate insulating layer is 5 nm. In FIGS. 21A to 21C, the horizontal axis indicates gate voltage V_g (unit: V) and the vertical 15 axis indicates drain current I_d (unit: A) and mobility μ (unit: cm^2/Vs).

[0254]

 FIGS. 22A to 22C show the gate voltage dependence of the drain current I_d (a solid line) and the mobility μ (a dotted line) of the transistor having the structure in FIG. 23B and an offset length L_{off} of 15 nm. The drain current I_d is obtained by calculation 20 under the assumption that the drain voltage is +1 V and the mobility μ is obtained by calculation under the assumption that the drain voltage is +0.1 V. FIG. 22A shows the gate voltage dependence of the transistor in the case where the thickness t of the gate insulating layer is 15 nm, FIG. 22B shows that of the transistor in the case where the thickness t of the gate insulating layer is 10 nm, and FIG. 22C shows that of the 25 transistor in the case where the thickness t of the gate insulating layer is 5 nm. In FIGS. 22A to 22C, the horizontal axis indicates gate voltage V_g (unit: V) and the vertical axis indicates drain current I_d (unit: A) and mobility μ (unit: cm^2/Vs).

[0255]

 In either of the structures, as the gate insulating layer is thinner, the off-state 30 current is significantly decreased, whereas no noticeable change arises in the peak value of the mobility μ and the on-state current.

[0256]

Note that the peak of the mobility μ is approximately $80 \text{ cm}^2/\text{Vs}$ in FIGS. 20A to 20C, approximately $60 \text{ cm}^2/\text{Vs}$ in FIGS. 21A to 21C, and approximately $40 \text{ cm}^2/\text{Vs}$ in FIGS. 22A to 22C; thus, the peak of the mobility μ is decreased as the offset length L_{off} is increased. Further, the same applies to the off-state current. The on-state current is also decreased as the offset length L_{off} is increased; however, the decrease in the on-state current is much more gradual than the decrease in the off-state current. Further, the graphs show that in either of the structures, the drain current I_d exceeds $10 \text{ }\mu\text{A}$ at a gate voltage V_g of around 1 V .

[0257]

A transistor in which an oxide semiconductor including In, Sn, and Zn as main components is used for a channel formation region can have favorable characteristics by depositing the oxide semiconductor while heating a substrate or by performing heat treatment after the oxide semiconductor film is formed. Note that a main component refers to an element included in a composition at 5 atomic% or more.

[0258]

By intentionally heating the substrate after formation of the oxide semiconductor film including In, Sn, and Zn as main components, the field-effect mobility of the transistor can be improved. Further, the threshold voltage of the transistor can be positively shifted to make the transistor normally off.

[0259]

As an example, FIGS. 24A to 24C each show characteristics (gate voltage dependence of drain current I_D (a solid line) and mobility μ_{FE} (a dotted line)) of a transistor that includes an oxide semiconductor film including In, Sn, and Zn as main components and having a channel length L of $3 \text{ }\mu\text{m}$ and a channel width W of $10 \text{ }\mu\text{m}$, and a gate insulating film with a thickness of 100 nm . Note that V_D was set to 10 V . In FIGS. 24A to 24C, the horizontal axis indicates gate voltage V_G (unit: V) and the vertical axis indicates drain current I_D (unit: A) and mobility μ_{FE} (unit: cm^2/Vs).

[0260]

FIG. 24A shows characteristics of a transistor whose oxide semiconductor film including In, Sn, and Zn as main components was formed by sputtering without heating

a substrate intentionally. The peak of the field-effect mobility of the transistor is 18.8 cm^2/Vs . On the other hand, when the oxide semiconductor film including In, Sn, and Zn as main components is formed while heating the substrate intentionally, the field-effect mobility can be improved. FIG. 24B shows characteristics of a transistor
5 whose oxide semiconductor film including In, Sn, and Zn as main components was formed while heating a substrate at 200 °C. The peak of the field-effect mobility of the transistor is 32.2 cm^2/Vs .

[0261]

The field-effect mobility can be further improved by performing heat treatment
10 after formation of the oxide semiconductor film including In, Sn, and Zn as main components. FIG. 24C shows characteristics of a transistor whose oxide semiconductor film including In, Sn, and Zn as main components was formed by sputtering at 200 °C and then subjected to heat treatment at 650 °C. The peak of the field-effect mobility of the transistor is 34.5 cm^2/Vs .

15 [0262]

The intentional heating of the substrate is expected to have an effect of reducing moisture taken into the oxide semiconductor film during the formation by sputtering. Further, the heat treatment after film formation enables hydrogen, a hydroxyl group, or moisture to be released and removed from the oxide semiconductor
20 film. In this manner, the field-effect mobility can be improved. Such an improvement in field-effect mobility is presumed to be achieved not only by removal of impurities by dehydration or dehydrogenation but also by a reduction in interatomic distance due to an increase in density. In addition, the oxide semiconductor can be crystallized by being purified by removal of impurities from the oxide semiconductor.
25 In the case of using such a purified non-single-crystal oxide semiconductor, ideally, a field-effect mobility exceeding 100 cm^2/Vs is expected to be realized.

[0263]

The oxide semiconductor including In, Sn, and Zn as main components may be crystallized in the following manner: oxygen ions are implanted into the oxide
30 semiconductor, hydrogen, a hydroxyl group, or moisture included in the oxide semiconductor is released by heat treatment, and the oxide semiconductor is crystallized

through the heat treatment or by another heat treatment performed later. By such crystallization treatment or recrystallization treatment, a non-single-crystal oxide semiconductor having favorable crystallinity can be obtained.

[0264]

5 The intentional heating of the substrate during film formation and/or the heat treatment after the film formation contributes not only to improving field-effect mobility but also to making the transistor normally off. In a transistor in which an oxide semiconductor film that includes In, Sn, and Zn as main components and is formed without heating a substrate intentionally is used as a channel formation region,
10 the threshold voltage tends to be shifted negatively. In contrast, when the oxide semiconductor film formed while heating the substrate intentionally is used, the problem of the negative shift of the threshold voltage can be solved. That is, the threshold voltage is shifted so that the transistor becomes normally off; this tendency can be confirmed by comparison between FIGS. 24A and 24B.

15 [0265]

Note that the threshold voltage can also be controlled by changing the ratio of In, Sn, and Zn; when the composition ratio of In, Sn, and Zn is 2:1:3, a normally-off transistor is expected to be formed. In addition, an oxide semiconductor film having high crystallinity can be obtained by setting the composition ratio of a target as follows:

20 In:Sn:Zn = 2:1:3.

[0266]

The temperature of the intentional heating of the substrate or the temperature of the heat treatment is 150 °C or higher, preferably 200 °C or higher, further preferably 400 °C or higher. When film formation or heat treatment is performed at a high
25 temperature, the transistor can be normally off.

[0267]

By intentionally heating the substrate during film formation and/or by performing heat treatment after the film formation, the stability against a gate-bias stress can be increased. For example, when a gate bias is applied with an intensity of 2
30 MV/cm at 150 °C for one hour, drift of the threshold voltage can be less than ± 1.5 V, preferably less than ± 1.0 V.

[0268]

A BT test was performed on the following two transistors: Sample 1 on which heat treatment was not performed after formation of an oxide semiconductor film, and Sample 2 on which heat treatment at 650 °C was performed after formation of an oxide semiconductor film.

[0269]

First, V_g - I_d characteristics of the transistors were measured at a substrate temperature of 25 °C and a drain voltage V_{ds} of 10 V. Then, the substrate temperature was set to 150 °C and V_{ds} was set to 0.1 V. After that, V_g of 20 V was applied so that the intensity of an electric field applied to the gate insulating layer was 2 MV/cm, and the condition was kept for one hour. Next, V_g was set to 0 V. Then, V_g - I_d characteristics of the transistors were measured at a substrate temperature of 25 °C and V_{ds} of 10 V. This process is called a positive BT test.

[0270]

In a similar manner, first, V_g - I_d characteristics of the transistors were measured at a substrate temperature of 25 °C and V_{ds} of 10 V. Then, the substrate temperature was set at 150 °C and V_{ds} was set to 0.1 V. After that, V_g of -20 V was applied so that the intensity of an electric field applied to the gate insulating layer was -2 MV/cm, and the condition was kept for one hour. Next, V_g was set to 0 V. Then, V_g - I_d characteristics of the transistors were measured at a substrate temperature of 25 °C and V_{ds} of 10 V. This process is called a negative BT test.

[0271]

FIGS. 25A and 25B show results of the positive BT test and the negative BT test, respectively, of Sample 1. FIGS. 26A and 26B show results of the positive BT test and the negative BT test, respectively, of Sample 2. In FIGS. 25A and 25B and FIGS. 26A and 26B, the horizontal axis indicates gate voltage V_g (unit: V) and the vertical axis indicates drain current I_d (unit: A).

[0272]

The amount of shift in the threshold voltage of Sample 1 due to the positive BT test and that due to the negative BT test were 1.80 V and 0.42 V, respectively. The amount of shift in the threshold voltage of Sample 2 due to the positive BT test and that

due to the negative BT test were 0.79 V and 0.76 V, respectively. It is found that, in each of Sample 1 and Sample 2, the amount of shift in the threshold voltage between before and after the BT tests is small and the reliability is high.

[0273]

5 The heat treatment can be performed in an oxygen atmosphere; alternatively, the heat treatment may be performed first in an atmosphere of nitrogen or an inert gas or under reduced pressure, and then in an atmosphere including oxygen. Oxygen is supplied to the oxide semiconductor after dehydration or dehydrogenation, whereby the effect of the heat treatment can be further increased. As a method for supplying
10 oxygen after dehydration or dehydrogenation, a method in which oxygen ions are accelerated by an electric field and implanted into the oxide semiconductor film may be employed.

[0274]

 A defect due to oxygen vacancy is easily caused in the oxide semiconductor or
15 at an interface between the oxide semiconductor and a film in contact with the oxide semiconductor; when excess oxygen is included in the oxide semiconductor by the heat treatment, oxygen vacancy caused constantly can be compensated for with excess oxygen. The excess oxygen is mainly oxygen existing between lattices. When the concentration of oxygen is set in the range of $1 \times 10^{16} / \text{cm}^3$ to $2 \times 10^{20} / \text{cm}^3$, excess
20 oxygen can be included in the oxide semiconductor without causing crystal distortion or the like.

[0275]

 When heat treatment is performed so that at least part of the oxide semiconductor includes crystal, a more stable oxide semiconductor film can be obtained.
25 For example, when an oxide semiconductor film that is formed by sputtering using a target having a composition ratio of In:Sn:Zn = 1:1:1 without heating a substrate intentionally is analyzed by X-ray diffraction (XRD), a halo pattern is observed. The formed oxide semiconductor film can be crystallized by being subjected to heat treatment. The temperature of the heat treatment can be set as appropriate; when the
30 heat treatment is performed at 650 °C, for example, a clear diffraction peak can be observed with X-ray diffraction.

[0276]

An XRD analysis of an In-Sn-Zn-O film was conducted. The XRD analysis was conducted using an X-ray diffractometer D8 ADVANCE manufactured by Bruker AXS, and measurement was performed by an out-of-plane method.

5 [0277]

Sample A and Sample B were prepared and the XRD analysis was performed thereon. A method for forming Sample A and Sample B will be described below.

[0278]

10 An In-Sn-Zn-O film with a thickness of 100 nm was formed over a quartz substrate that had been subjected to dehydrogenation treatment.

[0279]

The In-Sn-Zn-O film was formed with a sputtering apparatus with a power of 100 W (DC) in an oxygen atmosphere. An In-Sn-Zn-O target having an atomic ratio of In:Sn:Zn = 1:1:1 was used as a target. Note that the substrate heating temperature in
15 film formation was set at 200 °C. A sample formed in this manner was used as Sample A.

[0280]

Next, a sample formed by a method similar to that of Sample A was subjected to heat treatment at 650 °C. As the heat treatment, heat treatment in a nitrogen
20 atmosphere was first performed for one hour and heat treatment in an oxygen atmosphere was further performed for one hour without lowering the temperature. A sample formed in this manner was used as Sample B.

[0281]

FIG. 27 shows XRD spectra of Sample A and Sample B. No peak derived
25 from crystal was observed in Sample A, whereas peaks derived from crystal were observed when 2θ was around 35 deg. and at 37 deg. to 38 deg. in Sample B.

[0282]

As described above, by intentionally heating a substrate during deposition of an oxide semiconductor including In, Sn, and Zn as main components and/or by
30 performing heat treatment after the deposition, characteristics of a transistor can be improved.

[0283]

These substrate heating and heat treatment have an effect of preventing hydrogen and a hydroxyl group, which are unfavorable impurities for an oxide semiconductor, from being included in the film or an effect of removing hydrogen and a hydroxyl group from the film. That is, an oxide semiconductor can be purified by removing hydrogen serving as a donor impurity from the oxide semiconductor, whereby a normally-off transistor can be obtained. The high purification of an oxide semiconductor enables the off-state current of the transistor to be 1 aA/ μm or lower. Here, the unit of the off-state current represents current per micrometer of a channel width.

[0284]

Specifically, FIG. 28 shows a relation between the off-state current of a transistor and the inverse of substrate temperature (absolute temperature) at measurement. Here, for simplicity, the horizontal axis represents a value ($1000/T$) obtained by multiplying an inverse of substrate temperature at measurement by 1000. Moreover, the vertical axis in FIG. 28 indicates off-state current (unit: aA/ μm). As shown in FIG. 28, the off-state current of the transistor can be 1 aA/ μm (1×10^{-18} A/ μm) or lower, 100 zA/ μm (1×10^{-19} A/ μm) or lower, and 1 zA/ μm (1×10^{-21} A/ μm) or lower when the substrate temperature is 125 °C, 85 °C, and room temperature (27 °C), respectively. Preferably, the off-state current can be 0.1 aA/ μm (1×10^{-19} A/ μm) or lower, 10 zA/ μm (1×10^{-20} A/ μm) or lower, and 0.1 zA/ μm (1×10^{-22} A/ μm) or lower at 125 °C, 85 °C, and room temperature, respectively.

[0285]

Note that in order to prevent hydrogen and moisture from being included in the oxide semiconductor film during formation of the film, it is preferable to increase the purity of a sputtering gas by sufficiently suppressing leakage from the outside of a deposition chamber and degasification through an inner wall of the deposition chamber. For example, a gas with a dew point of -70 °C or lower is preferably used as the sputtering gas in order to prevent moisture from being included in the film. In addition, it is preferable to use a target that is highly purified so as not to include impurities such as hydrogen and moisture. Although it is possible to remove moisture from a film of

an oxide semiconductor including In, Sn, and Zn as main components by heat treatment, a film that does not include moisture originally is preferably formed because moisture is released from the oxide semiconductor including In, Sn, and Zn as main components at a higher temperature than from an oxide semiconductor including In, Ga, and Zn as main components.

[0286]

The relation between the substrate temperature and electric characteristics of the transistor of Sample B, on which heat treatment at 650 °C was performed after formation of the oxide semiconductor film, was evaluated.

[0287]

The transistor used for the measurement has a channel length L of 3 μm , a channel width W of 10 μm , L_{ov} of 0 μm , and dW of 0 μm . Note that V_{ds} was set to 10 V. Note that the substrate temperature was -40 °C, -25 °C, 25 °C, 75 °C, 125 °C, and 150 °C. Here, in the transistor, the width of a portion where a gate electrode overlaps with one of a pair of electrodes is referred to as L_{ov} , and the width of a portion of the pair of electrodes, which does not overlap with an oxide semiconductor film, is referred to as dW .

[0288]

FIG. 29 shows the V_g dependence of I_d (a solid line) and field-effect mobility (a dotted line). FIG. 30A shows a relation between the substrate temperature and the threshold voltage, and FIG. 30B shows a relation between the substrate temperature and the field-effect mobility.

[0289]

From FIG. 30A, it is found that the threshold voltage gets lower as the substrate temperature increases. Note that the threshold voltage is decreased from 0.38 V to 1.08 V in the range from -40 °C to 150 °C.

[0290]

From FIG. 30B, it is found that the field-effect mobility gets lower as the substrate temperature increases. Note that the field-effect mobility is decreased from 37.4 cm^2/Vs to 33.4 cm^2/Vs in the range from -40 °C to 150 °C. Thus, it is found that variation in electric characteristics is small in the above temperature range.

[0291]

In a transistor in which such an oxide semiconductor including In, Sn, and Zn as main components is used for a channel formation region, a field-effect mobility of 30 cm²/Vs or higher, preferably 40 cm²/Vs or higher, further preferably 60 cm²/Vs or higher can be obtained with the off-state current maintained at 1 aA/μm or lower, which can achieve on-state current needed for an LSI. For example, in an FET where L/W is 33 nm/40 nm, an on-state current of 12 μA or higher can flow when the gate voltage is 2.7 V and the drain voltage is 1.0 V. In addition, sufficient electric characteristics can be ensured in a temperature range needed for the operation of a transistor. With such characteristics, an integrated circuit having a novel function can be realized without decreasing the operation speed even when a transistor including an oxide semiconductor is provided in an integrated circuit formed using a Si semiconductor.

[0292]

This embodiment can be implemented in appropriate combination with the structures described in the other embodiments.

[0293]

(Embodiment 4)

In this embodiment, examples of electronic devices including the semiconductor device according to one embodiment of the present invention will be described with reference to FIGS. 7A to 7E.

[0294]

The semiconductor device according to one embodiment of the present invention can be used for display devices, laptops, and image reproducing devices provided with recording media (typically, devices that reproduce the content of recording media such as digital versatile discs (DVDs) and have displays for displaying the reproduced images). Other examples of electronic devices that can include the semiconductor device according to one embodiment of the present invention are mobile phones, portable game machines, personal digital assistants, e-book readers, video cameras, digital still cameras, goggle-type displays (head mounted displays), navigation systems, audio reproducing devices (e.g., car audio systems and digital audio players), copiers, facsimiles, printers, multifunction printers, automated teller machines (ATM),

and vending machines.

[0295]

FIG. 7A illustrates a display device including a housing 5001, a display portion 5002, a supporting base 5003, and the like. The semiconductor device according to one embodiment of the present invention can be used for the display portion 5002. By using the semiconductor device according to one embodiment of the present invention for the display portion 5002, high-contrast image data can be obtained. The display device includes, in its category, any display device for displaying information, such as display devices for personal computers, TV broadcast reception, advertisement, and the like.

[0296]

FIG. 7B illustrates a personal digital assistant including a housing 5101, a display portion 5102, operation keys 5103, and the like. The semiconductor device according to one embodiment of the present invention can be used for the display portion 5102. By using the semiconductor device according to one embodiment of the present invention for the display portion 5102, high-contrast image data can be obtained or power consumption of the personal digital assistant can be reduced.

[0297]

FIG. 7C illustrates an automated teller machine that includes a housing 5201, a display portion 5202, a coin slot 5203, a paper money slot 5204, a card slot 5205, a passbook slot 5206, and the like. The semiconductor device according to one embodiment of the present invention can be used for the display portion 5202. By using the semiconductor device according to one embodiment of the present invention for the display portion 5202, high-contrast image data can be obtained. In addition, the automated teller machine including the semiconductor device according to one embodiment of the present invention can read biometric information such as a finger print, a face, a handprint, a palm print, a pattern of a hand vein, an iris, and the like used for biometric authentication with higher accuracy. It is therefore possible to reduce a false non-match rate which is false recognition of a person to be identified as a different person and a false acceptance rate which is false recognition of a different person as a person to be identified.

[0298]

FIG. 7D illustrates a portable game machine that includes a housing 5301, a housing 5302, a display portion 5303, a display portion 5304, a microphone 5305, a speaker 5306, an operation key 5307, a stylus 5308, and the like. The semiconductor device according to one embodiment of the present invention can be used for the display portion 5303 or the display portion 5304. By using the semiconductor device according to one embodiment of the present invention for the display portion 5303 or the display portion 5304, high-contrast image data can be obtained. Although the portable game machine in FIG. 7D has the two display portions 5303 and 5304, the number of display portions included in the portable game machine is not limited to two.

[0299]

FIG. 7E illustrates a mobile phone that includes a housing 5401, a display portion 5402, an audio input portion 5403, an audio output portion 5404, operation keys 5405, a light-receiving portion 5406, and the like. Light received in the light-receiving portion 5406 is converted into electrical signals, whereby external images can be loaded. The semiconductor display device according to one embodiment of the present invention can be used for the display portion 5402. By using the semiconductor device according to one embodiment of the present invention for the display portion 5402, high-contrast image data can be obtained. In addition, the semiconductor device according to one embodiment of the present invention can be used to convert light received by the light-receiving portion 5406 into electrical signals, whereby high-contrast image data can be obtained.

[0300]

This embodiment can be implemented in combination with any of the other embodiments as appropriate.

[0301]

(Example 1)

In this example, the results of calculating the operation of a photosensor driven by the driving method according to one embodiment of the present invention will be described with reference to FIG. 8, FIGS. 9A and 9B, and FIG. 10.

[0302]

FIG. 8 illustrates the circuit configuration of a photosensor used in this example. In FIG. 8, a PIN photodiode 163 generates a current corresponding to light entering the

i-layer. An equivalent circuit of the PIN photodiode 163 is constituted by a constant current source 161, a capacitor 162, and the photodiode 101. The transistor 102 which is an amplifier element converts a voltage of the charge retention node FD into a current corresponding to the potential of the charge retention node FD. The transistor 103 which is a switching element controls accumulation of charge in the charge retention node FD by the PIN photodiode 163. The transistor 105 controls an output of the photosensor. The charge retention node FD holds charge that varies depending on the amount of light received by the PIN photodiode 163. The wiring TX is a signal line for controlling the transistor 103. The wiring SE is a signal line for controlling the transistor 105. The wiring RD is a signal line for controlling initialization of the potential of the charge retention node FD. The wiring OUT is an output wiring for outputting a signal corresponding to charge accumulation in the PIN photodiode 163. A wiring VSS and a wiring VDD are power supply wirings. A resistor 150 is a pull-down resistor.

[0303]

A method for driving the photosensor in this example is the same as that for the photosensor 100; therefore, the description is not repeated here. For the operation of the photosensor in this example, the timing chart in FIG. 2 can be referred to.

[0304]

In the calculation, the potential of the charge retention node FD at a fall time TX_{H-L} , which is the time it takes to switch the potential of the wiring TX from the potential HTX to the potential LTX at the time T4 in FIG. 2, was evaluated.

[0305]

For the calculation, the circuit simulator SPICE (Simulation Program with Integrated Circuit Emphasis) was used.

[0306]

Specifically, the potential of the charge retention node FD in the operation of the photosensor to which each of the following fall times TX_{H-L} is applied in the cases where the current I_{diode} of the constant current source 161 is 0.10 nanoamperes (nA), 0.30 nA, and 0.34 nA was obtained. Note that the value of I_{diode} corresponds to the intensity of light entering the photodiode 101.

[0307]

As the fall times TX_{H-L} , the following 21 values were used: 0 nanoseconds (ns) which is a conventional example; 1 ns, 2 ns, 3 ns, 4 ns, 5 ns, 6 ns, 7 ns, 8 ns, 9 ns, 10 ns, 20 ns, 30 ns, 40 ns, 50 ns, 60 ns, 70 ns, 80 ns, 90 ns, and 100 ns which are examples to which one embodiment of the present invention is applied; and 200 ns which is a comparative example.

[0308]

Other calculation conditions are as follows. The capacitance of the capacitor 162 was 1 femtofarad (fF). The time for performing an accumulation operation (the time between the time T3 and the time T4 in FIG. 2) was 2.8 milliseconds (ms). The transistors 102, 103, and 105 had the same size and the same characteristics.

[0309]

FIGS. 9A and 9B show the relation between the fall time TX_{H-L} of the wiring TX and the potential of the charge retention node FD. FIG. 9B is an enlarged view of FIG. 9A in the range of the fall time TX_{H-L} from 0 ns to 10 ns. In FIGS. 9A and 9B, the horizontal axis indicates fall time TX_{H-L} (unit: ns) and the vertical axis indicates the potential (unit: V) of the charge retention node FD.

[0310]

As shown in FIGS. 9A and 9B, the potentials in the examples to which one embodiment of the present invention was applied were higher than the potential in the conventional example ($TX_{H-L} = 0$ ns) regardless of the values of I_{diode} .

[0311]

The difference between the potential in the conventional example and the potentials in the examples to which one embodiment of the present invention was applied was larger when the value of I_{diode} was large than when the value of I_{diode} was small. In particular, when I_{diode} was 0.34 nA, the potential in the conventional example ($TX_{H-L} = 0$ ns) was -16.2 V, whereas the potential in the example to which one embodiment of the present invention was applied ($TX_{H-L} = 1$ ns) was -13.8 V. In other words, it has been suggested that clock feedthrough can be suppressed by applying one embodiment of the present invention particularly when the intensity of light entering the photodiode 101 is high.

[0312]

When I_{diode} was 0.34 nA, the potential in the comparative example ($\text{TX}_{\text{H-L}} = 200$ ns) was lower than that in the conventional example.

[0313]

These results show that a change in the potential of the charge retention node FD (clock feedthrough) due to parasitic capacitance of the transistor 103 used in this example can be suppressed when the fall time $\text{TX}_{\text{H-L}}$ of the wiring TX is longer than 0 ns and shorter than 200 ns.

[0314]

In addition, it has been suggested that the fall of a pulse signal of the wiring TX is too gentle when $\text{TX}_{\text{H-L}}$ is equal to or longer than 200 ns, and thus clock feedthrough occurs.

[0315]

FIG. 10 shows the relation between the amount of current I_{diode} of the constant current source 161 and the potential of the charge retention node FD. In FIG. 10, the vertical axis indicates the potential (unit: V) of the charge retention node FD and the horizontal axis indicates I_{diode} (unit: nA). The potential at which all charge leaks from the charge retention node FD is -16.05 V in FIG. 10.

[0316]

In FIG. 10, the potential with $\text{TX}_{\text{H-L}} = 0$ ns, which is the conventional example, reached -16.05 V when I_{diode} was 0.34 nA. On the other hand, the potential with $\text{TX}_{\text{H-L}} = 10$ ns, which is the example to which one embodiment of the present invention was applied, reached -16.05 V when I_{diode} was 0.38 nA.

[0317]

In other words, the conventional photosensor can output signals corresponding to potentials that correspond to the intensity of light with I_{diode} in the range of 0 to 0.34 nA. In addition, the photosensor to which one embodiment of the present invention is applied can output signals corresponding to potentials that correspond to a wider range of light intensity, that is, the intensity of light with I_{diode} in the range of 0 to 0.38 nA.

[0318]

These results suggest that the photosensor to which one embodiment of the present invention is applied can obtain data of a higher contrast image than the

conventional photosensor.

[0319]

(Example 2)

5 In this example, the operation of a solid-state imaging device which is a semiconductor device according to one embodiment of the present invention will be described with reference to FIGS. 11A and 11B, FIGS. 12A and 12B, and FIGS. 13A and 13B.

[0320]

10 This example explains two solid-state imaging devices: a structural example to which one embodiment of the present invention is applied, and a comparative example to which the present invention is not applied. The configurations of photosensors included in the solid-state imaging devices used in this example are described.

[0321]

15 The photosensor included in the solid-state imaging device of the structural example is a photosensor 112 illustrated in FIG. 13A.

[0322]

20 In the photosensor 112, the photodiode 101 generates a current corresponding to light entering the i-layer. The transistor 102 which is an amplifier element converts a voltage of the charge retention node FD into a current corresponding to the potential of the charge retention node FD. The transistor 103 which is a switching element controls accumulation of charge in the charge retention node FD by the photodiode 101. The transistor 105 controls an output of the photosensor. The charge retention node FD holds charge that varies depending on the amount of light received by the photodiode 101.

25 [0323]

In FIG. 13A, the wiring TX is a signal line for controlling the transistor 103. The wiring SE is a signal line for controlling the transistor 105. The wiring RD is a signal line for controlling initialization of the potential of the charge retention node FD. The wiring OUT is an output wiring for outputting a signal corresponding to charge accumulation in the photodiode 101. The wiring VSS and the wiring VDD are power supply wirings. The resistor 150 is a pull-down resistor. A capacitor 151 is electrically connected to the wiring TX.

[0324]

The photosensor included in the comparative solid-state imaging device is a photosensor 113 illustrated in FIG. 13B. The photosensor 113 has the same configuration as the photosensor 112 except that the capacitor 151 is not provided.

5 [0325]

The operation of the photosensors included in the solid-state imaging devices used in this example will be described. For the operation of the photosensors in this example, the timing chart in FIG. 2 can be referred to. In this example, the potentials of the wiring TX were set such that the potential HTX was 3 V and the potential LTX
10 was -16 V.

[0326]

FIG. 11A shows a waveform of an input to the wiring TX in the structural example. Note that 0 milliseconds (ms) shown in FIG. 11A corresponds to the time T4 in FIG. 2. Specifically, the capacitor 151 with a capacitance of 1 μ F (microfarad) was
15 used so that the level of a pulse changes from the potential HTX to the potential LTX more gently than in the comparative example.

[0327]

FIG. 11B shows a waveform of an input to the wiring TX in the comparative example. Note that 0 ms shown in FIG. 11B corresponds to the time T4 in FIG. 2. Specifically, the level of a pulse changes from the potential HTX to the potential LTX at
20 the time of 0 ms.

[0328]

In FIGS. 11A and 11B, the vertical axis indicates the potential (unit: V) of the wiring TX and the horizontal axis indicates time (unit: ms).

25 [0329]

Next, the configuration of a photosensor reading circuit will be described with reference to FIG. 14. A display portion in the solid-state imaging device in this example includes pixels of 1024 rows and 768 columns. One display element is provided in every pixel in each row and each column. One photosensor is provided in
30 every four pixels in two rows and two columns. That is, the display elements are provided in 1024 rows and 768 columns, and the photosensors are provided in 512 rows

and 384 columns. In addition, photosensor output signal lines of two columns are regarded as one pair. In other words, one output is obtained from two photosensors provided between eight pixels in two rows and four columns and is output to the outside of the display device.

5 [0330]

A scan line driver circuit for the photosensors illustrated in FIG. 14 simultaneously drives pixels in four rows (i.e., photosensors in two rows) and sequentially shifts selected rows of photosensors by one row, which corresponds to two rows of pixels. Here, photosensors in each row are continually selected in a period
10 during which the scan line driver circuit shifts selected rows twice. Note that outputs of photosensors in two rows are superimposed in a photosensor output signal line 343 at one time. All the photosensors can be driven by repeating a shift of selected rows 512 times.

[0331]

15 As illustrated in FIG. 14, the photosensor reading circuit includes one selector per 24 columns of pixels. The selector selects one pair from 12 pairs of photosensor output signal lines 343 (one pair corresponds to the photosensor output signal lines 343 of two columns) in the display portion and obtains an output. That is, the photosensor reading circuit includes 32 selectors in total and thus obtains 32 outputs at one time.
20 Selection is performed on all the 12 pairs by each of the selectors, whereby a total of 384 outputs which correspond to photosensors in one row can be obtained. The selector selects one pair from the 12 pairs every time selected rows are shifted by the scan line driver circuit for the photosensors, so that outputs from all of the photosensors can be obtained.

25 [0332]

In this example, as illustrated in FIG. 14, an output of the photosensor, which is an analog signal, is extracted to the outside of the display device, amplified by an amplifier provided outside the display device, and converted into a digital signal with an AD converter.

30 [0333]

FIGS. 12A and 12B are histograms each showing the results of capturing images of a black object and a white object with the solid-state imaging devices in this

example. In FIGS. 12A and 12B, the vertical axis indicates the number of pixels (no unit) and the horizontal axis indicates the output voltage (unit: V) of the AD converter.

[0334]

In FIG. 12B, the result of capturing an image of the black object with the comparative solid-state imaging device is shown by a solid line, and the result of capturing an image of the white object is shown by a dashed line. FIGS. 15C and 15D show the actually obtained images of the black object and the white object, respectively. As seen from FIG. 12B and FIGS. 15C and 15D, the contrast between black and white is very low.

[0335]

In FIG. 12A, the result of capturing an image of the black object with the solid-state imaging device of the structural example is shown by a solid line, and the result of capturing an image of the white object is shown by a dashed line. FIGS. 15A and 15B show the actually obtained images of the black object and the white object, respectively. As seen from FIG. 12A and FIGS. 15A and 15B, the contrast between black and white is higher than that in the comparative device.

[0336]

These results suggest that when the capacitor electrically connected to the wiring TX is provided in the solid-state imaging device and a pulse whose level changes from the potential HTX to the potential LTX gently by using the capacitor is input as the potential of the wiring TX, a change in the potential of the charge retention node FD (clock feedthrough) due to parasitic capacitance of the transistor 103 can be suppressed.

[0337]

As has been described, by applying one embodiment of the present invention, a semiconductor device that includes the photosensor, is small in size, and can obtain high-contrast image data can be provided.

[0338]

(Example 3)

In this example, an example of a transistor in which an In-Sn-Zn-O film is used as an oxide semiconductor film will be described with reference to FIGS. 31A and 31B.

[0339]

FIGS. 31A and 31B are a top view and a cross-sectional view of a coplanar

transistor having a top-gate top-contact structure. FIG. 31A is the top view of the transistor. FIG. 31B illustrates cross section A-B along dashed-dotted line A-B in FIG. 31A.

[0340]

5 The transistor illustrated in FIG. 31B includes a substrate 2100; a base insulating layer 2102 provided over the substrate 2100; a protective insulating film 2104 provided in the periphery of the base insulating layer 2102; an oxide semiconductor film 2106 that is provided over the base insulating layer 2102 and the protective insulating film 2104 and includes a high-resistance region 2106a and low-resistance regions
10 2106b; a gate insulating layer 2108 provided over the oxide semiconductor film 2106; a gate electrode 2110 provided to overlap with the oxide semiconductor film 2106 with the gate insulating layer 2108 positioned therebetween; a sidewall insulating film 2112 provided in contact with a side surface of the gate electrode 2110; a pair of electrodes 2114 provided in contact with at least the low-resistance regions 2106b; an interlayer
15 insulating film 2116 provided to cover at least the oxide semiconductor film 2106, the gate electrode 2110, and the pair of electrodes 2114; and a wiring 2118 provided to be connected to at least one of the pair of electrodes 2114 through an opening formed in the interlayer insulating film 2116.

[0341]

20 Although not illustrated, a protective film may be provided to cover the interlayer insulating film 2116 and the wiring 2118. With the protective film, a minute amount of leakage current generated by surface conduction of the interlayer insulating film 2116 can be reduced, so that the off-state current of the transistor can be reduced.

[0342]

25 This example can be implemented in appropriate combination with any of the structures described in the other embodiments and examples.

[0343]

(Example 4)

30 In this example, another example of a transistor in which an In-Sn-Zn-O film is used as an oxide semiconductor film, which is different from the transistor in Example 3, will be described with reference to FIGS. 32A and 32B.

[0344]

FIGS. 32A and 32B are a top view and a cross-sectional view illustrating a structure of a transistor. FIG. 32A is the top view of the transistor. FIG. 32B is a cross-sectional view along dashed-dotted line A-B in FIG. 32A.

[0345]

5 The transistor illustrated in FIG. 32B includes a substrate 6000; a base insulating layer 6020 provided over the substrate 6000; an oxide semiconductor film 6060 provided over the base insulating layer 6020; a pair of electrodes 6140 in contact with the oxide semiconductor film 6060; a gate insulating layer 6080 provided over the oxide semiconductor film 6060 and the pair of electrodes 6140; a gate electrode 6100
10 provided to overlap with the oxide semiconductor film 6060 with the gate insulating layer 6080 positioned therebetween; an interlayer insulating film 6160 provided to cover the gate insulating layer 6080 and the gate electrode 6100; wirings 6180 connected to the pair of electrodes 6140 through openings formed in the interlayer insulating film 6160; and a protective film 6200 provided to cover the interlayer
15 insulating film 6160 and the wirings 6180.

[0346]

 As the substrate 6000, a glass substrate was used. As the base insulating layer 6020, a silicon oxide film was used. As the oxide semiconductor film 6060, an In-Sn-Zn-O film was used. As the pair of electrodes 6140, a tungsten film was used.
20 As the gate insulating layer 6080, a silicon oxide film was used. The gate electrode 6100 had a stacked structure of a tantalum nitride film and a tungsten film. The interlayer insulating film 6160 had a stacked structure of a silicon oxynitride film and a polyimide film. The wirings 6180 had a stacked structure in which a titanium film, an aluminum film, and a titanium film were formed in this order. As the protective film
25 6200, a polyimide film was used.

[0347]

 Note that in the transistor having the structure illustrated in FIG. 32A, the width of a portion where the gate electrode 6100 overlaps with one of the pair of electrodes 6140 is referred to as L_{ov} . Similarly, the width of a portion of the pair of electrodes 6140, which does not overlap with the oxide semiconductor film 6060, is referred to as dW .
30

[0348]

This example can be implemented in appropriate combination with any of the structures described in the other embodiments and examples.

EXPLANATION OF REFERENCES

- 5 [0349]
100: photosensor, 101: photodiode, 102: transistor, 103: transistor, 105: transistor, 107: transistor, 110: photosensor, 111: photosensor, 112: photosensor, 113: photosensor, 150: resistor, 151: capacitor, 161: constant current source, 162: capacitor, 163: PIN photodiode, 343: output signal line, 601: gate electrode layer, 602: gate insulating layer,
10 603: oxide semiconductor layer, 605a: source electrode layer, 605b: drain electrode layer, 607: insulating layer, 620: transistor, 627: channel protective layer, 630: transistor, 636a: source wiring layer, 636b: drain wiring layer, 637: base insulating layer, 640: transistor, 650: transistor, 700: substrate, 701: insulating film, 702: semiconductor film, 703: semiconductor film, 704: photodiode, 705: transistor, 707: gate electrode, 708:
15 insulating film, 711: wiring, 712: insulating film, 713: gate electrode, 714: gate insulating layer, 715: oxide semiconductor layer, 716: conductive film, 717: conductive film, 718: conductive film, 719: conductive film, 720: conductive film, 721: conductive film, 722: insulating film, 724: transistor, 727: region, 728: region, 729: region, 1010: base insulating layer, 1030a: semiconductor region, 1030b: semiconductor region,
20 1030c: semiconductor region, 1040: gate insulating layer, 2100: substrate, 2102: base insulating layer, 2104: protective insulating film, 2106: oxide semiconductor film, 2106a: high-resistance region, 2106b: low-resistance region, 2108: gate insulating layer, 2110: gate electrode, 2112: sidewall insulating film, 2114: electrode, 2116: interlayer insulating film, 2118: wiring, 5001: housing, 5002: display portion, 5003: supporting
25 base, 5101: housing, 5102: display portion, 5103: operation key, 5201: housing, 5202: display portion, 5203: coin slot, 5204: paper money slot, 5205: card slot, 5206: passbook slot, 5301: housing, 5302: housing, 5303: display portion, 5304: display portion, 5305: microphone, 5306: speaker, 5307: operation key, 5308: stylus, 5401: housing, 5402: display portion, 5403: audio input portion, 5404: audio output portion,
30 5405: operation key, 5406: light-receiving portion, 6000: substrate, 6020: base insulating layer, 6060: oxide semiconductor film, 6080: gate insulating layer, 6100: gate electrode, 6140: electrode, 6160: interlayer insulating film, 6180: wiring, 6200:

protective film

This application is based on Japanese Patent Application serial No. 2010-267422 and No. 2011-108164 filed with Japan Patent Office on November 30,
5 2010 and May 13, 2011, respectively, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A method for driving a photosensor including a light-receiving element, a transistor serving as a switching element, and a charge retention node electrically connected to the light-receiving element through the transistor, the method comprising the step of:

suppressing reduction in charge held in the charge retention node by extending a fall time of an input waveform of a driving pulse supplied to the transistor to turn off the transistor.

2. The method for driving a photosensor, according to claim 1, wherein a channel formation region of the transistor comprises an oxide semiconductor.

3. The method for driving a photosensor, according to claim 1, wherein the fall time of the input waveform of the driving pulse supplied to the transistor to turn off the transistor is longer than 0 ns and shorter than 200 ns.

4. A method for driving a semiconductor device including a photosensor including a light-receiving element, a transistor serving as a switching element, and a charge retention node electrically connected to the light-receiving element through the transistor; and a capacitor electrically connected to a signal line configured to control the transistor, the method comprising the step of:

suppressing reduction in charge held in the charge retention node by extending, by the capacitor, a fall time of an input waveform of a driving pulse supplied to the transistor to turn off the transistor.

5. The method for driving a semiconductor device, according to claim 4, wherein a channel formation region of the transistor comprises an oxide semiconductor.

6. The method for driving a semiconductor device, according to claim 4, wherein the fall time of the input waveform of the driving pulse supplied to the transistor to turn off the transistor is longer than 0 ns and shorter than 200 ns.

7. A semiconductor device comprising:

a photosensor including a light-receiving element, a transistor, and a charge retention node electrically connected to the light-receiving element through the transistor,

wherein reduction in charge held in the charge retention node is suppressed by extending a fall time of an input waveform of a driving pulse supplied to the transistor to turn off the transistor.

8. The semiconductor device according to claim 7, wherein a channel formation region of the transistor comprises an oxide semiconductor.

9. The semiconductor device according to claim 7, wherein the fall time of the input waveform of the driving pulse supplied to the transistor to turn off the transistor is longer than 0 ns and shorter than 200 ns.

10. An electronic device comprising the semiconductor device according to claim 7.

11. An electronic device comprising the semiconductor device according to claim 8.

12. A semiconductor device comprising:

a photosensor including a light-receiving element, a transistor, and a charge retention node electrically connected to the light-receiving element through the transistor; and

a capacitor electrically connected to a signal line configured to control the transistor,

wherein reduction in charge held in the charge retention node is suppressed by extending, by the capacitor, a fall time of an input waveform of a driving pulse supplied to the transistor to turn off the transistor.

13. The semiconductor device according to claim 12, wherein a channel formation region of the transistor comprises an oxide semiconductor.

5 14. The semiconductor device according to claim 12, wherein the fall time of the input waveform of the driving pulse supplied to the transistor to turn off the transistor is longer than 0 ns and shorter than 200 ns.

10 15. An electronic device comprising the semiconductor device according to claim 12.

16. An electronic device comprising the semiconductor device according to claim 13.

15 17. A semiconductor device comprising a display portion, the display portion comprising:

a display element; and

a photosensor including a light-receiving element, a transistor, and a charge retention node electrically connected to the light-receiving element through the transistor,

20 wherein reduction in charge held in the charge retention node is suppressed by extending a fall time of an input waveform of a driving pulse supplied to the transistor to turn off the transistor.

25 18. The semiconductor device according to claim 17, wherein a channel formation region of the transistor comprises an oxide semiconductor.

19. The semiconductor device according to claim 17, wherein the fall time of the input waveform of the driving pulse supplied to the transistor to turn off the transistor is longer than 0 ns and shorter than 200 ns.

30 20. A semiconductor device comprising a display portion, the display portion comprising:

a display element;

a photosensor including a light-receiving element, a transistor, and a charge retention node electrically connected to the light-receiving element through the transistor; and

5 a capacitor electrically connected to a signal line configured to control the transistor,

wherein reduction in charge held in the charge retention node is suppressed by extending, by the capacitor, a fall time of an input waveform of a driving pulse supplied to the transistor to turn off the transistor.

10

21. The semiconductor device according to claim 20, wherein a channel formation region of the transistor comprises an oxide semiconductor.

22. The semiconductor device according to claim 20, wherein the fall time of
15 the input waveform of the driving pulse supplied to the transistor to turn off the transistor is longer than 0 ns and shorter than 200 ns.

20

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FIG. 1A

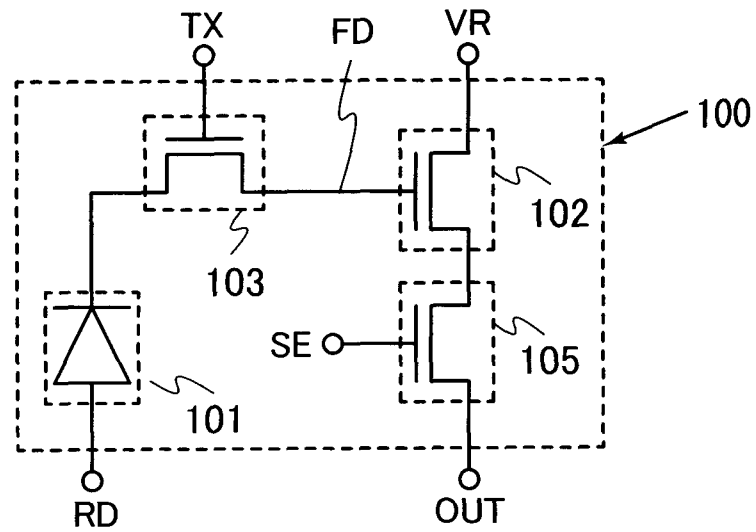


FIG. 1B

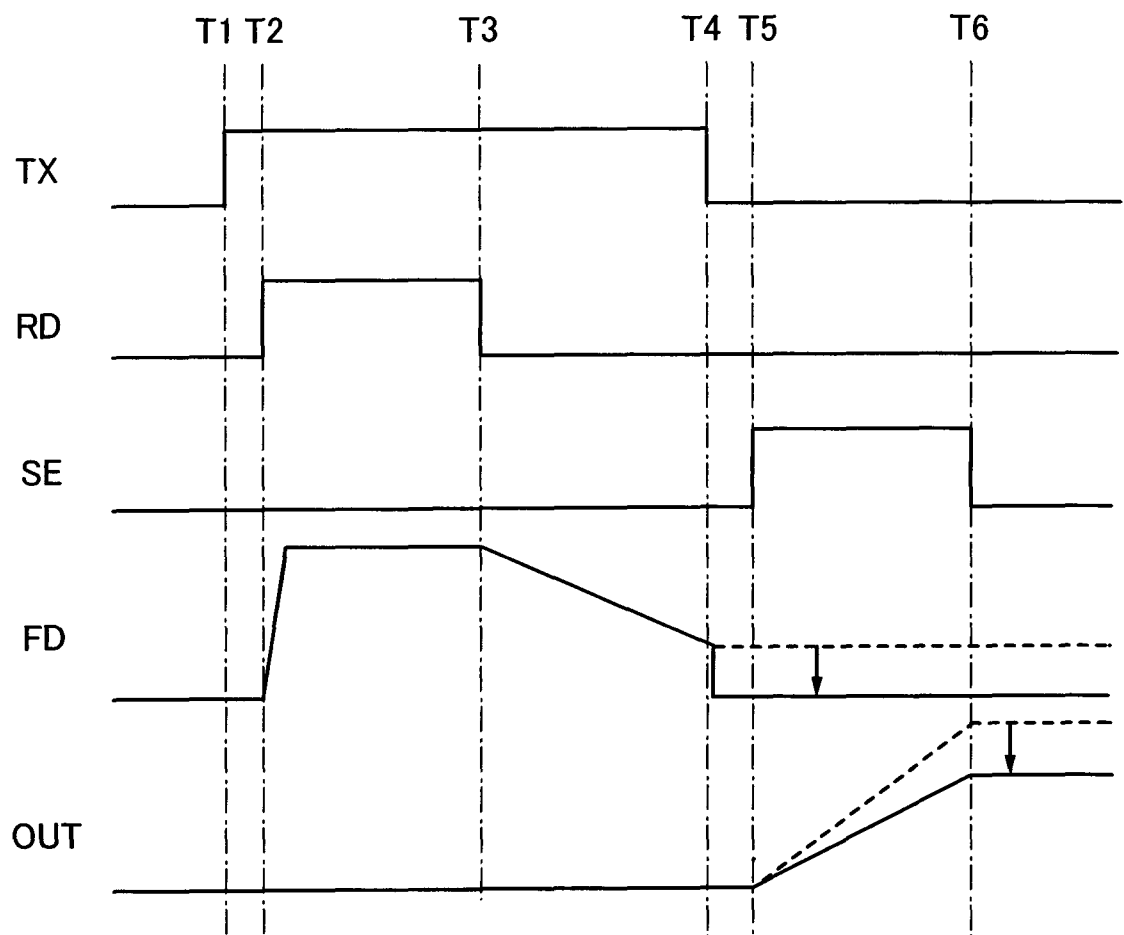
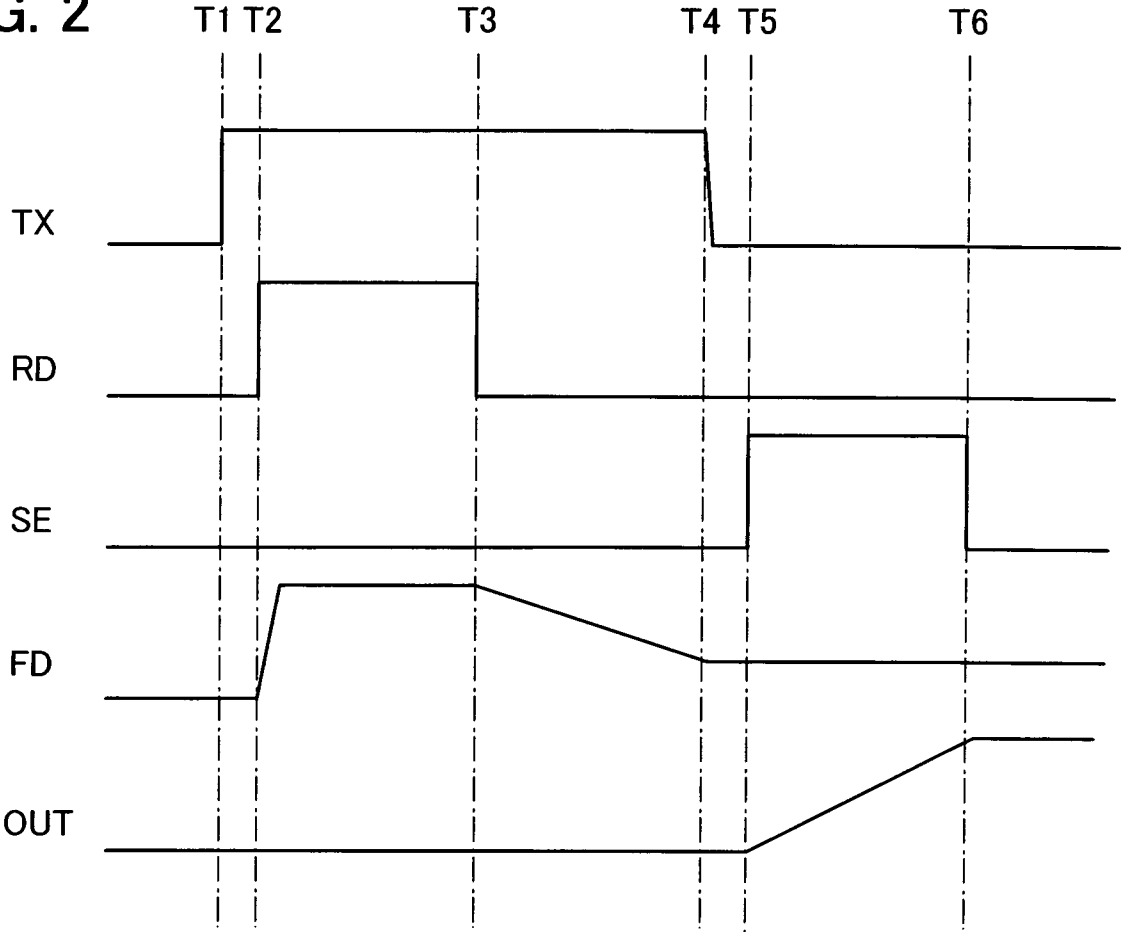


FIG. 2



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FIG. 3A

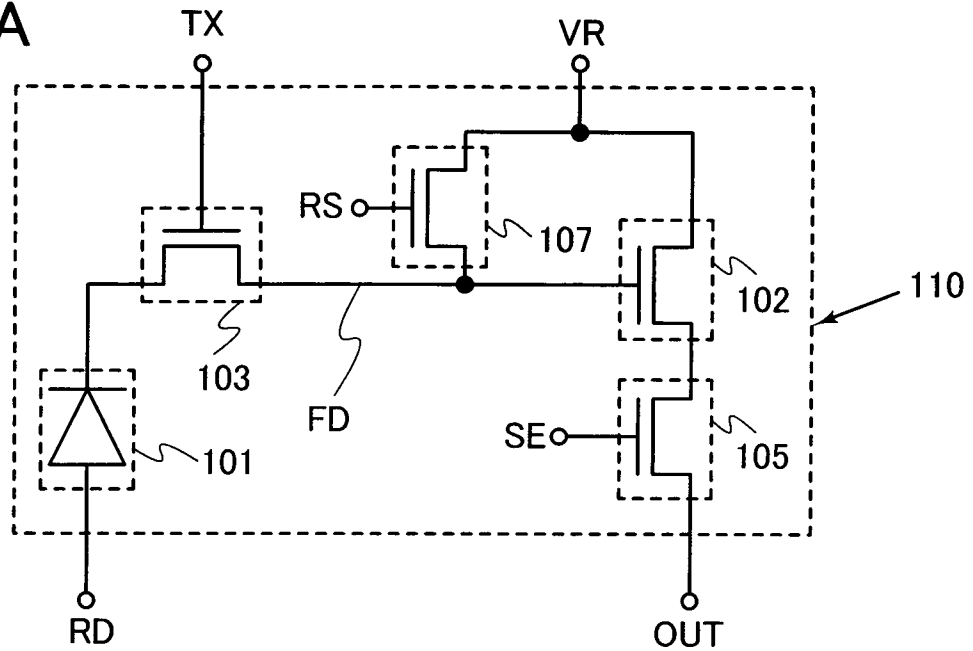


FIG. 3B

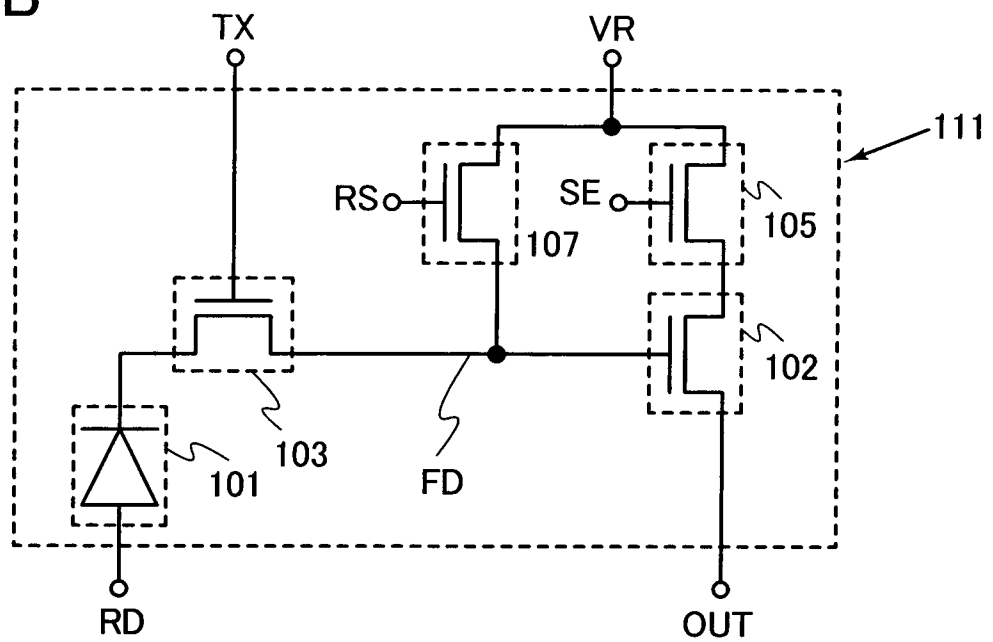


FIG. 4

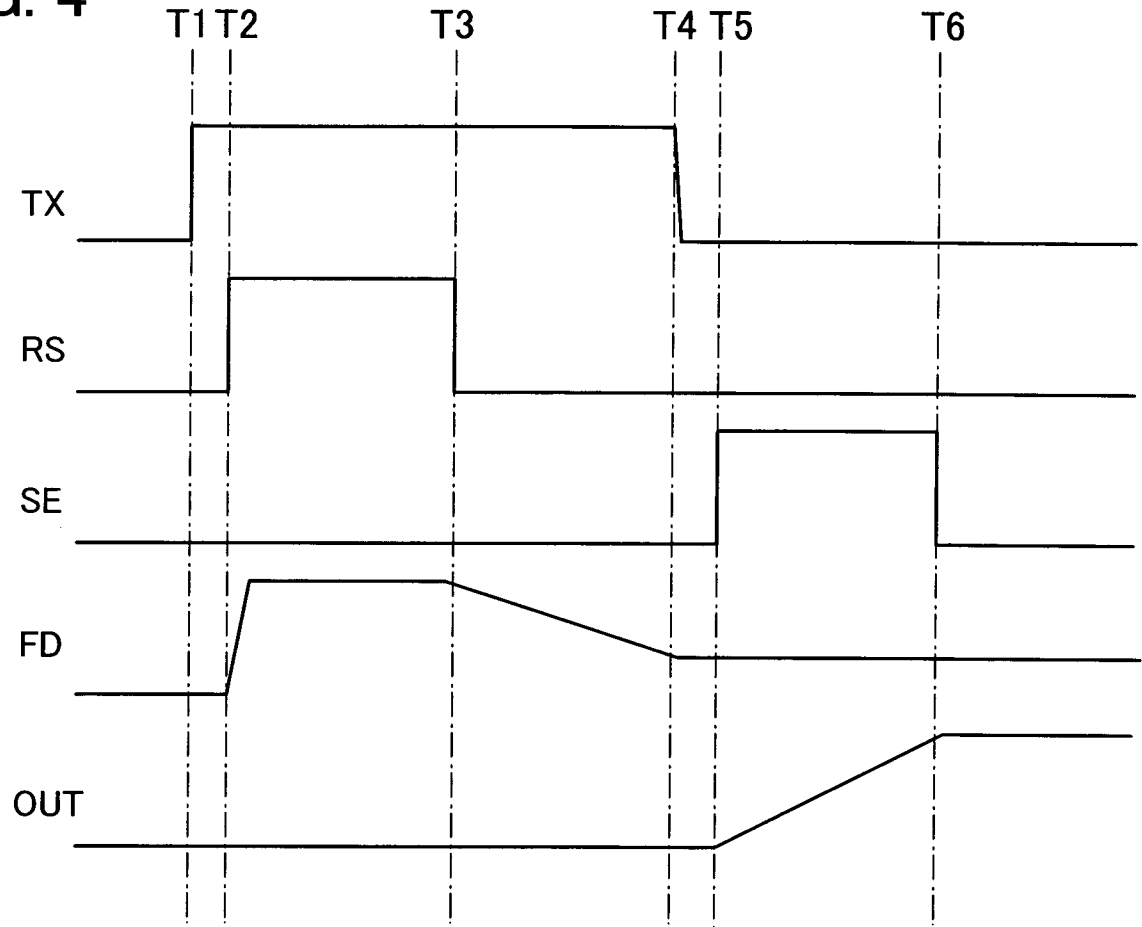


FIG. 5A

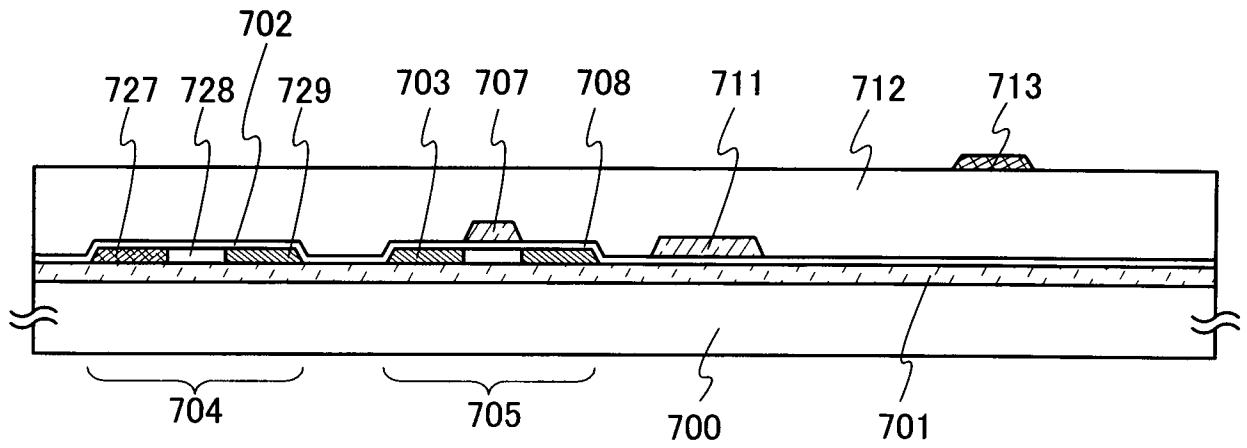


FIG. 5B

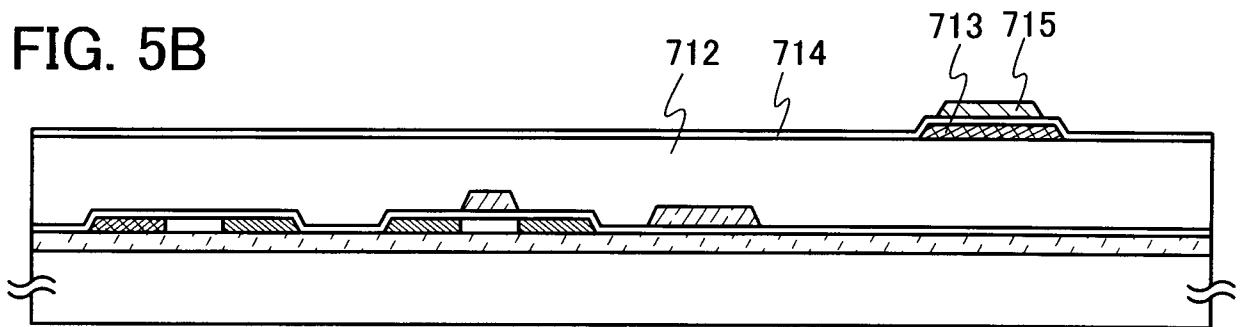
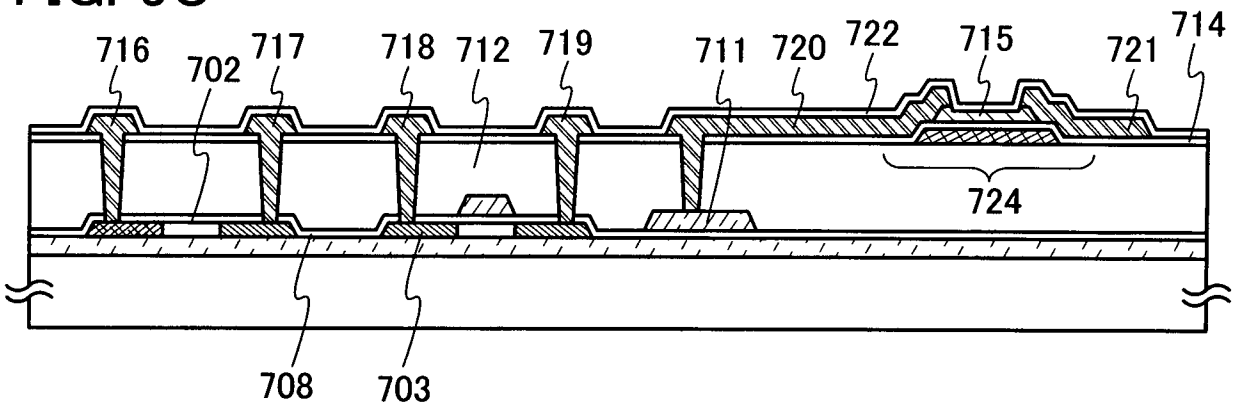


FIG. 5C



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FIG. 6A

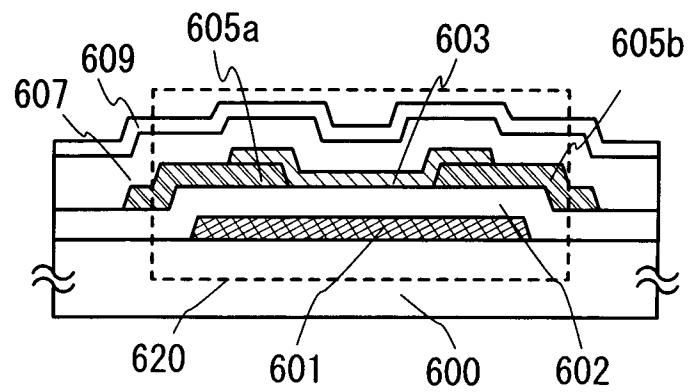


FIG. 6B

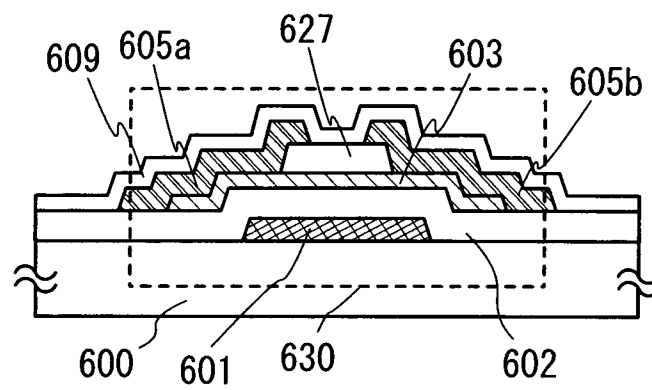


FIG. 6C

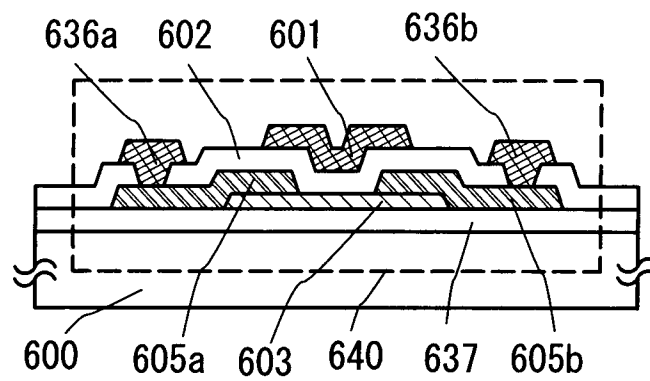


FIG. 6D

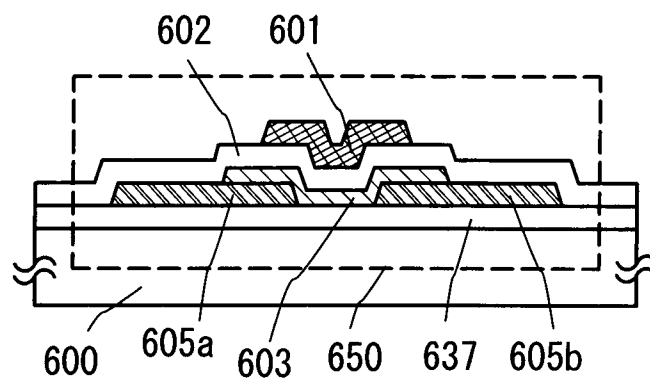


FIG. 7A

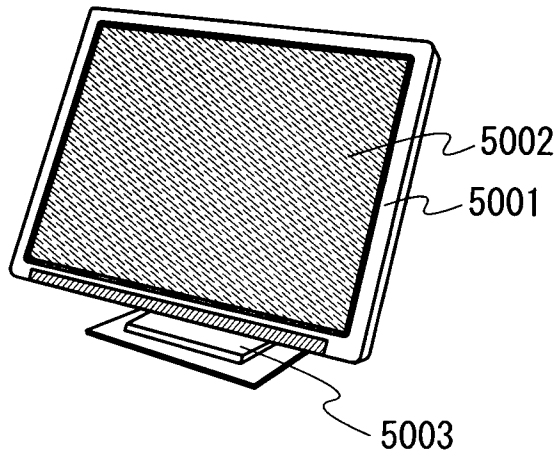


FIG. 7B

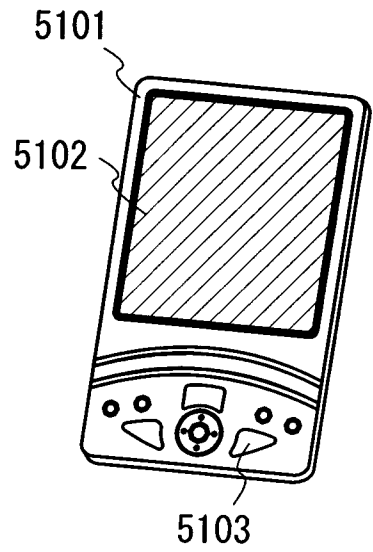


FIG. 7C

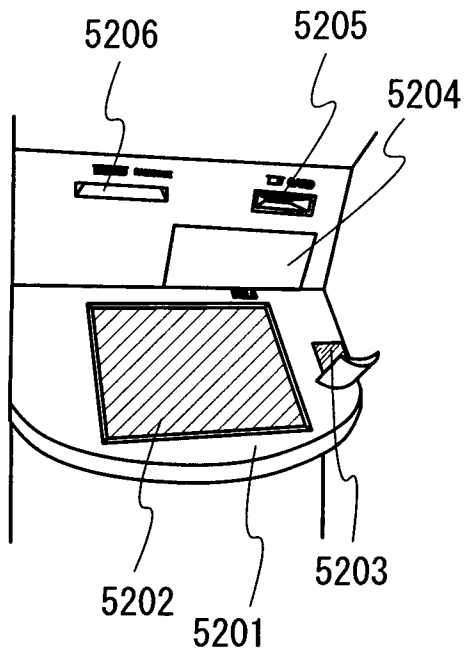


FIG. 7D

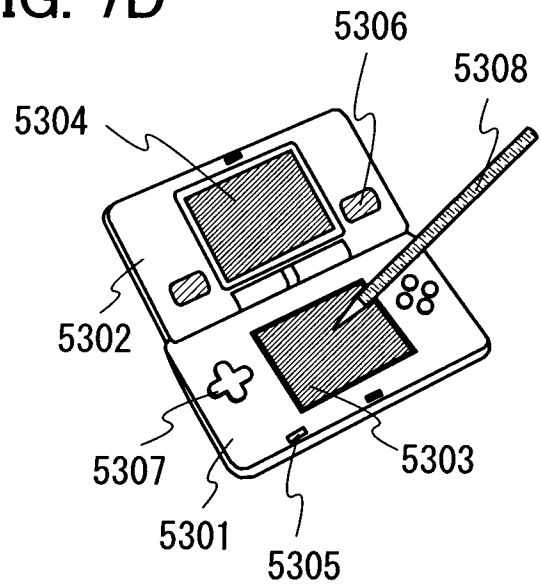
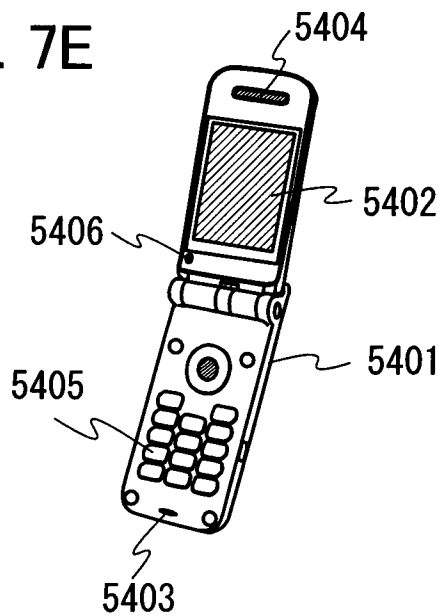
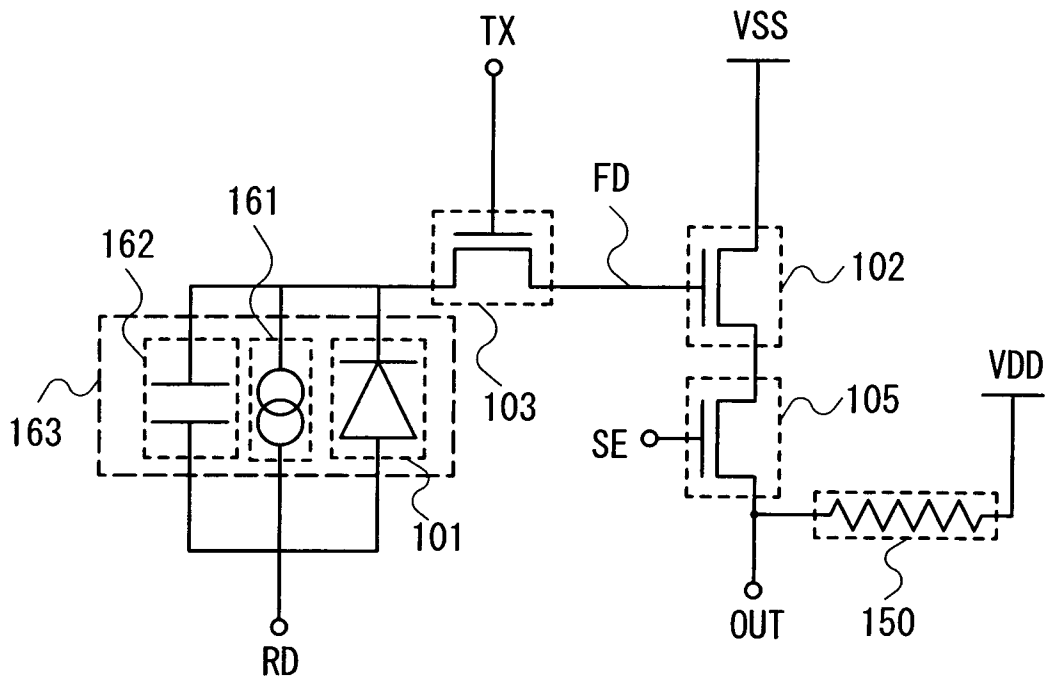


FIG. 7E



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FIG. 8



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FIG. 9A

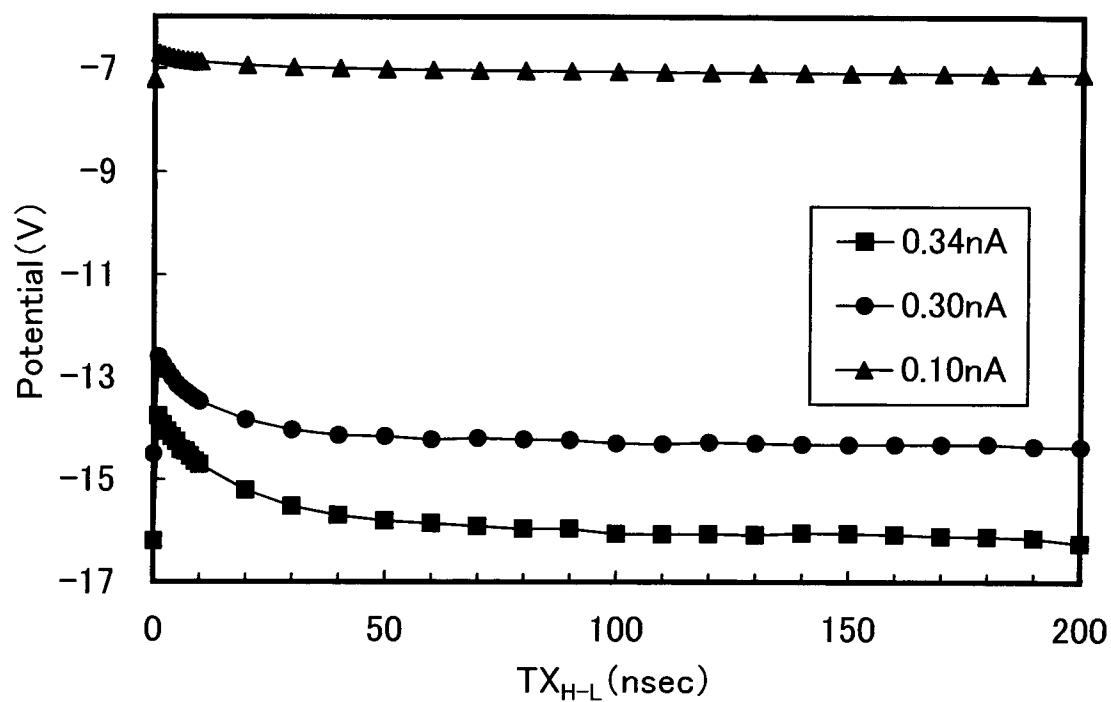
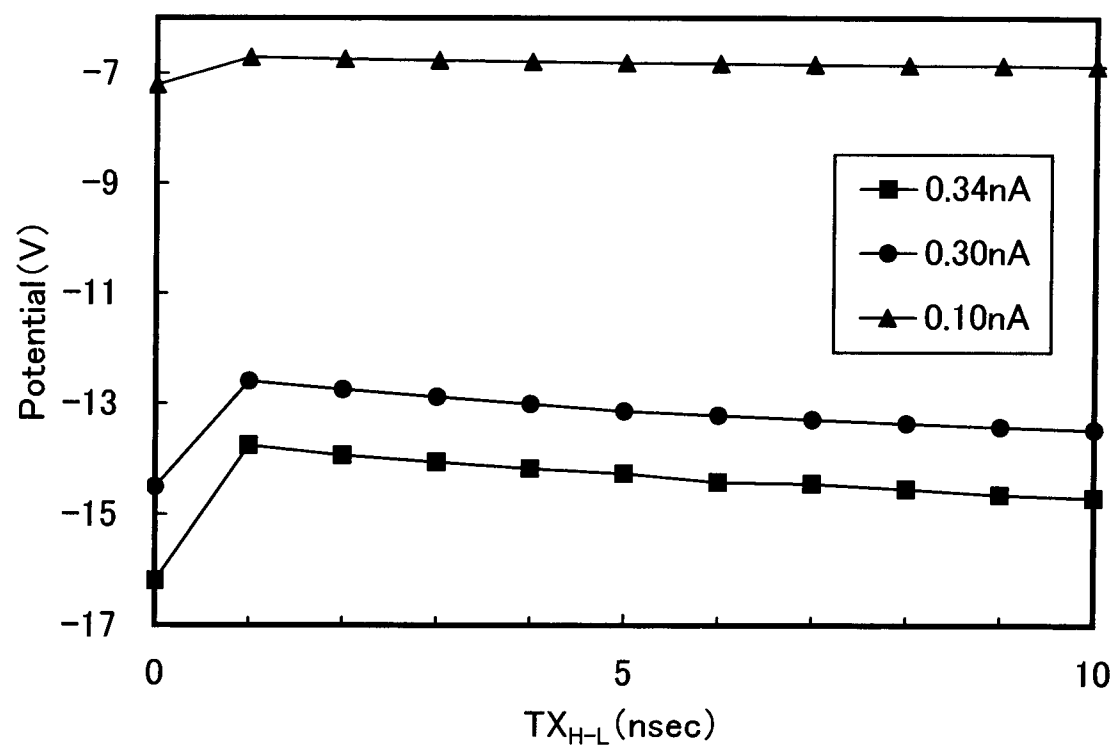
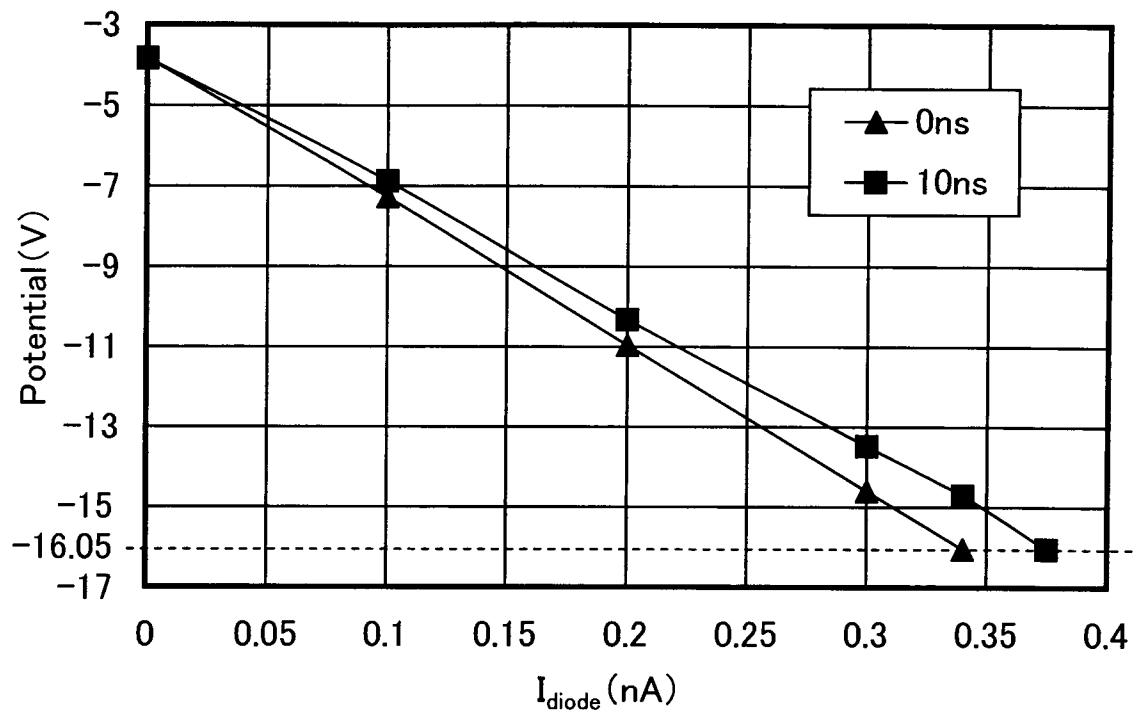


FIG. 9B



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FIG. 10



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FIG. 11A

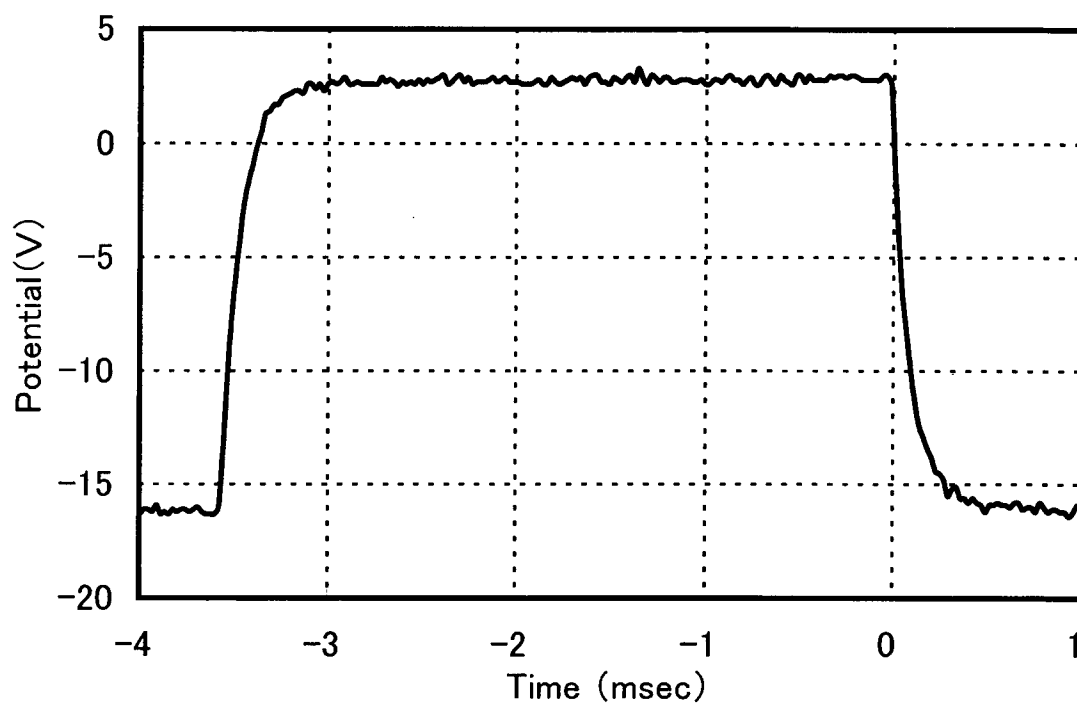
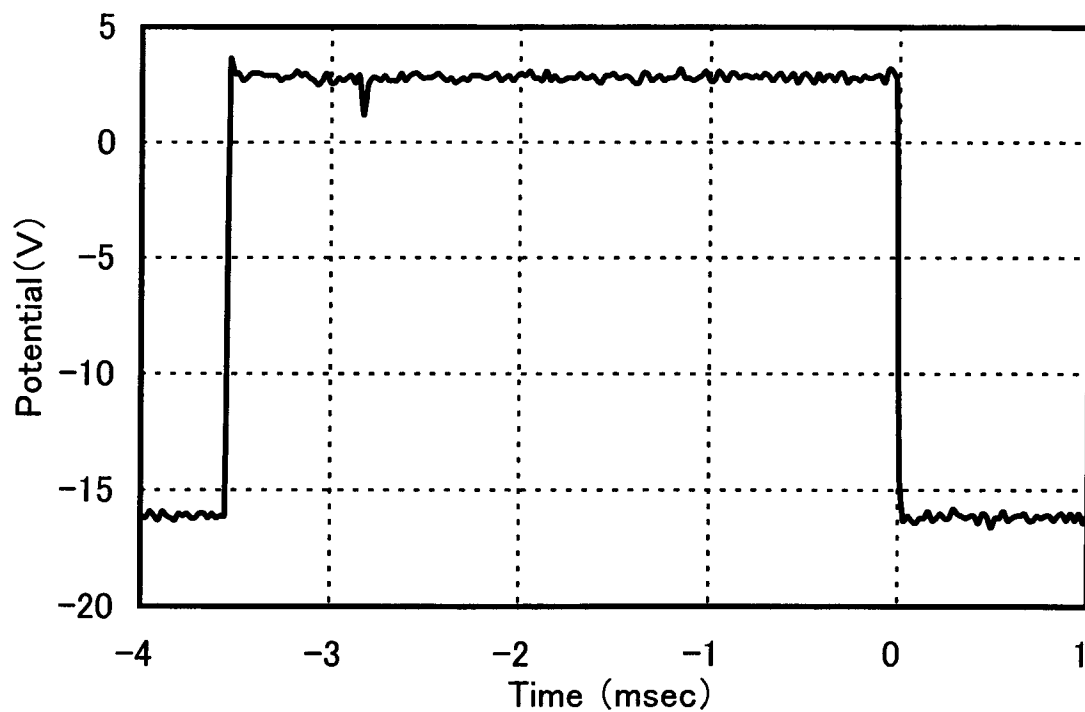


FIG. 11B



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FIG. 12A

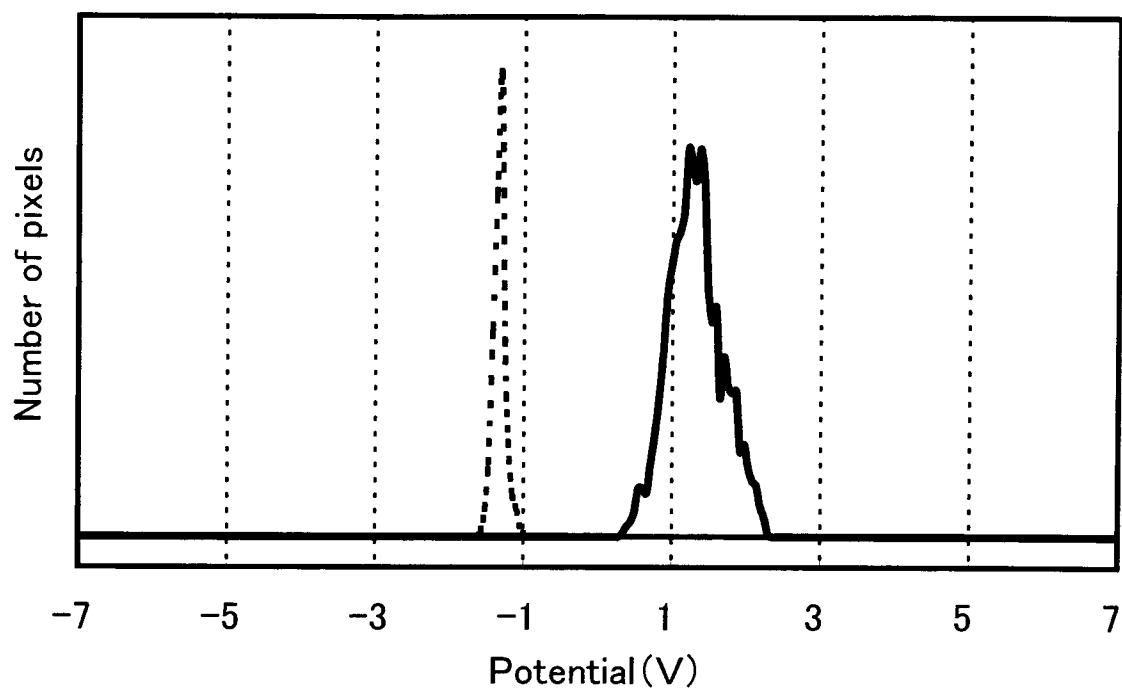


FIG. 12B

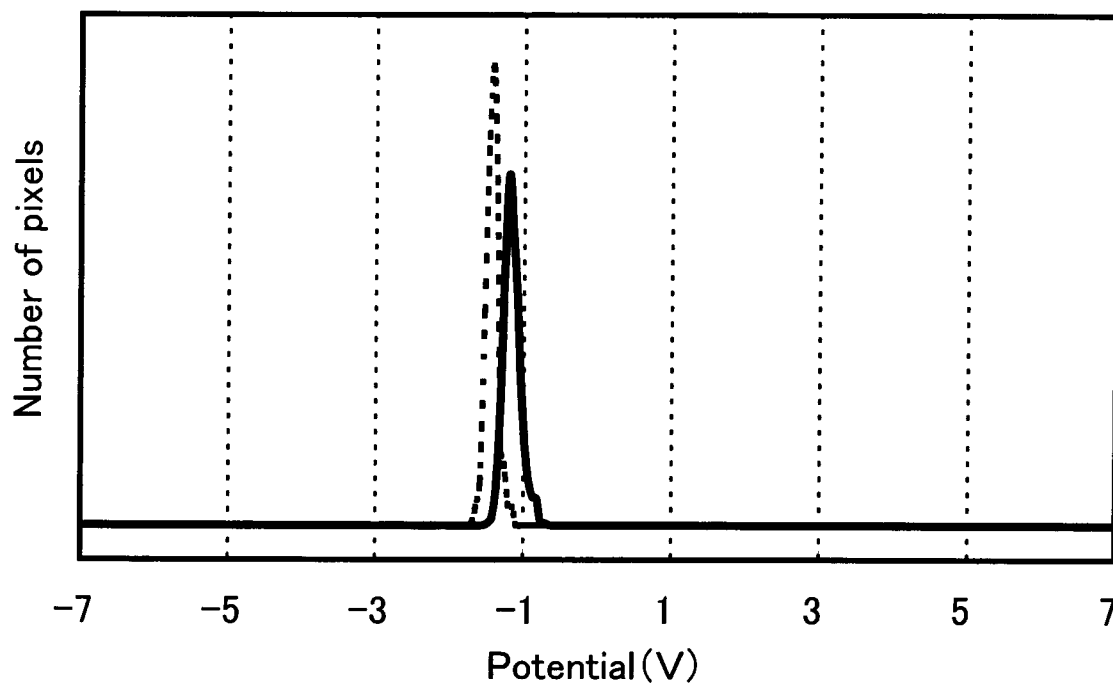


FIG. 13A

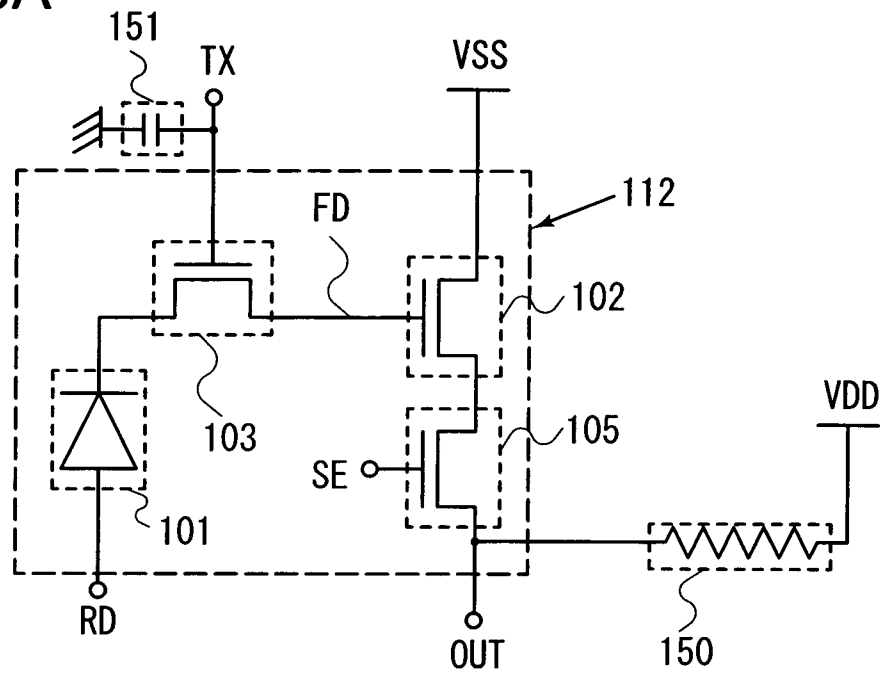


FIG. 13B

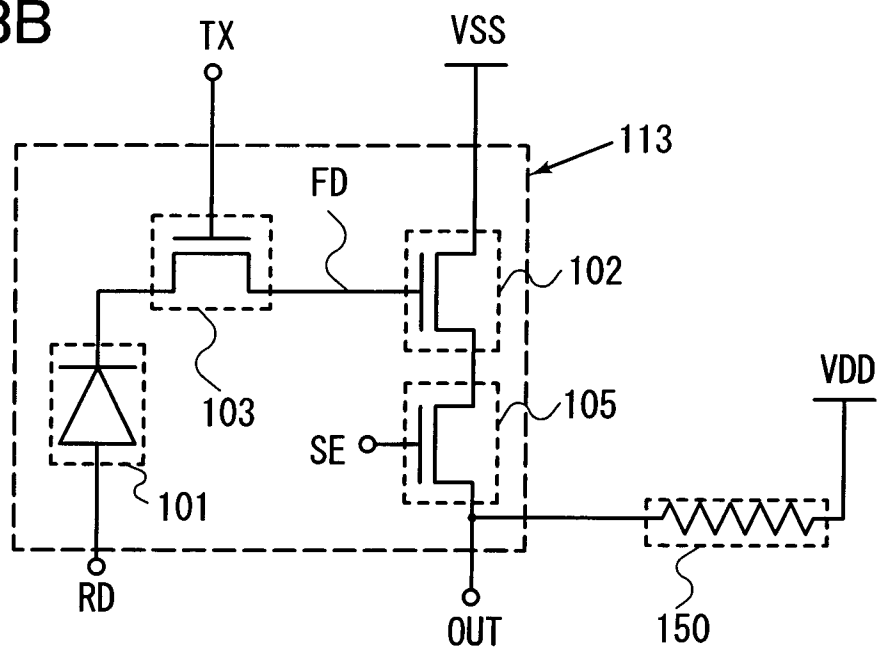
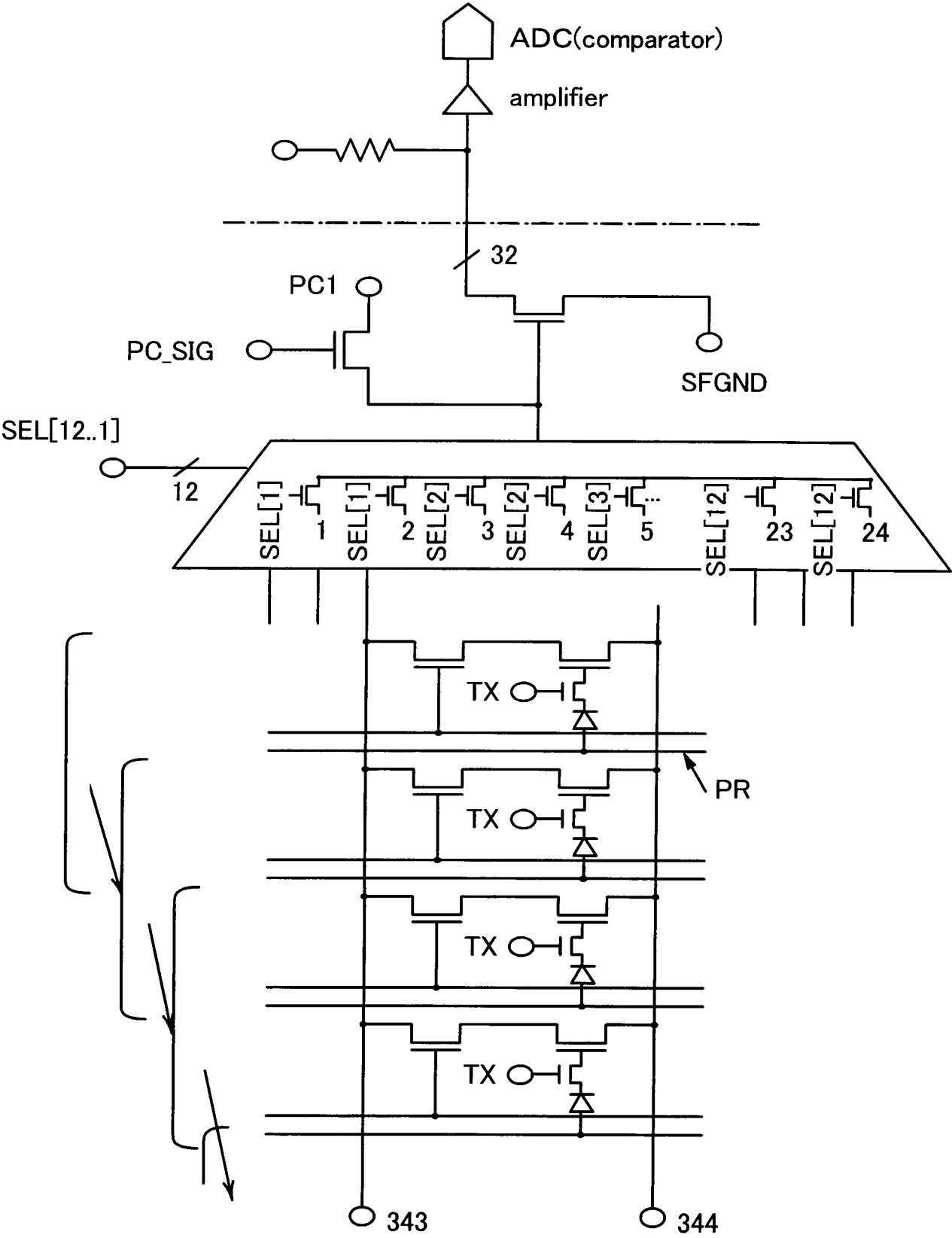


FIG. 14



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FIG. 15A

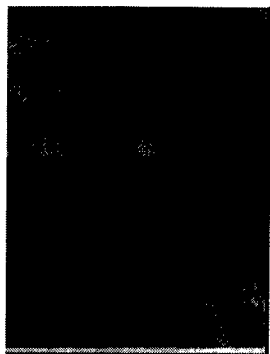


FIG. 15B

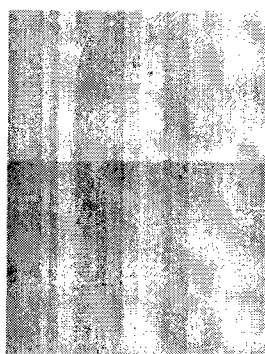


FIG. 15C

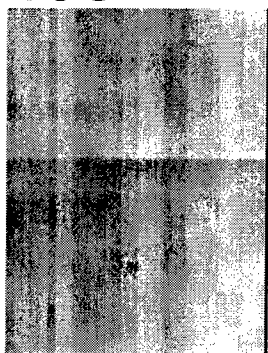
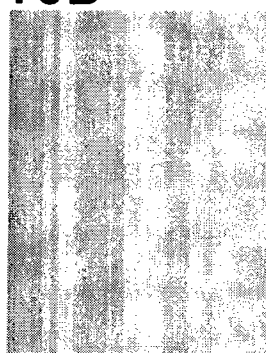


FIG. 15D



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FIG. 16A

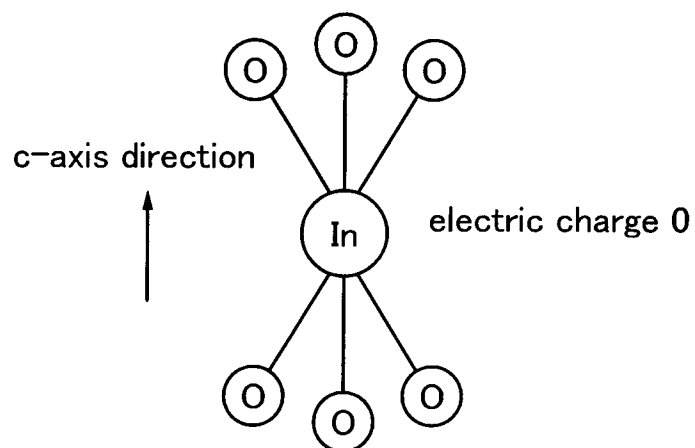


FIG. 16D

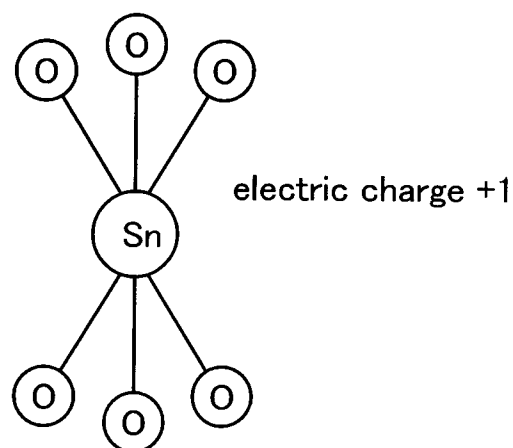


FIG. 16B

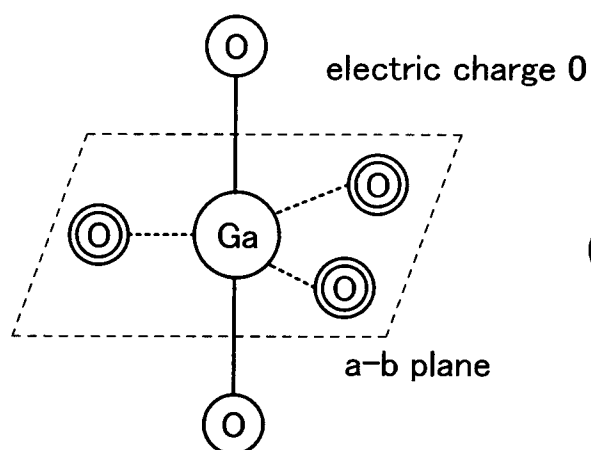


FIG. 16E

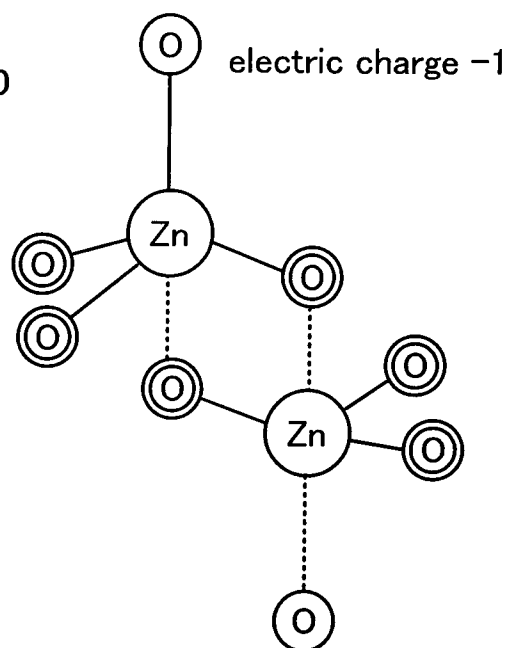


FIG. 16C

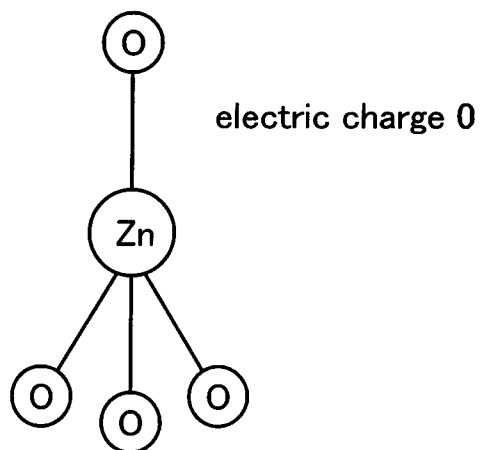


FIG. 17A

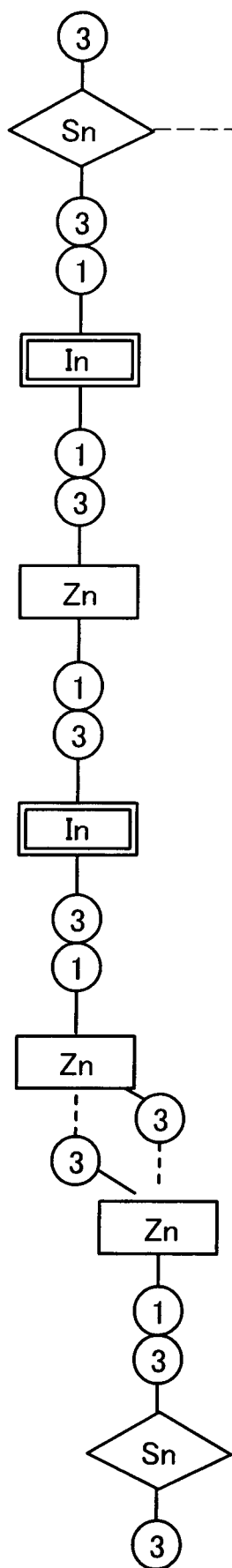
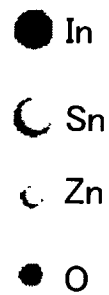
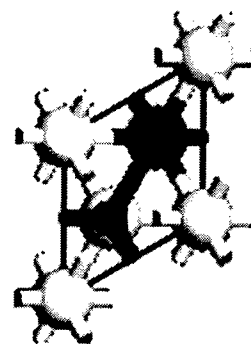


FIG. 17B



FIG. 17C



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FIG. 18A

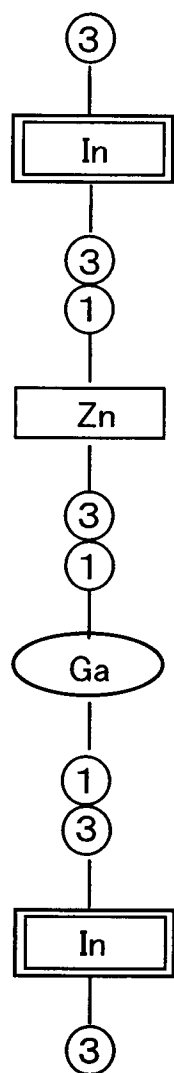


FIG. 18B

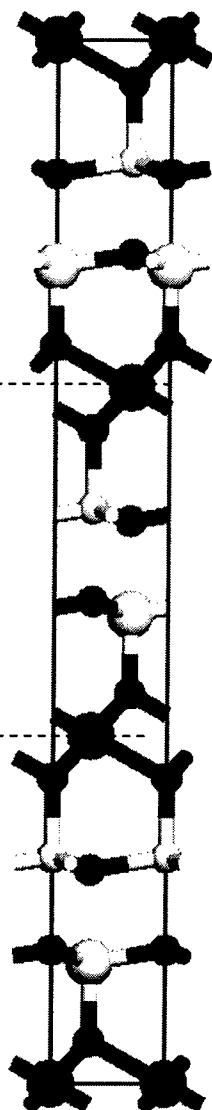
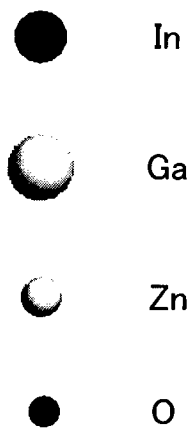
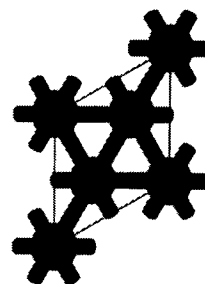
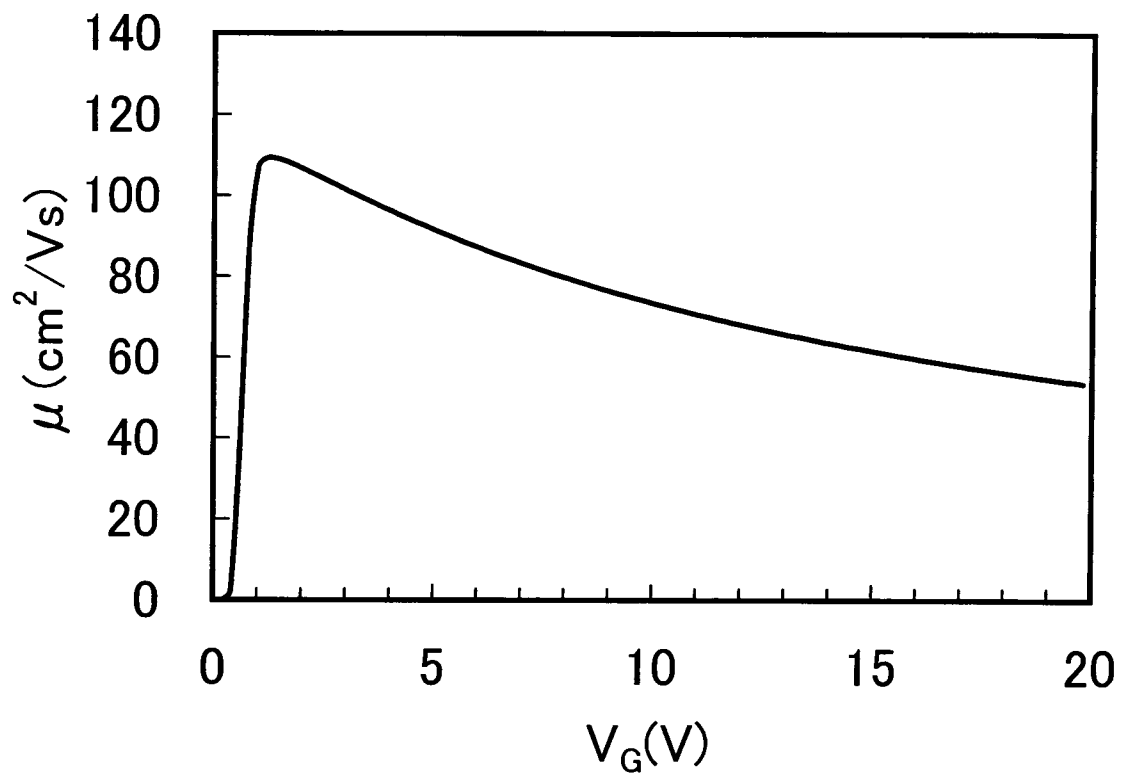


FIG. 18C



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FIG. 19



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FIG. 20A

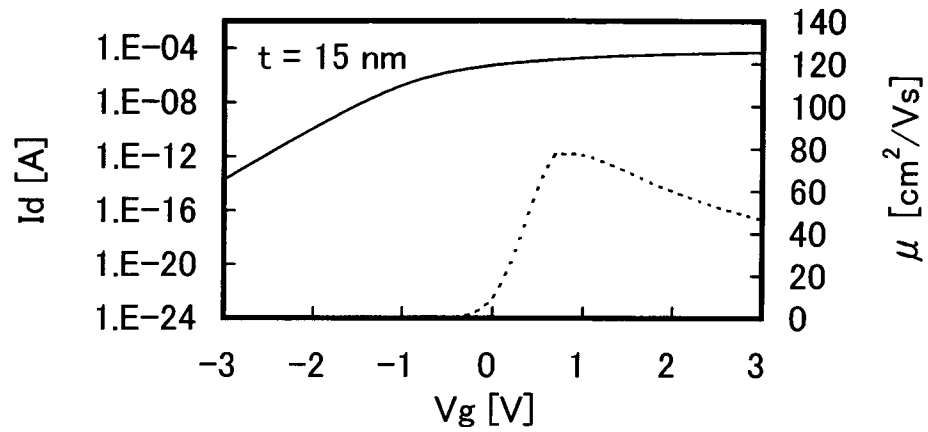


FIG. 20B

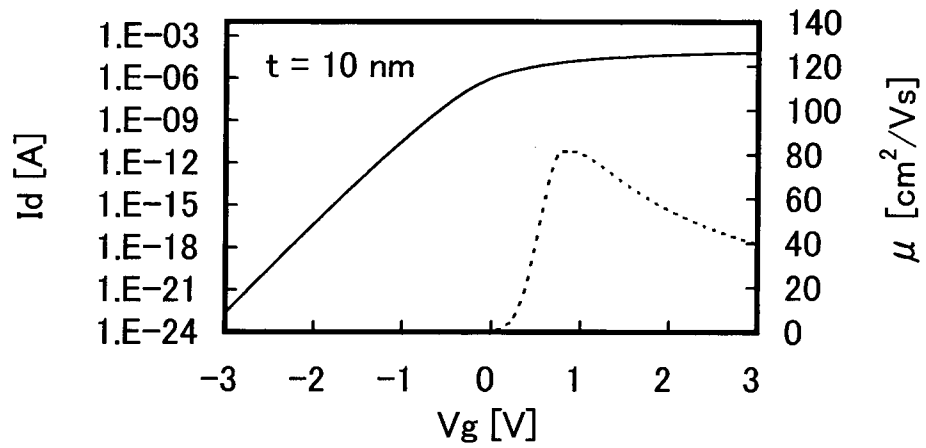


FIG. 20C

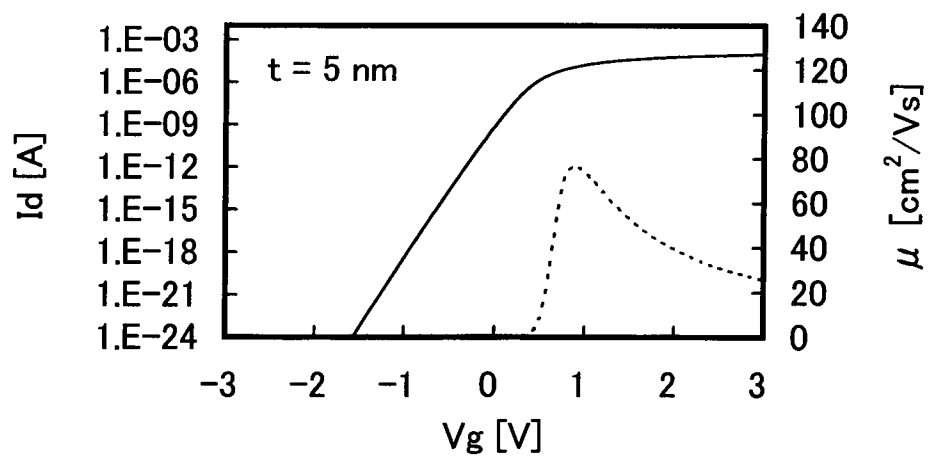


FIG. 21A

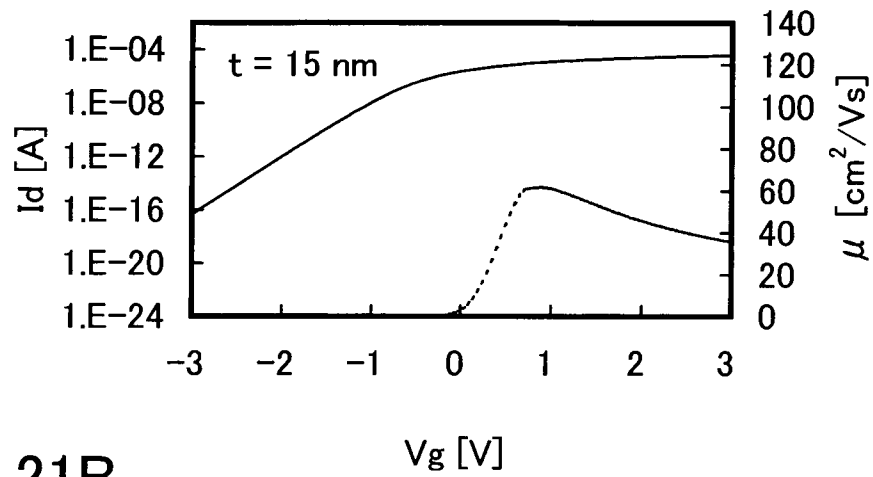


FIG. 21B

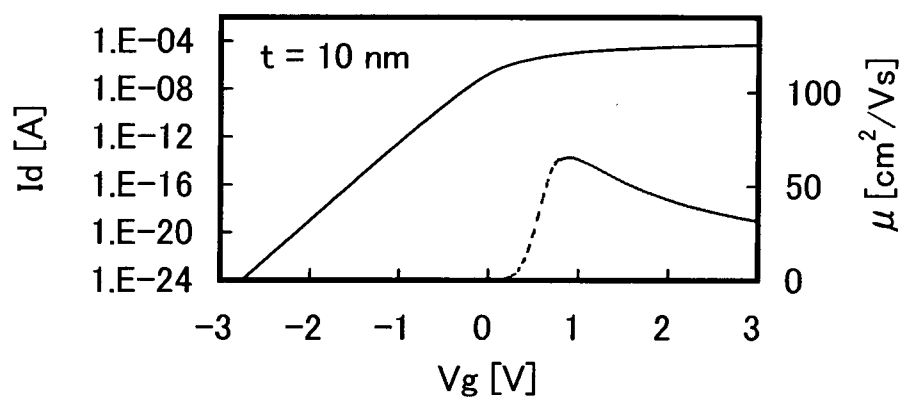
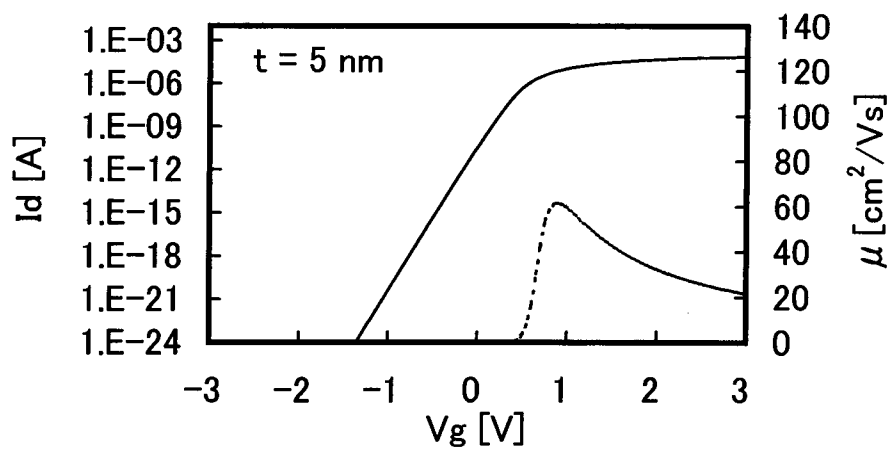


FIG. 21C



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FIG. 22A

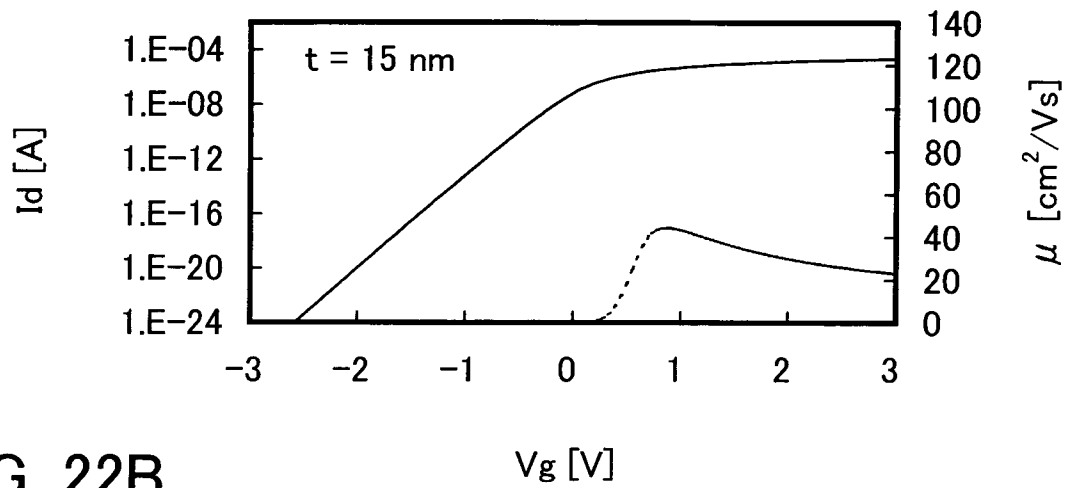


FIG. 22B

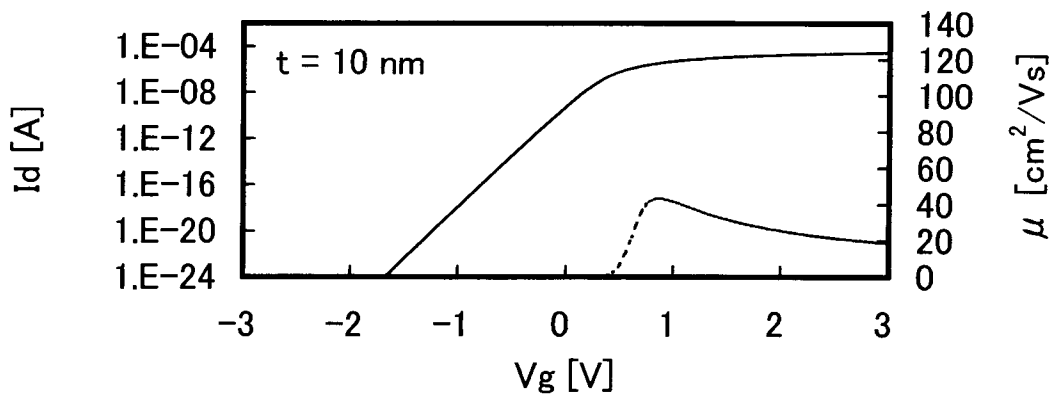


FIG. 22C

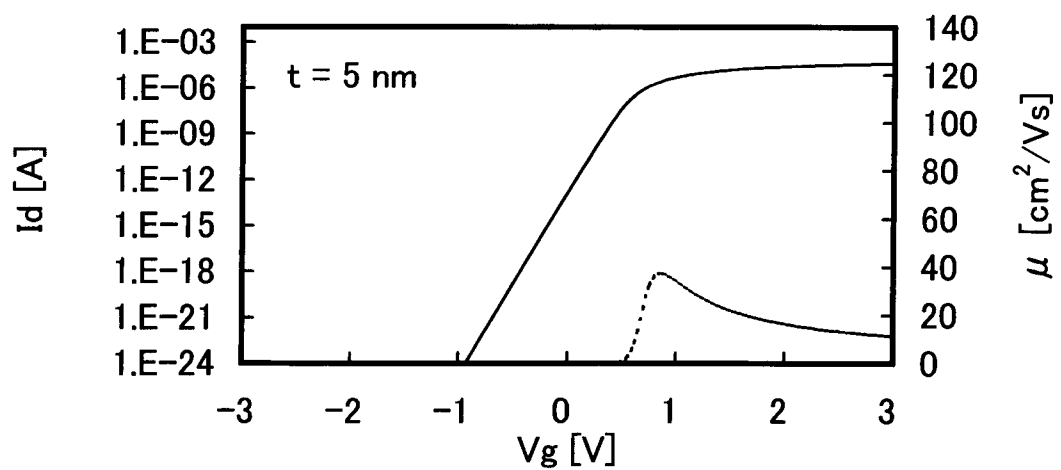


FIG. 23A

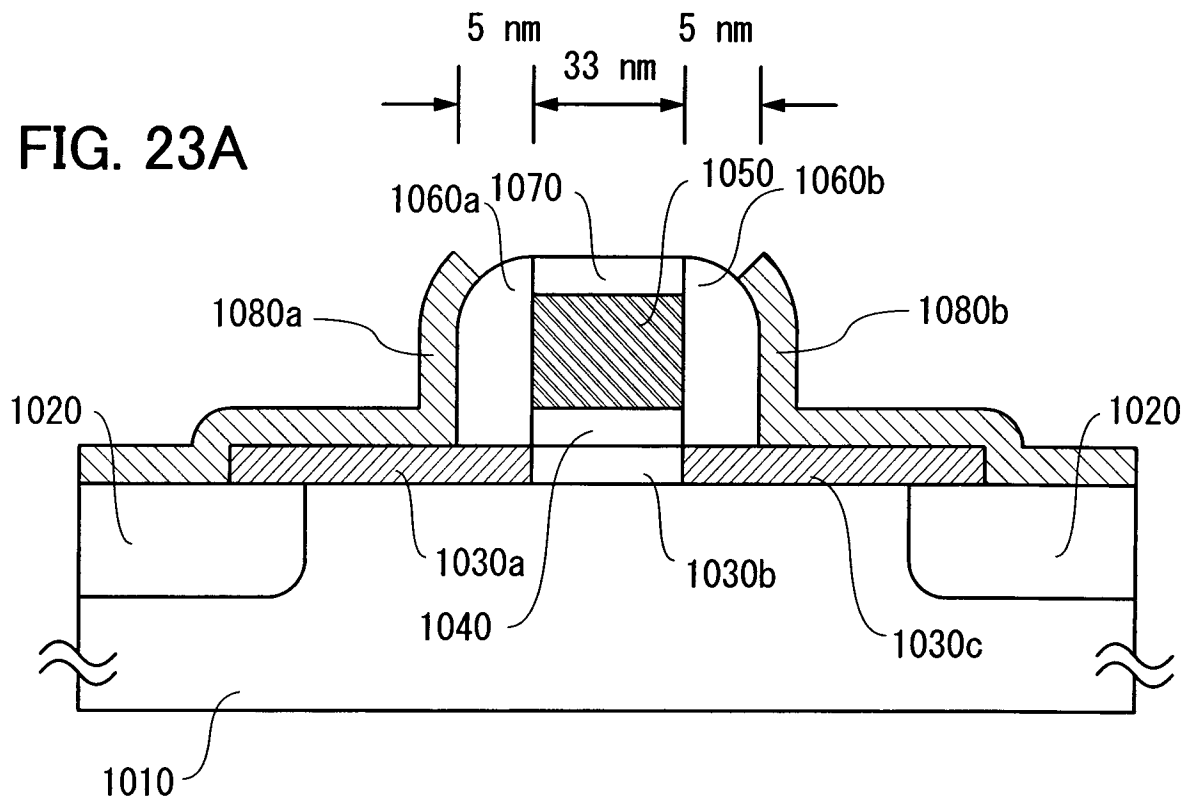
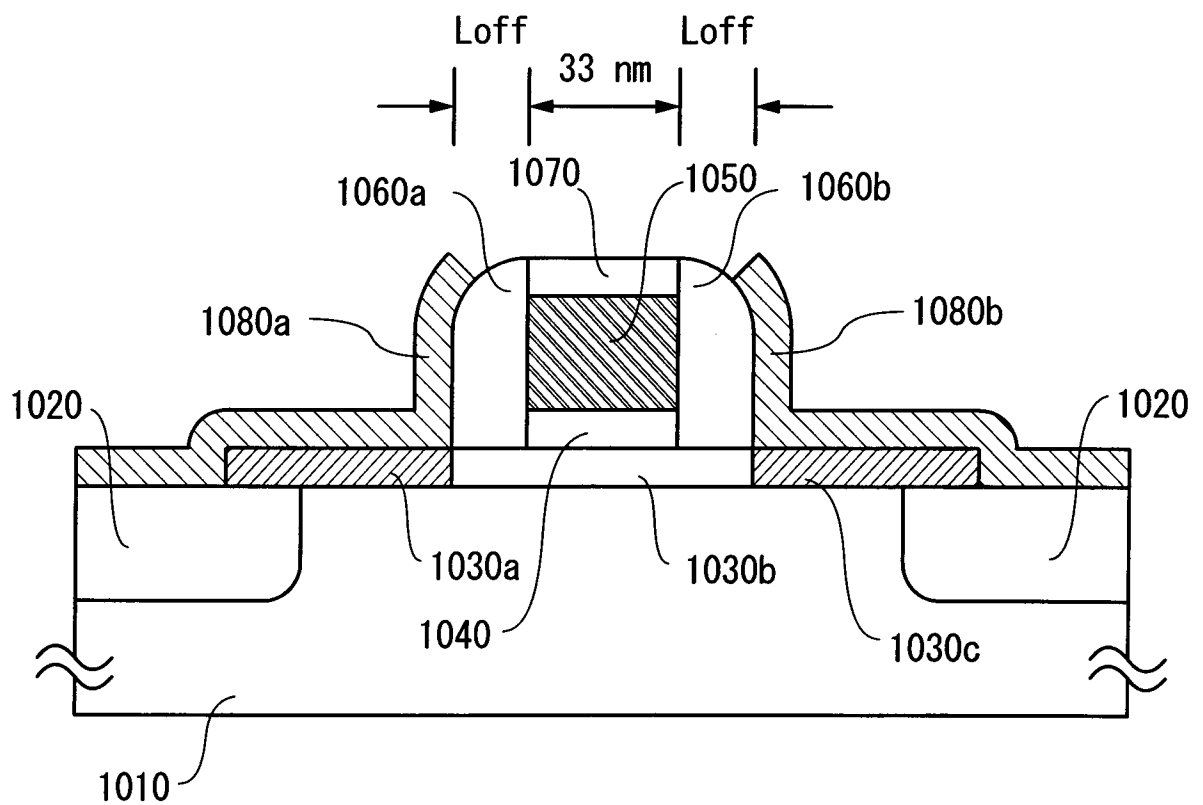


FIG. 23B



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FIG. 24A

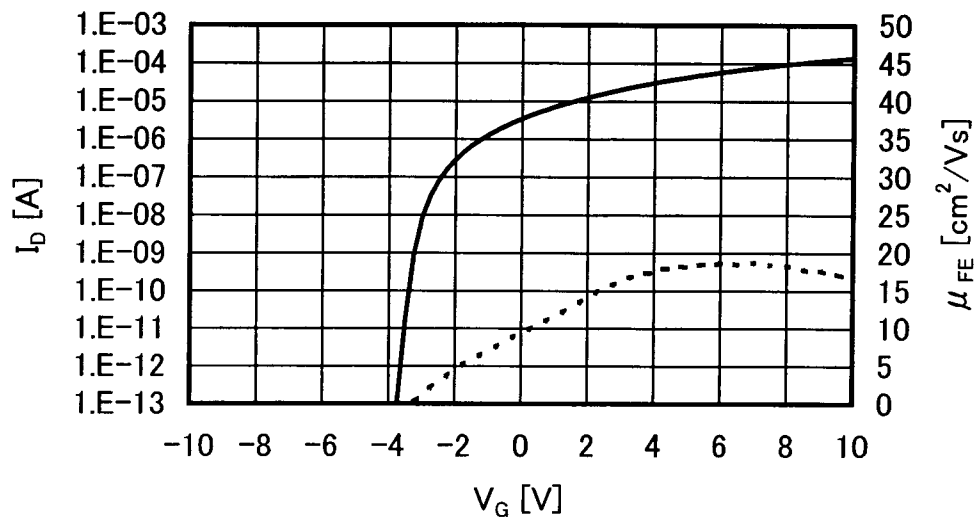


FIG. 24B

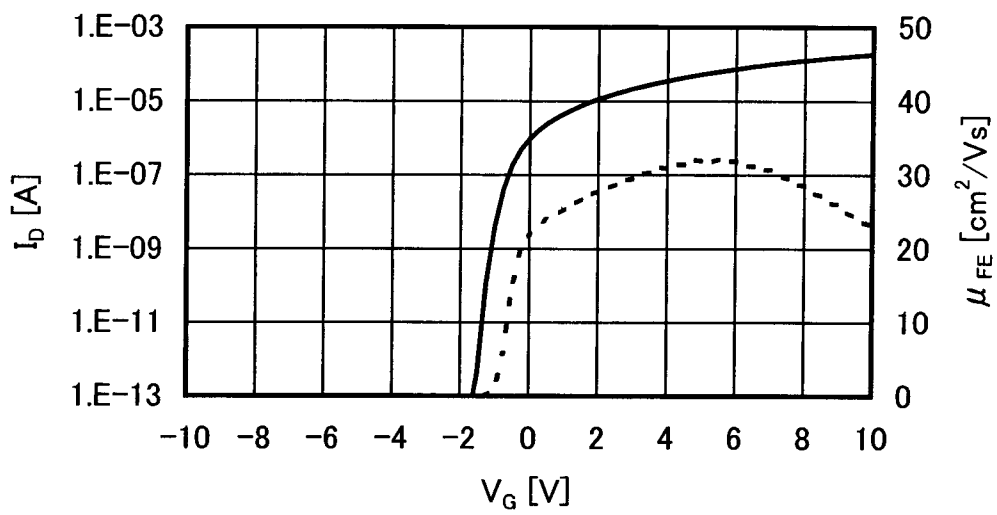
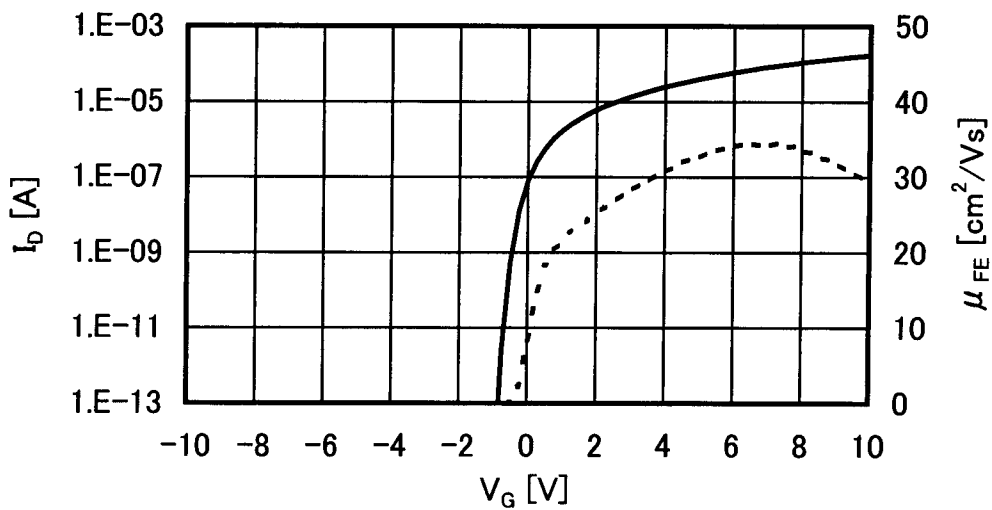


FIG. 24C



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FIG. 25A

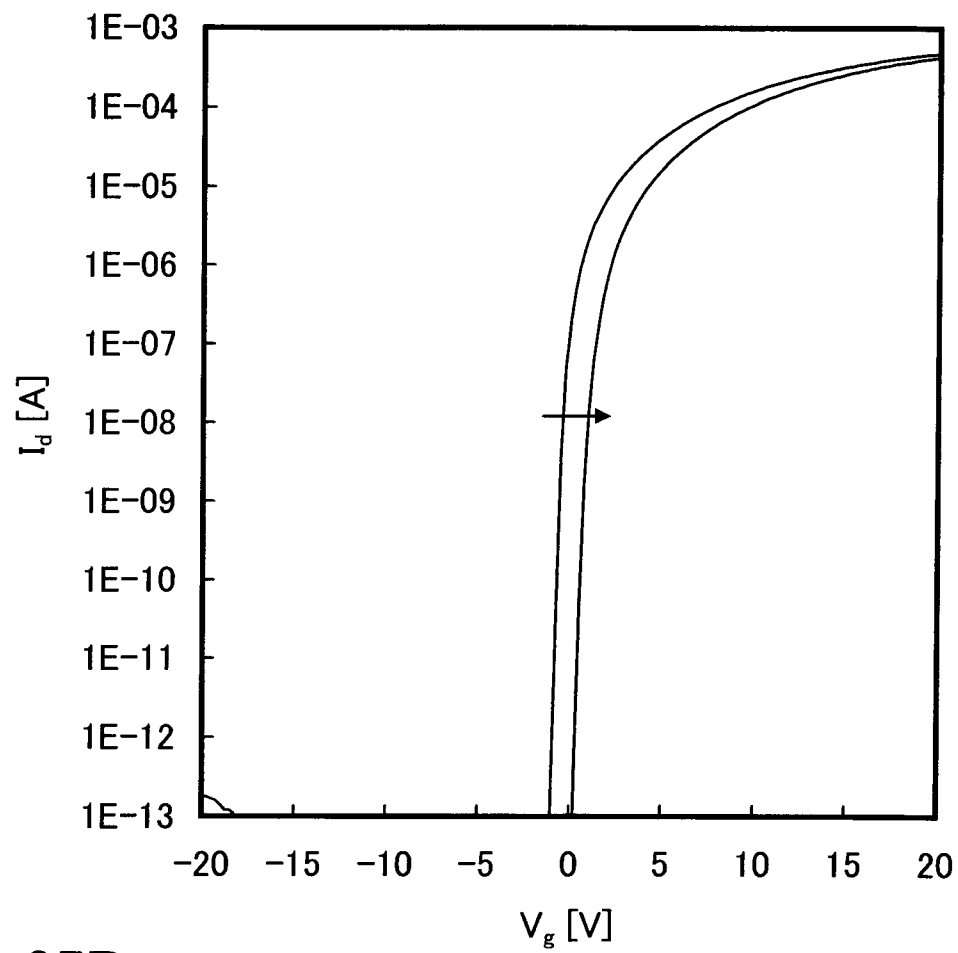


FIG. 25B

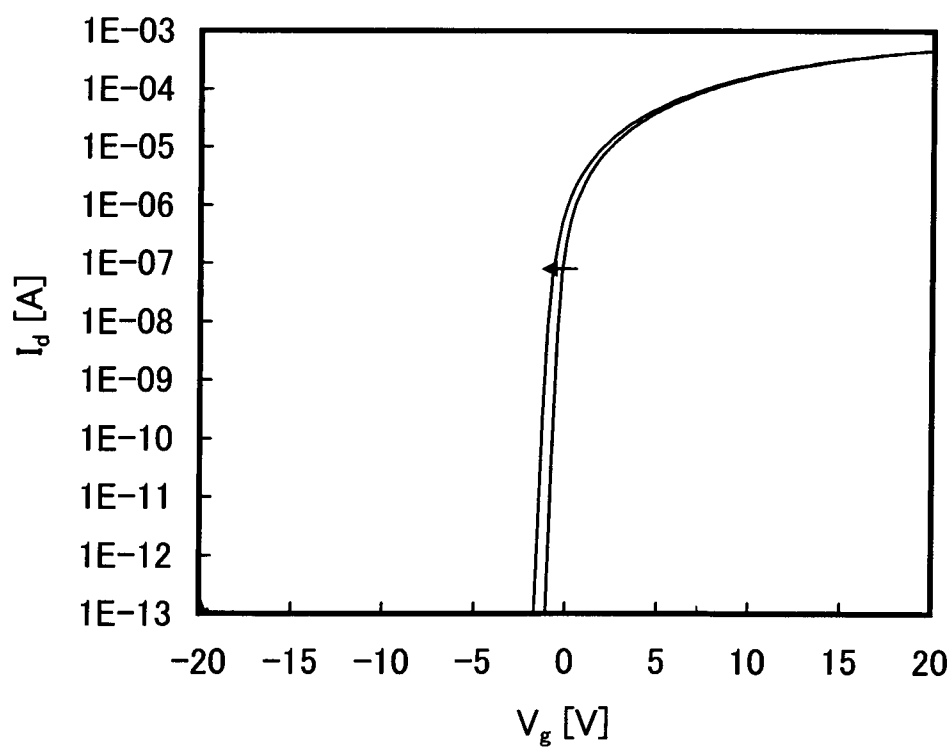


FIG. 26A

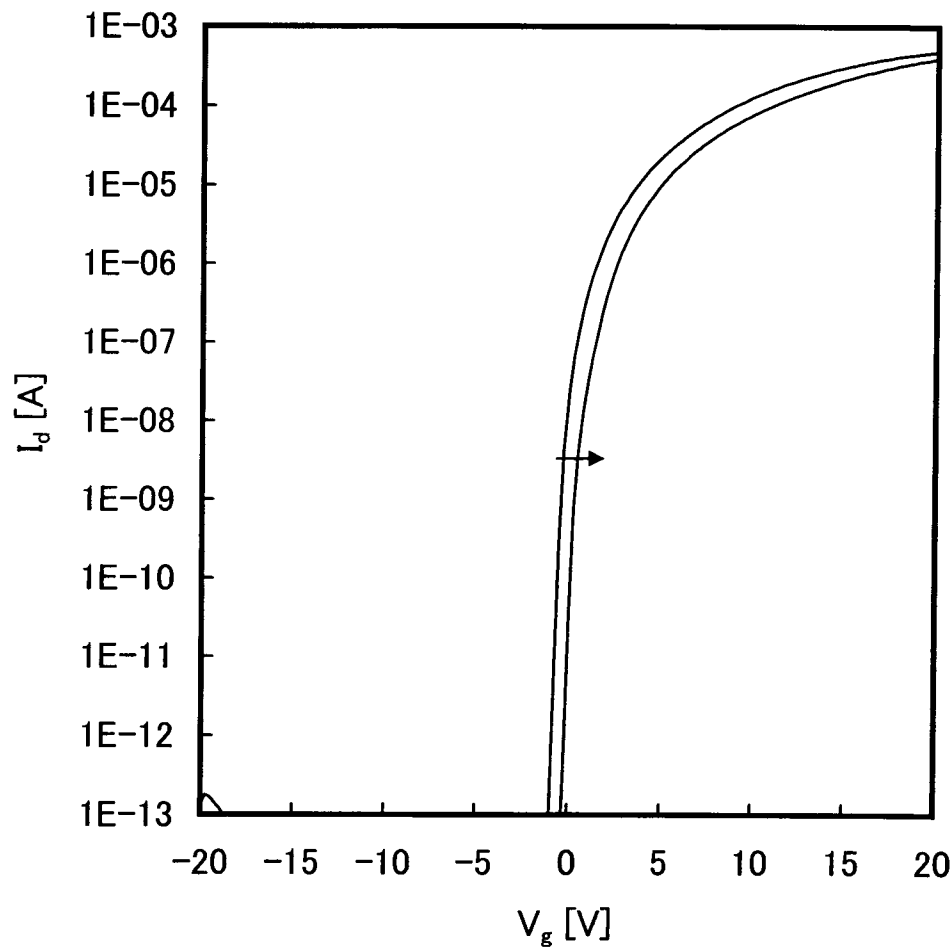
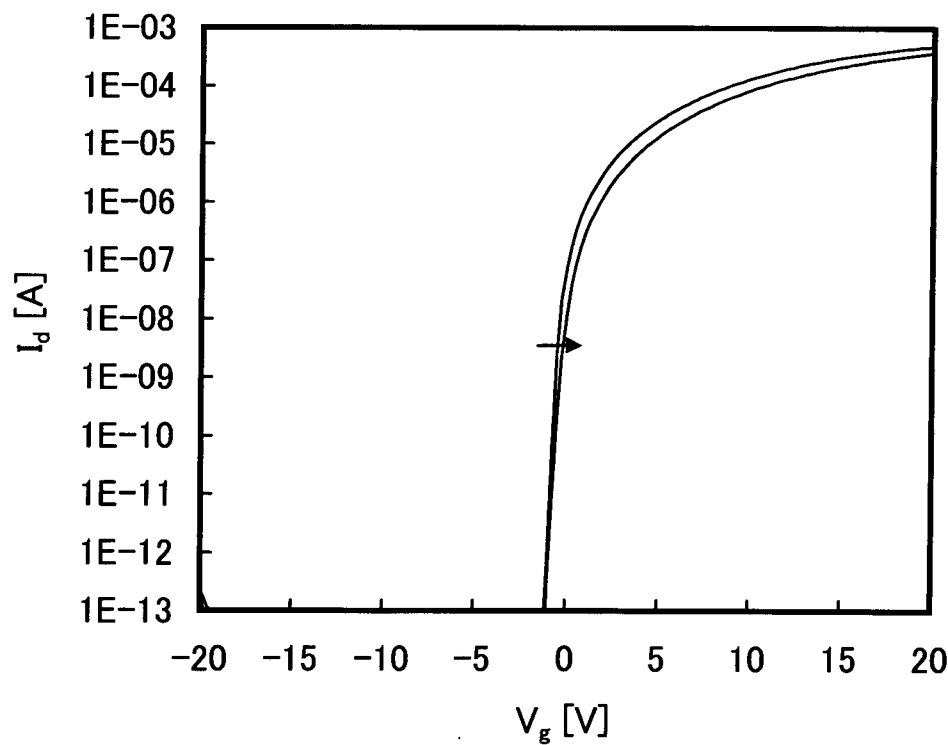
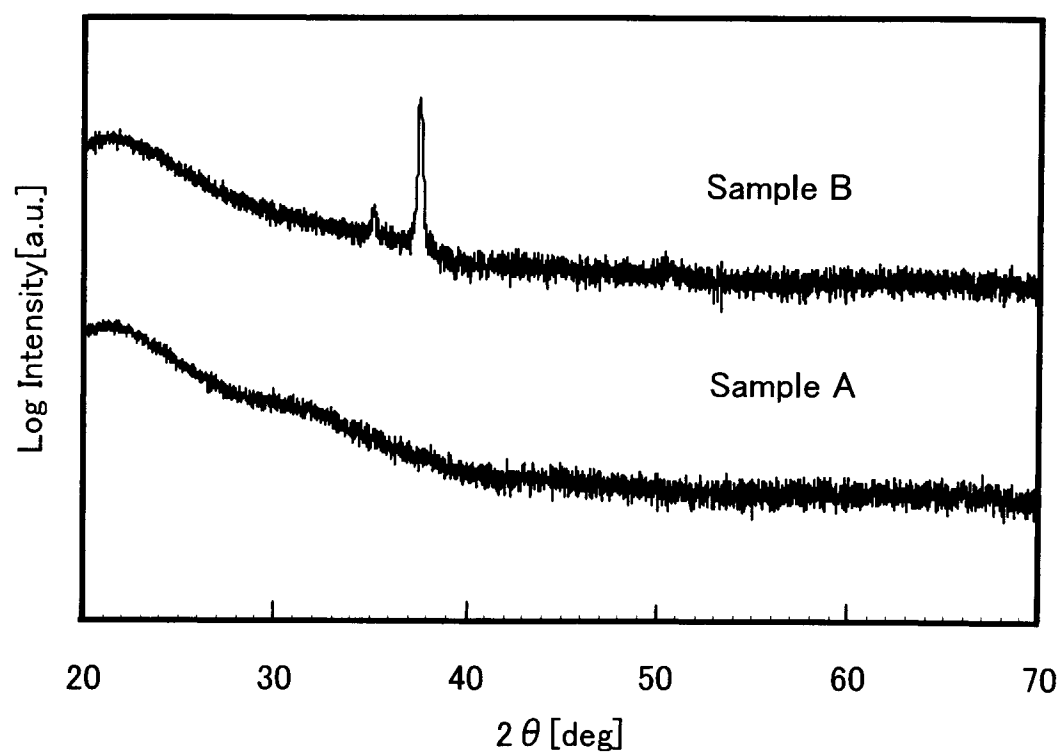


FIG. 26B



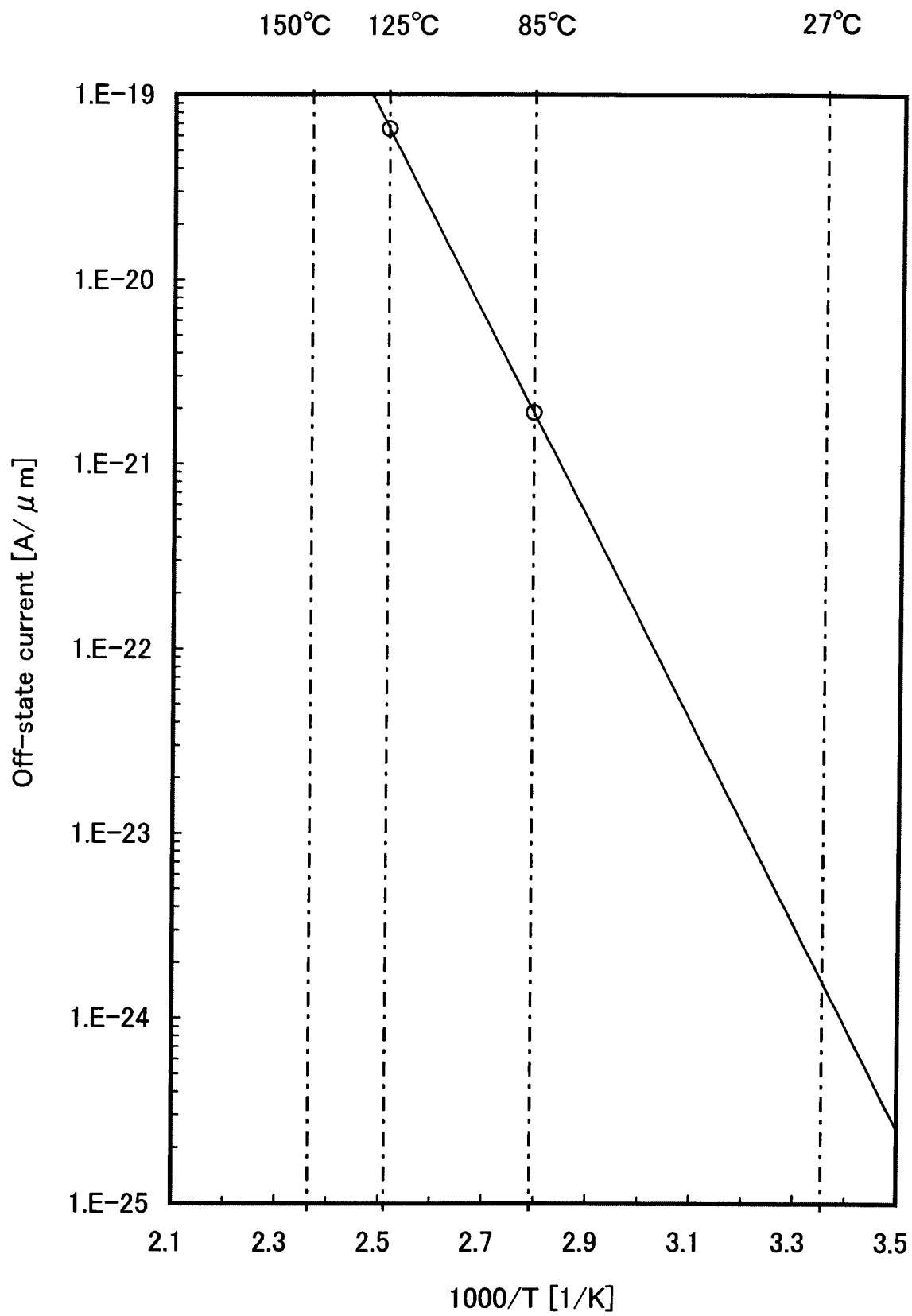
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FIG. 27



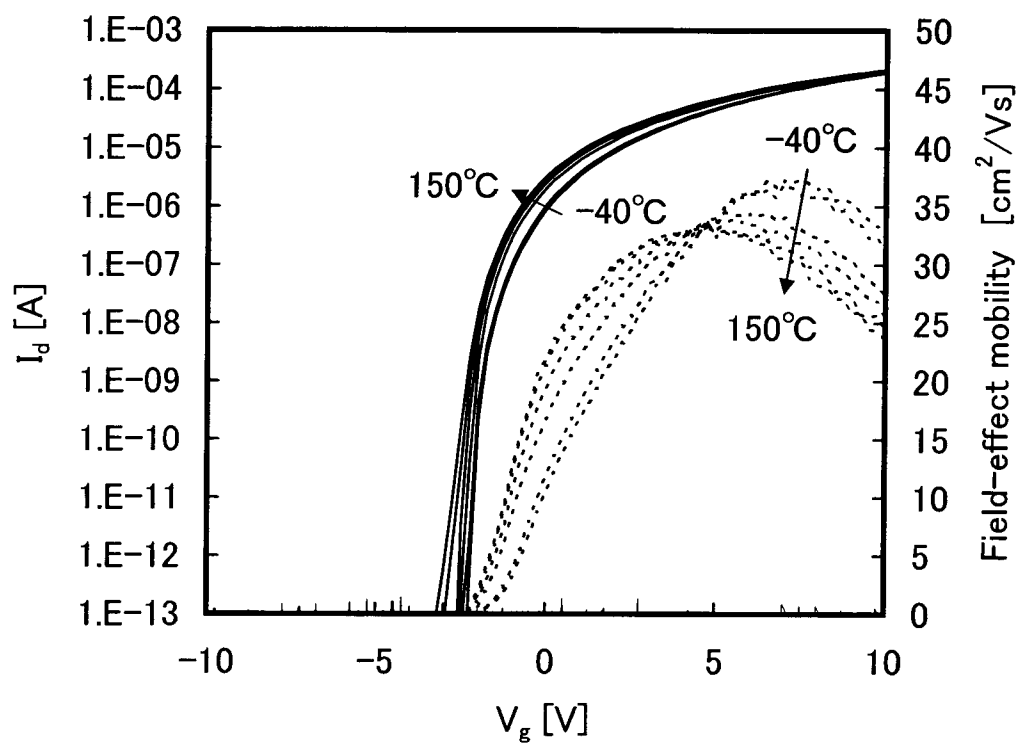
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FIG. 28



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FIG. 29



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FIG. 30A

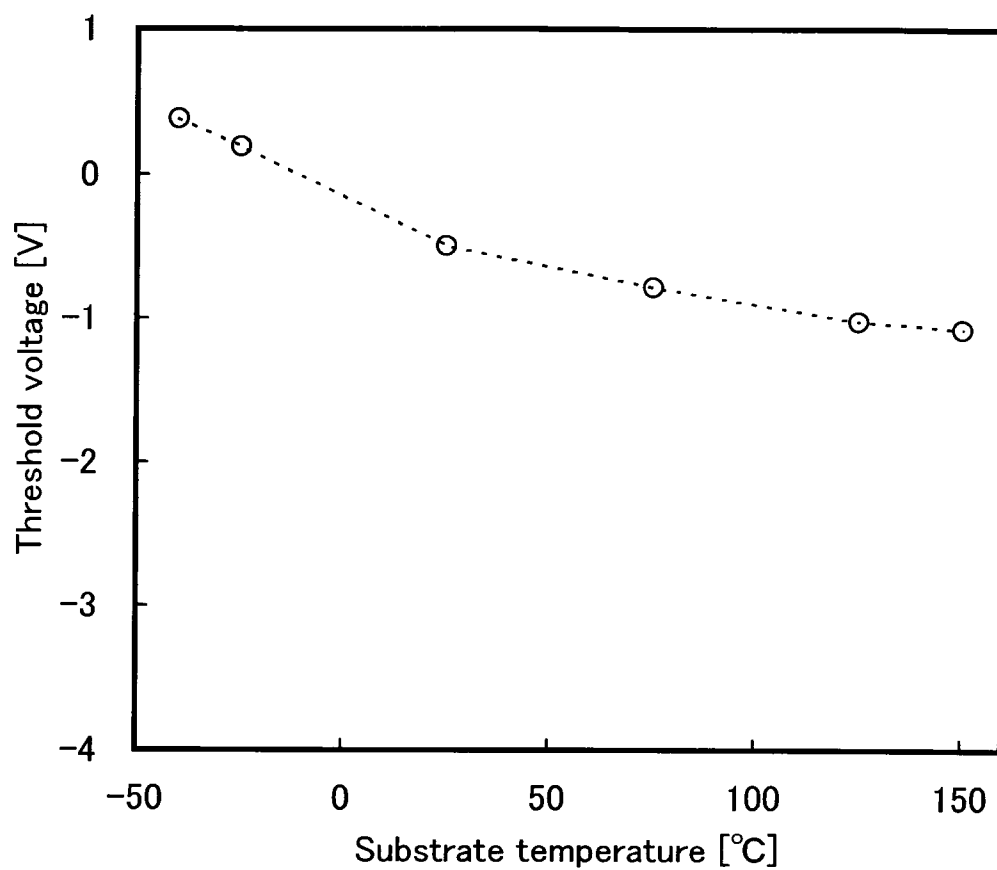
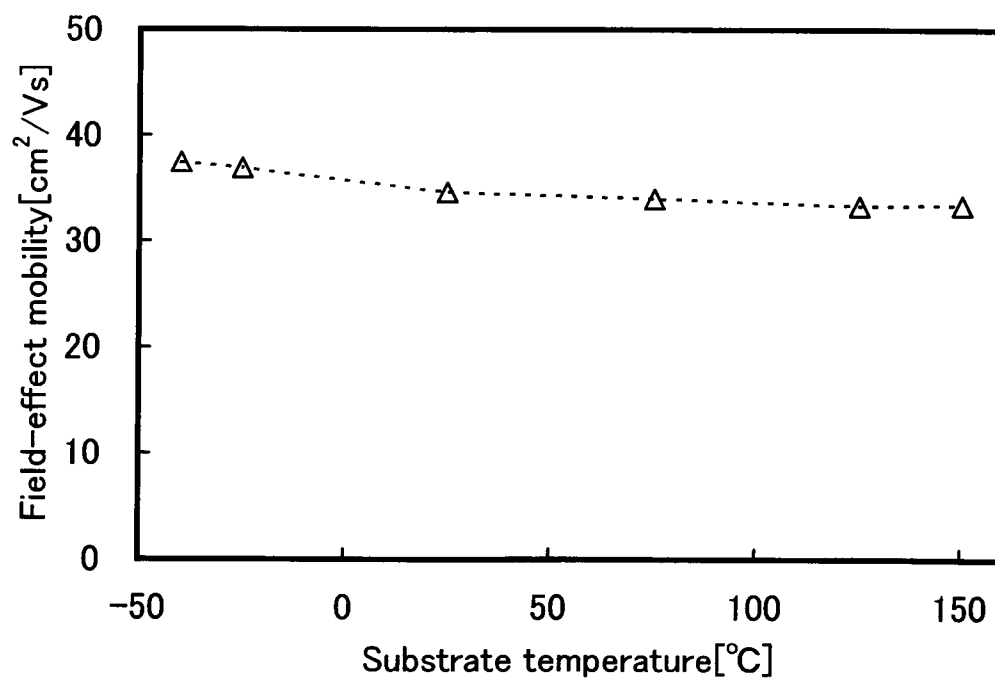


FIG. 30B



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FIG. 31A

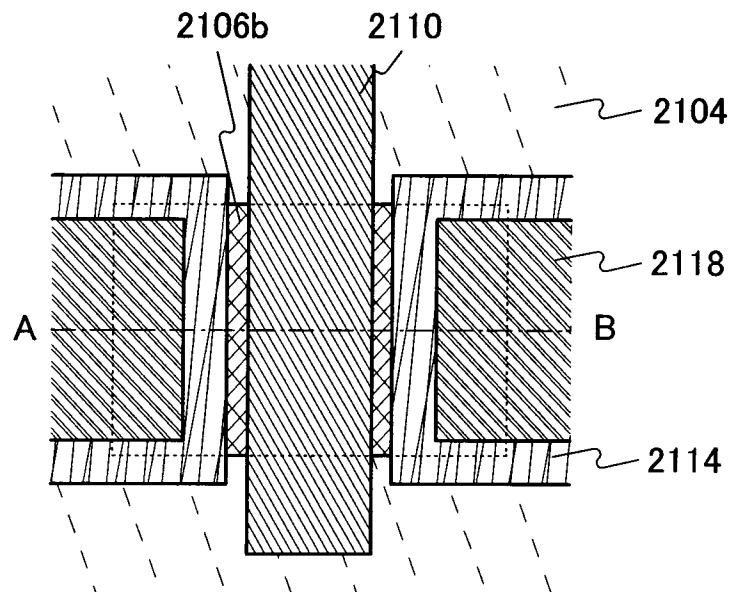


FIG. 31B

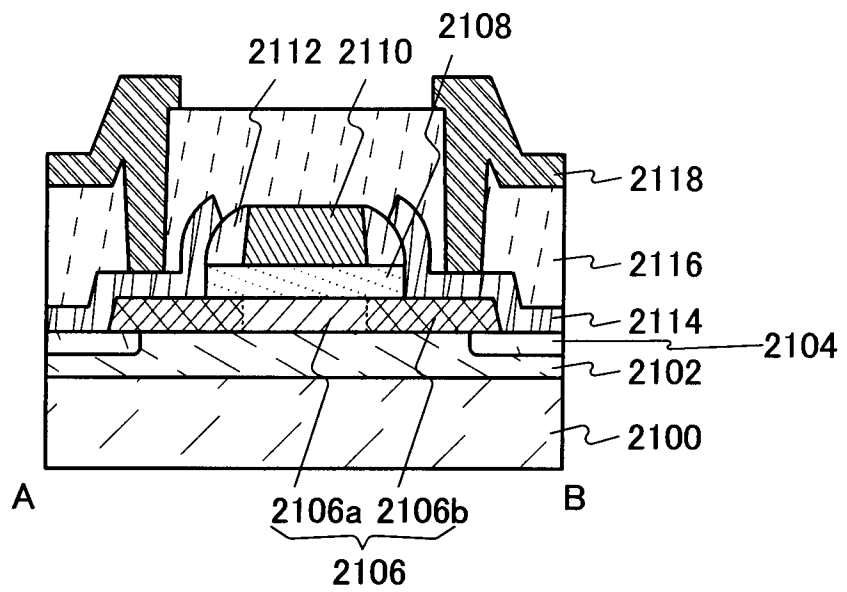


FIG. 32A

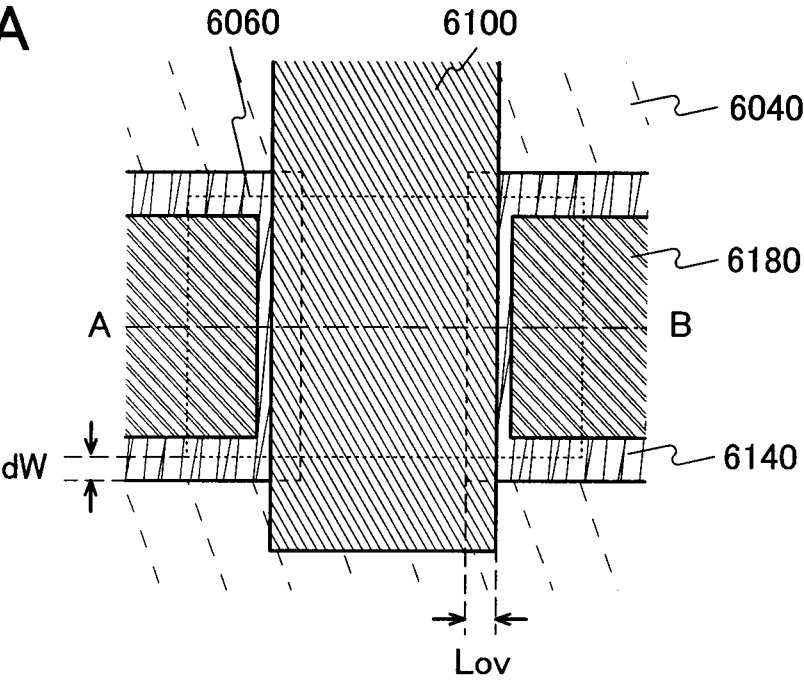
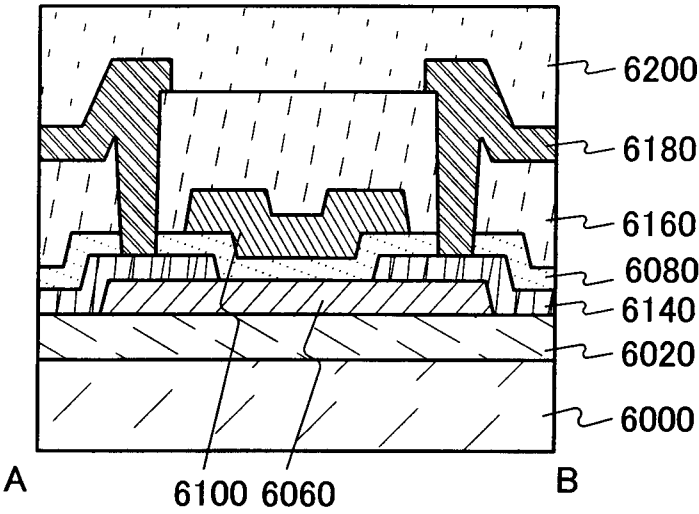


FIG. 32B



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/077107

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H04N5/376 (2011.01) i, H01L27/146 (2006.01) i, H01L29/786 (2006.01) i,
H04N5/374 (2011.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H04N5/376, H01L27/146, H01L29/786, H04N5/374

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2012
Registered utility model specifications of Japan 1996-2012
Published registered utility model applications of Japan 1994-2012

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 61-148693 A (Hitachi, Ltd.) 1986.07.07, page 1-2, Fig3(c) (No Family)	1-22
X	JP 2007-052291 A (Sony Corporation) 2007.03.01, paragraph 23-37, Fig.4 (No Family)	1-22
A	JP 2010-011426 A (Canon Inc.) 2010.01.14, Full text, all drawings (No Family)	1-22
A	JP 2000-232348 A (Kawasaki Steel Corporation) 2000.08.22, Full text, all drawings (No Family)	1-22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

10.01.2012

Date of mailing of the international search report

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