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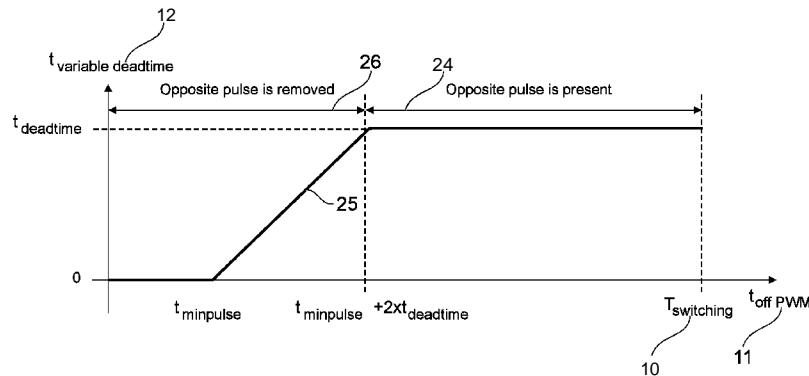


Fig. 7

(57) **Abstract:** The present disclosure relates to a controller, a circuit and method for controlling a power converter using pulse width modulation (PWM). At least one logic block (13, 15, 16) of the controller is configured to remove a command (4) which is configured to control the other power semiconductor switch (2) in a half-bridge (1,2) so that the other power semiconductor switch (2) remains in a non-conductive state while an antiparallel diode (6) allows an electric current (5) to pass in one direction, called the diode's forward direction, while blocking current in the opposite direction. In case the diode (6) is conducting instead of the other power semiconductor switch during the duration of the state of the command, the switching command (4) for the latter is omitted. The controller is further configured to modify the dead time interval (Tdead) between switching from the power semiconductor switch (3) to another power semiconductor switch (4) or vice versa in order to avoid a discontinuity in the transfer function (25).

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## CONVERTER CONTROLLER WITH HALF BRIDGE ADAPTIVE DEAD TIME CIRCUIT AND METHOD

Technical Field

5 The present disclosure relates to a controller for a power converter. More particularly, the present disclosure relates to a controller, a circuit and method for controlling the power converter using pulse width modulation (PWM).

10 Background

The state of the art in power converters provides an adjustable voltage and frequency to the output through a pulse width modulated (PWM, pulse width modulation) voltage source inverter drive. Power converters can be 15 used in uninterruptible power supplies (UPS), electric motors, etc. The PWM command is used in the power converter for controlling power to electrical devices, made practical by modern electronic power switches. The duty cycle of a switch (ratio of on-time to total cycle time) is varied to achieve a desired average output voltage, current etc., when averaged 20 over time.

A typical power converter is a switching power converter. It has two or more power semiconductor devices such as power semiconductor switches. The power semiconductor switches can, for example, be 25 implemented by insulated-gate bipolar transistors (IGBT). A simple logical error - turning a transistor on at the wrong instant - can cause catastrophic failure in the right or wrong circumstances. When the state of the transistor must change due to requested PWM, the conducting transistor is turned off. Then, after a delay (called dead time), the other 30 transistor is turned on. The delay is added to ensure that there is no

possibility of both transistors conducting at the same time. Dead time is necessary to prevent short circuit of the power supply of the switching power converter.

5 Although the dead time is short, it causes deviation from the desired output. The deviations result in reduced output voltage, distorted machine currents, and torque pulsations. Dead time in the switching output stage also causes nonlinearity in the power circuit transfer function that may be difficult to remove.

10 Due to the dead time, it is also never possible to reach maximum modulation depth. The maximum actual duty cycle of PWM is limited by the dead time between the power converter commands. Dead time limits the time that the power converter can spend in an active state as a fraction 15 of the total time under consideration. System requirements of the power converter for the minimum allowed command pulse also limits the duty cycle. Due to these constraints, the capacity of the power converter is not fully used. For example, an inverter having a 15 kHz switching frequency, 2  $\mu$ s dead time, and 2  $\mu$ s minimum pulse can reach a maximal modulation 20 depth of only 94%. 6% of the theoretical modulation range is lost, which translates into a 6% loss of efficiency. This causes loss in maximum reachable output voltage mostly and additionally negative effect on output voltage waveform in closed loop system, for example due to an earlier saturation of the PWM command.

25 A known solution to improve the loss and performance has been to increase the DC bus voltage to compensate loss of modulation depth. This, however, increases the cost of the power converter system. The present invention is directed to overcoming one or more of the 30 problems as set forth above.

Summary of the Invention

In one aspect, the present disclosure is directed to a controller for a power converter using pulse width modulation. The controller comprises at least one control module configured to cause the controller to generate a command for switching a power semiconductor switch between a conductive and non-conductive state. The controller is configured to generate a delay interval between switching from the power semiconductor switch to another power semiconductor switch. The controller is further configured to remove the command configured to control the power semiconductor switch so that the power semiconductor switch remains in a non-conductive state. Now a diode allows an electric current to pass the power semiconductor switch in one direction, while blocking current in the opposite direction. The controller is further configured to modify the delay interval between switching from the power semiconductor switch to said another power semiconductor switch.

In another aspect, the present disclosure is directed to a circuit, comprising the controller, wherein the at least one circuit block comprises the at least one logic module.

In another aspect, the present disclosure is directed to a method for controlling a power converter using pulse width modulation. The method comprises generating a command for switching a power semiconductor switch between a conductive and non-conductive state. The method comprises generating a delay interval between switching from the power semiconductor switch to another power semiconductor switch. The method further comprises removing the command configured to control the power semiconductor switch so that the power semiconductor switch remains in

an open state. The method still allows an electric current to pass in one direction, while blocking current in the opposite direction. The method also comprises modifying the delay interval between switching from the power semiconductor switch to said another power semiconductor switch.

5

At least one of the above aspects provides one or more solutions to the problems and disadvantages with the background art. Other technical advantages of the present disclosure will be readily apparent to one skilled in the art from the following description and claims. Various embodiments 10 of the present application obtain only a subset of the advantages set forth. No one advantage is critical to the embodiments. Any claimed embodiment may be technically combined with any other claimed embodiment(s).

Brief Description of the Drawings

The accompanying drawings illustrate exemplary embodiments of the disclosure, and together with the general description given above and the 5 detailed description of the embodiments given below, serve to explain, by way of example, the principles of the disclosure.

FIG. 1 shows a circuit diagram of a power converter, wherein a top command is driven according to an exemplary embodiment of the present disclosure;

10 FIG. 2 shows a circuit diagram of the power converter, during dead time according to an exemplary embodiment of the present disclosure;

FIG. 3 shows the circuit diagram of a power converter controller, wherein a bottom command is driven according to an exemplary embodiment of the present disclosure;

15 FIG. 4 is a waveform diagram illustrating operation of a controller for a power converter, wherein the dead time is applied, according to an exemplary embodiment of the present disclosure;

FIG. 5 shows a state diagram of a controller for a power converter, wherein the controller removes a command of a power semiconductor 20 device according to an exemplary embodiment of the present disclosure;

FIG. 6 shows a state diagram of a controller for a power converter, wherein the controller removes a command of a power semiconductor device and variable dead time is applied according to an exemplary embodiment of the present disclosure;

25 FIG. 7 shows a function of the variable dead time according to an exemplary embodiment of the present disclosure;

FIG. 8 shows a block diagram of a controller for a power converter according to an exemplary embodiment of the present disclosure; and

FIG. 9 illustrates a transfer function of the controller according to 30 exemplary embodiments of the present disclosure.

Detailed Description

An exemplary embodiment of the present disclosure provides a controller, 5 a circuit and a method for controlling a power converter, the power converter using pulse width modulation (PWM). The controller comprises one or more logic block configured to cause the controller to generate a command for switching a power semiconductor switch between a conductive and non-conductive state. The controller is configured to 10 generate a delay interval between switching from the power semiconductor switch to another power semiconductor switch. The controller is further configured to remove a command which is configured to control a power semiconductor switch so that the power semiconductor switch remains in a non-conductive state. However a diode allows an 15 electric current to pass the power semiconductor switch in one direction, called the diode's forward direction, while blocking current in the opposite direction. The controller is further configured to modify the interval between switching from the power semiconductor switch to another power semiconductor switch. The controller removes the power semiconductor 20 command which is not applicable because the diode is used instead of the power semiconductor switch to conduct current during the duration of the state of the command. The interval between switching from the power semiconductor switch to another power semiconductor switch is also modified. The interval can be removed or reduced. As a result, duty cycle 25 and effectiveness of the power converter can be improved due to better control because unnecessary dead time delays, which decrease the duty cycle, can be mitigated.

FIG. 1 shows a circuit diagram of a power converter, wherein top 30 command is driven according to an exemplary embodiment of the present

disclosure. Figure 1 illustrates an operation of power converter driven with a PWM modulation. Figure 1 assumes that the current stays positive during all of the switching period. The power converter comprises two power semiconductor switches 1,2. The power semiconductor switches 5 1,2 may be, for example, power MOSFETs or insulated gate bipolar transistors (IGBTs). A first power semiconductor switch 1 operates by top command 3 (and may be alternatively referred to as top power semiconductor switch). A second power semiconductor switch 2 operates by bottom command (and may be alternatively referred to as bottom power semiconductor switch). A top command 3 is in active state, i.e. on, commanding the power semiconductor switch 1. The power semiconductor switch 1 is accordingly closed and on (in an active state) and conducting the current. A current flow 5 is shown by the dashed line in the Figure 1. The bottom command 4 is off and in non-active state. 10 Accordingly the power semiconductor switch 2 is open and off (in a non-active state) and not conducting current. 15

FIG. 2 shows a circuit diagram of a power converter, wherein dead time is active according to an exemplary embodiment of the present disclosure. 20 The time delay taking place between switching the power semiconductor switches 1,2 is called the dead time. The dead time is required between each state transition: From top to bottom, and from bottom to top. The dead time prevents any cross conduction of the power converter, such as a DC short circuit of the DC voltage, caused by the two power semiconductor switches 1,2 being closed at the same time. The cross conduction may lead to a destruction of the IGBT bridge. In Figure 2, top command 3 is off so that the power semiconductor switch 1 is open. The bottom command 4 is off and the power semiconductor switch 2 is therefore not driven. There is therefore no specific command for the dead 25 time. However, the current can flow only through a diode 6 as shown by 30

the current flow 5. The diode 6 can be a free wheeling diode or a flyback diode. In the controller the diode 6 allows an electric current to pass the power semiconductor switch 2 in one direction, which may be also called the diode's forward direction, while blocking current in the opposite 5 direction. The current can flow through the diode 6 which is parallel coupled with respect to the power semiconductor switch 2. The current flows when the current stays positive during the switching period.

FIG. 3 shows a circuit diagram of a power converter controller, wherein the 10 bottom command 4 is driven according to an exemplary embodiment of the present disclosure. Bottom command 4 is in active state, i.e. on. The power semiconductor switch 2, for example the bottom IGBT, is driven. The switch 2 cannot close. The current continues to flow through the diode 6 and the current path 5 is the same as in the example of Figure 2. This 15 fact can be utilized when removing the command for the power semiconductor switch that does not conduct current. In the example of Figure 3, top command 3 is off so that the power semiconductor device 1, for example top IGBT, is open and non-active.

20 Referring to Figure 4 shows a waveform diagram illustrating operation of a controller for a power converter, wherein the dead time is applied. Figure 4 shows a desired PWM waveform 7. The desired PWM 7 illustrates PWM out that is desired to be output from the power controller. The controller receives the PWM request 7 so as to control the power converter to create 25 requested PWM power output. State diagram of the top command 3 and bottom command 4 are also shown. Dead time 8 (alternatively referred to as duration of dead time or delay between switching from first to second power semiconductor switch and *vice versa*) is shown and can be also referred to as  $t_{deadtime}$ . Minimal pulse 9 illustrates minimum allowed pulse 30  $t_{minpulse}$ . It is the minimum duration of the power semiconductor switch

command and represents a standard security measure to safe guard against the power semiconductor switch having a system fail due to too short a pulse. A switching period 10 or  $T_{switching}$  is the period of the switching cycle.  $T_{offMin}$  11 is the actual duration when the power converter 5 is in an off or non-active state.

According to the Figures 1, 2 and 3 showing the current flow 5 in three possible state of the power converter (top command, bottom command, and dead time), the off time duration corresponds to the following function:

10

$$t_{offmin} = t_{minpulse} + 2 \times t_{deadtime} .$$

The maximum actual duty cycle (ratio of duration of active state to the total period) is then

15

$$\alpha = \frac{T_{switching} - t_{offMin}}{T_{switching}} .$$

For example with  $T_{switching} = 66.6 \mu\text{s}$ ,  $T_{deadtime} = 2 \mu\text{s}$  and  $T_{minpulse} = 2 \mu\text{s}$ , a 20 = 91 %. The output voltage may therefore reach only 91 % of input DC voltage.

FIG. 5 shows a state diagram of a controller for a power converter, wherein the controller removes a bottom command 4 of a power semiconductor switch 2 according to an exemplary embodiment of the 25 present disclosure.

According to the circuit diagram in Figures 1, 2 and 3, the second power semiconductor switch 2, for example the bottom IGBT, can never conduct current when  $I_{ac}$  (shown in Figures 1, 2 and 3) output current is positive.

The IGBT bridge is symmetric, so the same condition can be assumed with a negative current: in this case, the first power semiconductor switch 1, for example top IGBT, can never conduct current when Iac output 5 current is negative.

Referring back to Figure 5 when the controller removes the opposite power semiconductor switch command during the time when it cannot conduct current (removing the command 4 when the switch 2 does not 10 conduct current),  $t_{offMin}$  11 can now be  $t_{offMin} = t_{minPulse}$ , which is also shown on Figure 5.

The dead time and corresponding dead band may not be useful, especially when operating at high duty cycle. A power semiconductor 15 switch 2 which is driven after the dead time will never close. The diode 6 such as the free wheeling diode conducts instead of the power semiconductor switch 2.

Accordingly, the controller is configured to remove the power 20 semiconductor switch command. Additionally the corresponding dead time can be removed each time this power semiconductor switch will not drive current. For example when the controller determines that Iac is positive, the controller removes the bottom command 2. The controller can also remove the corresponding dead time each time power semiconductor 25 switch 2 will not drive current. Example of this state diagram is shown in Figure 5. The top command 3 drives now power semiconductor switch 1 for the requested PWM 7.

As long as the lac current remains positive, the off time of the power semiconductor switch 1, for example top IGBT, corresponds to the conduction of the diode 6, for example a free wheeling diode.

5 The embodiment of Figure 5 produces a non linearity on the command law. Therefore the transfer function is not continuous. The non linearity is due to a significant difference of actual PWM between the state where the dead band is applied and the state where the dead band is removed.

10 Figure 6 shows a state diagram of a controller for a power converter, wherein the controller removes a command 4 of a power semiconductor switch 2 and variable dead time 12 is applied according to an exemplary embodiment of the present disclosure. The controller is configured to remove the power semiconductor switch command when it is not useful as

15 described in the embodiment of Figure 5. In the embodiment of Figure 6 the controller is configured to modify the switching interval between first power semiconductor device 1 to second power semiconductor device 2, thus modifying the dead time. The dead time is maintained even when it is not useful as described in the embodiment of Figure 5. The duration of the

20 dead time is reduced as a function of the requested duty cycle of the PWM so as to render the dead time variable dead time 12. The duration of the variable dead time 12 is accordingly reduced in relation to the off state of the requested PWM,  $W W_M$ . The reduction of the dead time has an impact on the system performance, which is the case close to the maximum and

25 minimum values.

The controller is configured to modify variable dead time 12. The variable dead time 12  $t_{\text{variabledeadtime}}$  is a function 25 (as shown in an embodiment of figure 7) of  $W W_M$  (ref. 23 in figures, off time of the requested PWM), so

30 that  $t_{\text{variabledeadtime}} = f(t_{\text{offPWVI}})$ .

The function 25 uses the parameters (as referred to in the embodiments of figures 4 and 5)

5      Rated duration of dead time:  $t_{deadtime}$ . This is the value of the dead time.

The value of the rated duration of the dead time is a constant.

Minimal allowed pulse 9:  $t_{min\ pulse}$

Switching period 10:  $T_{switching}$

10     In the embodiment of Figures 6 and 7, the function 25 can be defined as follows, and is shown in an embodiment of Figure 7:

In the interval:  $[0, t_{min\ pulse}]$  of  $t_{offPWM}$ ,  $f(t_{offPWM})$ , the function 25, is a constant equal to 0.

15

In the interval  $[t_{min\ pulse}, t_{min\ pulse} + 2 \times t_{deadtime}]$  of  $t_{offPWM}$ ,  $f(t_{offPWM})$  is a linear function as follows:

$$f(t_{offPWIVI}) = 0, \text{ When } t_{offPWM} = t_{min\ pulse}$$

20

$$f(t_{offPWIVI}) = t_{deadtime} > \text{ When } t_{offPWM} = t_{min\ pulse} + 2 \times t_{deadtime}$$

In the interval  $[t_{min\ pulse} + 2 \times t_{deadtime}, T_{switching}]$  of  $t_{offPWM}$ ,  $f(t_{offPWIVI})$  is a constant equal to  $t_{deadtime}$ .

25

Referring to figure 6, the real off time 22 applied on the IGBT command is now  $t_{offreal} = WWM + t_{var\ labiedeadtime}$ . This is continuous when WWM varies so that the system PWM command law is continuous, and the discontinuity of the embodiments of figure 5 can be removed.

30

If a smoother response is requested, the point where  $t_{\text{variabiedeadtime}} = t_{\text{deadtime}}$  can be shifted from  $t_{\text{min pulse}} + 2 \times t_{\text{deadtime}}$  to higher values in a further embodiment.

5 In a further embodiment the power semiconductor switch command, for example the opposite pulse, can be removed within interval 26. Within interval 24 the command can be maintained present. The opposite pulse can be removed when variable dead time is used, and the value of the variable dead time is lower than its rated value  $t_{\text{deadtime}}$ .

10

Embodiment of Figure 6 provides better gain and better duty cycle. This gain is very important for power converter. The embodiment therefore enables better performance or lower cost. The transfer function is continuous, so there is no risk of instability.

15

### **Current level controller**

20 The current level controller provides an activation condition of the variable dead time for the controller. The variable dead time should be associated with a removal of the opposite command, which is possible when the current stays in the same direction during the whole switching cycle.

25 In a further embodiment, the controller also comprises a current level controller 16 (for example as shown in Figure 8) to detect whether the output current  $I_{\text{ac}}$  will remain in the same direction during all of the switching period. The current level controller 16 is configured to check the current level of the output current  $I_{\text{ac}}$ . If the current exceeds a threshold, the detector alerts the controller.

The current level controller 16 determines the current threshold according to the characteristics of the power converter. It corresponds to the worst current variation during the on switching cycle at the full duty cycle.

- 5 This current threshold can be optimised in a further embodiment of the present invention at a lower value by re-calculating the next maximal current variation, which can take into account the next duty cycle to be applied to the IGBT and the inductor voltage during the next duty cycle.
- 10 The current level controller controls according to the embodiments of Figures 5 and 6. The removal of the command is enabled by the current level controller. The variable dead time is enabled by a current level controller. The current level controller is configured so that:
  - 15 • If lac is greater than the removal threshold, the bottom power semiconductor switch command 4 removal is enabled and additionally the variable dead time is enabled,
  - 20 • If lac is less than the removal threshold, the top power semiconductor switch command 3 removal is enabled and additionally the variable dead time is enabled.

For example according to the embodiment of Figure 5 when current is below the removal threshold, the dead time may be applied, and real off state duration of the top power semiconductor switch is

$$t_{offReal} = t_{offPWM} + t_{deadtime}$$

When the current exceeds the threshold, dead time is not applied and the controller may remove it. The real off state duration of the top power semiconductor switch is  $t_{offReai} = t_{offP}WM$

5     Figure 8 shows a block diagram of a controller for a power converter according to an exemplary embodiment of the present disclosure. The controller comprises at least one logic module or block, which is configured to perform the operations and functions as described in embodiments of Figures 1, 2, 3, 4, 5 and 6. For example one or more logic

10    blocks are configured to remove the corresponding power semiconductor switch command, and apply a dead time corresponding to the received indication of input dead time duration. The controller comprises a command generator module 15. The command generator 15 comprises one or more of these logic blocks. The command generator module 15 is configured to perform these operations. The command generator 15 receives as its input a PWM command 7, and a variable dead time duration 12, which is determined by a dead time calculator 13. The command generator 15 also receives from the current level controller 16 a signal of the removal allowed for each IGBT driven by the controller as, for

15    example, described previously. The controller of Figure 7 can be implemented by digital signal processing (DSP), field-programmable gate array (FPGA), or ASIC. The controller may also be implemented by software or hardware so as to run the operations of Figures 1 to 7.

20    The controller can be embedded to the power converter core to replace ordinary command generators. The controller can therefore control an electric power engine, UPS, or the like electric power machine.

25    FIG. 9 illustrates a transfer function of the controller according to exemplary embodiments of the present disclosure. Figure 9 shows actual

PWM function of the requested PWM function. Curve 17 illustrates an ideal case having a perfect converter with no dead time and minimal pulse duration. Curve 18 illustrates the operation of the exemplary embodiment of the converter having the standard operation mode without the command 5 removal (when applying both dead time and minimal pulse duration). Curve 19 illustrates the operation of the exemplary embodiment of the converter having variable dead time in operation. The difference between the curves 18 and 19 corresponds to the effect of the dead band. The clamping of the curves corresponds to the mixed effect of the dead band 10 and minimal pulse duration. X-axis 21 stands for requested duty cycle and Y-axis 20 for actual duty cycle. The advantages of the exemplary embodiments can be higher duty cycle. This gain is beneficial for power converter. Accordingly it is possible to obtain better performance or save costs of the power converter. The exemplary embodiment of the variable 15 dead time provides a continuous transfer function having thereby no risk of instability of regulations.

It will be apparent to those skilled in the art that various modifications and variations can be made to the controller, circuit and method. Other 20 embodiments will be apparent to those skilled in the art from consideration of the specification and practice of the disclosed controller and method. It is intended that the specification and examples be considered as exemplary only, with a true scope being indicated by the following claims and their equivalents.

LIST OF ELEMENTSPower Converter Controller

- 5      1 first power semiconductor device
- 2 second power semiconductor device
- 3 top command
- 4 bottom command
- 5 current flow
- 10     6 diode
- 7 requested PWM
- 8 dead time
- 9 minimal pulse
- 10 switching period
- 15     11 duration when power converter is in off state
- 12 variable dead time
- 13 dead time calculator
- 15 command generator
- 16 current level controller
- 20     17 curve
- 18 curve
- 19 curve
- 20 Y-axis
- 21 X-axis
- 25     22 real off time
- 23 off time of requested PWM
- 24 interval
- 25 function
- 26 interval

Claims

What is claimed is:

- 5 1. A controller for a power converter using pulse width modulation, comprising: at least one control module configured to cause the controller to
  - generate a command for switching a power semiconductor switch between a conductive and non-conductive state;
- 10 2. The controller according to claim 1, wherein the controller is configured to generate a delay interval between switching from the power semiconductor switch to another power semiconductor switch;
3. The controller according to any preceding claim, wherein the controller is configured to remove the command configured to control the power semiconductor switch so that the power semiconductor switch remains in the non-conductive state, wherein a diode allows an electric current to pass the power semiconductor switch in one direction, while blocking current in the opposite direction; and
- 15 4. The controller according to any preceding claim, wherein the controller is configured to modify the delay interval between switching from the power semiconductor switch to said another power semiconductor switch.
- 20 2. The controller according to claim 1, wherein the controller is configured to remove said delay time.
- 25 3. The controller according to any preceding claim, wherein the controller is configured to modify duration of said delay time in relation to an indication of said delay time received.
4. The controller according to any preceding claim, wherein the controller is configured to modify duration of said delay interval in relation to the pulse width modulation being requested.

5. The controller according to any preceding claim, wherein the controller is configured to modify duration of said delay interval in relation to a duty cycle of the pulse width modulation being requested.
- 5 6. The controller according to any preceding claim, wherein the controller is configured to modify duration of said delay interval in relation to the time that the pulse width modulation is in an off state.
- 10 7. The controller according to any preceding claim, wherein the controller is configured to modify duration of said delay interval in relation to the time that the pulse width modulation is in an on state.
- 15 8. The controller according to any preceding claim, wherein the controller is configured to modify duration of said delay interval in relation to a function.
9. The controller according to any preceding claim, wherein the function comprises a linear function within a predetermined interval.
- 20 10. The controller according to any preceding claim, wherein the function comprises a constant value within a predetermined interval.
- 25 11. The controller according to any preceding claim, wherein the controller is configured to control said another power semiconductor switch so that the power semiconductor switches generate the pulse width modulation in relation to the commands.
- 30 12. The controller according to any preceding claim, wherein the controller is configured to receive a pulse width modulation command for controlling said another power semiconductor switch.

13. The controller according to any preceding claim, wherein said diode is parallel coupled with the power semiconductor switch.
- 5 14. The controller according to any preceding claim, comprising a current level controller configured to detect whether the current exceeds a threshold and to send the controller an allowance message for removing the command.
- 10 15. A circuit, comprising the controller according to any preceding claim, wherein at least one circuit block comprises the at least one logic module.
16. A method for controlling a power converter using pulse width modulation, comprising:
  - 15 generating a command for switching a power semiconductor switch between a conductive and non-conductive state;
  - generating a delay interval between switching from the power semiconductor switch to another power semiconductor switch;
  - removing the command configured to control the power semiconductor switch so that the power semiconductor switch remains in an open state and still allows an electric current to pass in one direction, while blocking current in the opposite direction, and
  - 20 modifying the delay interval between switching from the power semiconductor switch to said another power semiconductor switch.

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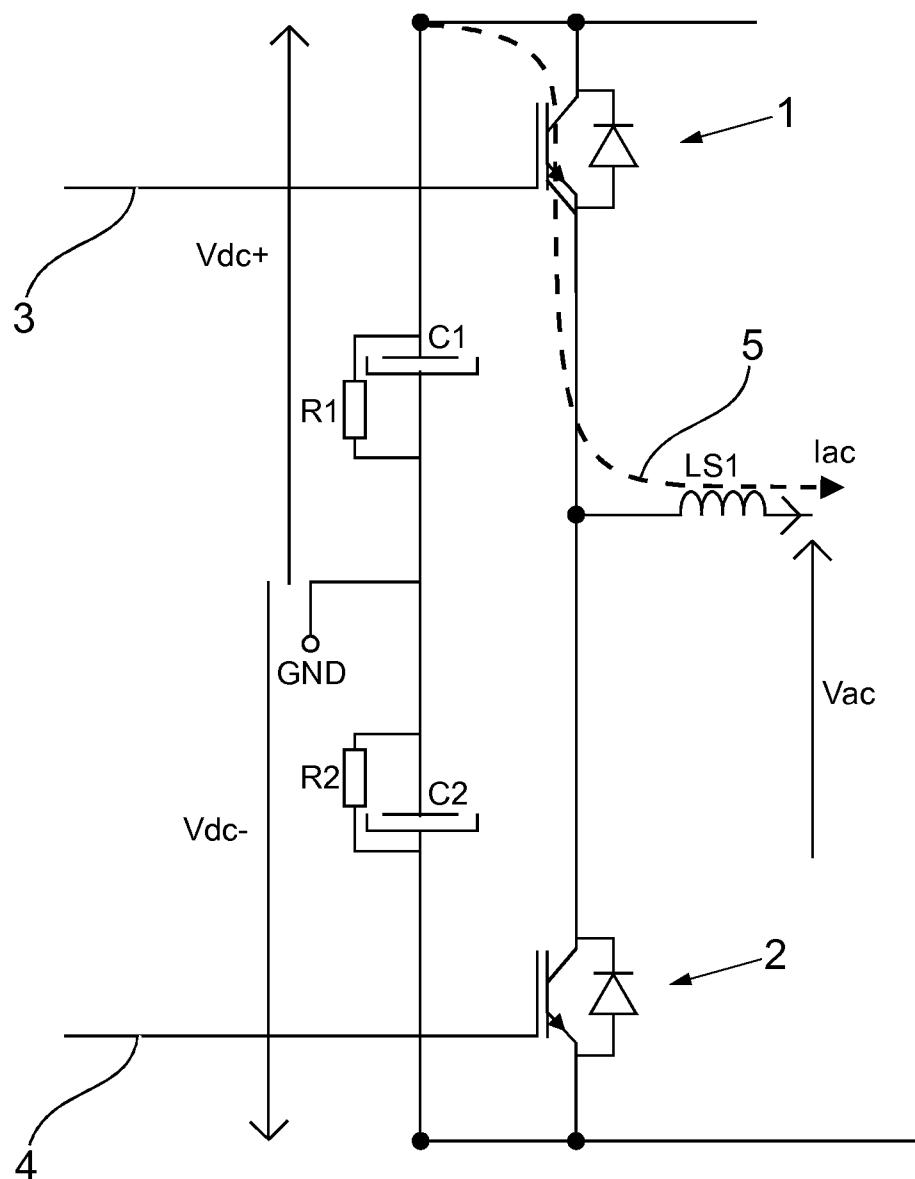


Fig. 1

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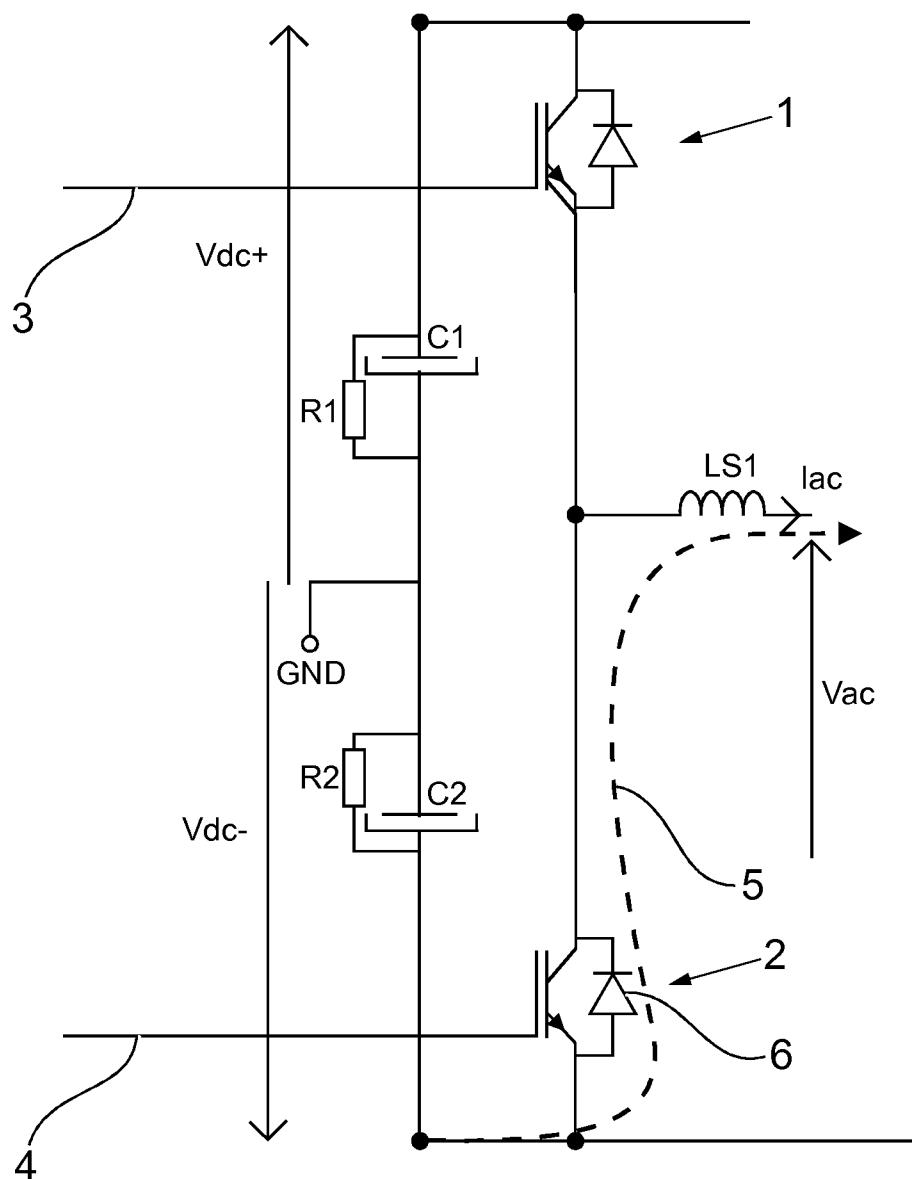


Fig. 2

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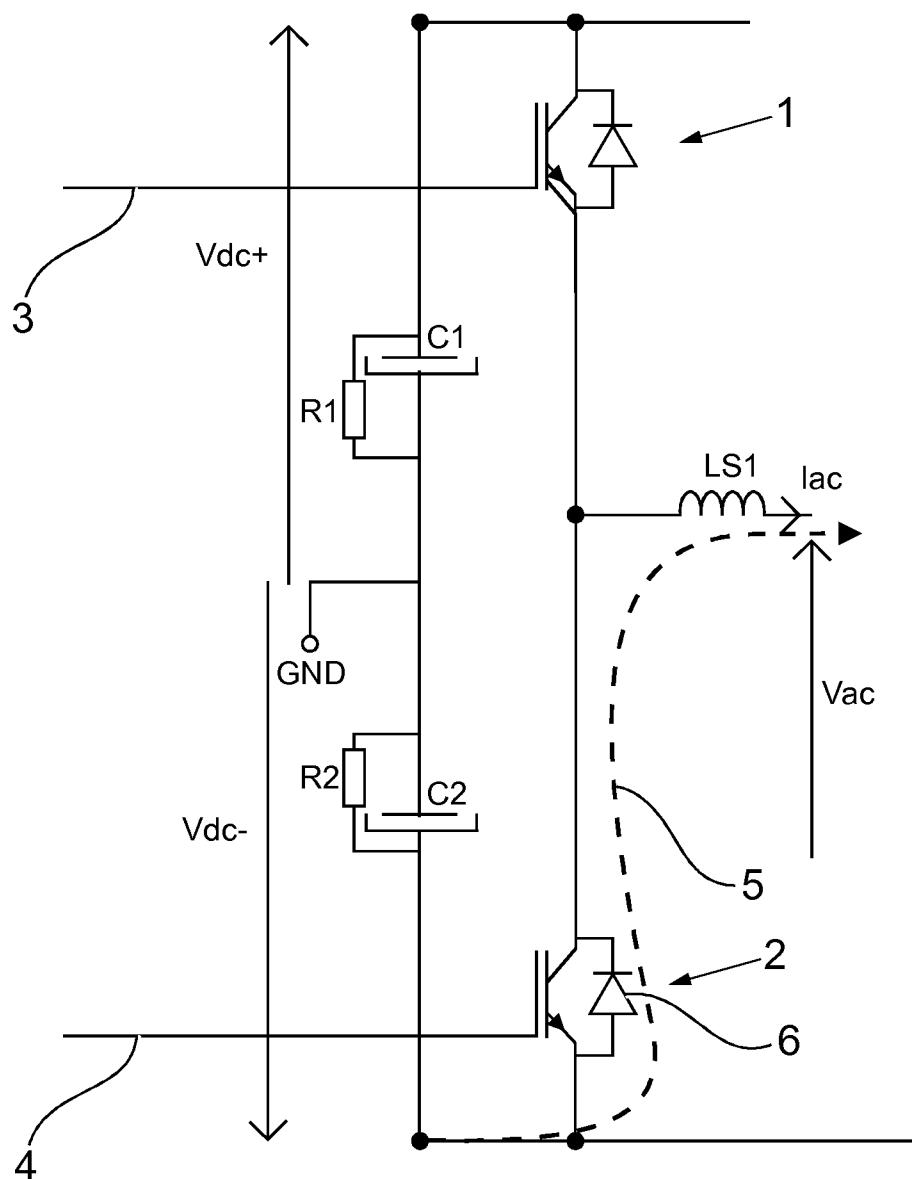


Fig. 3

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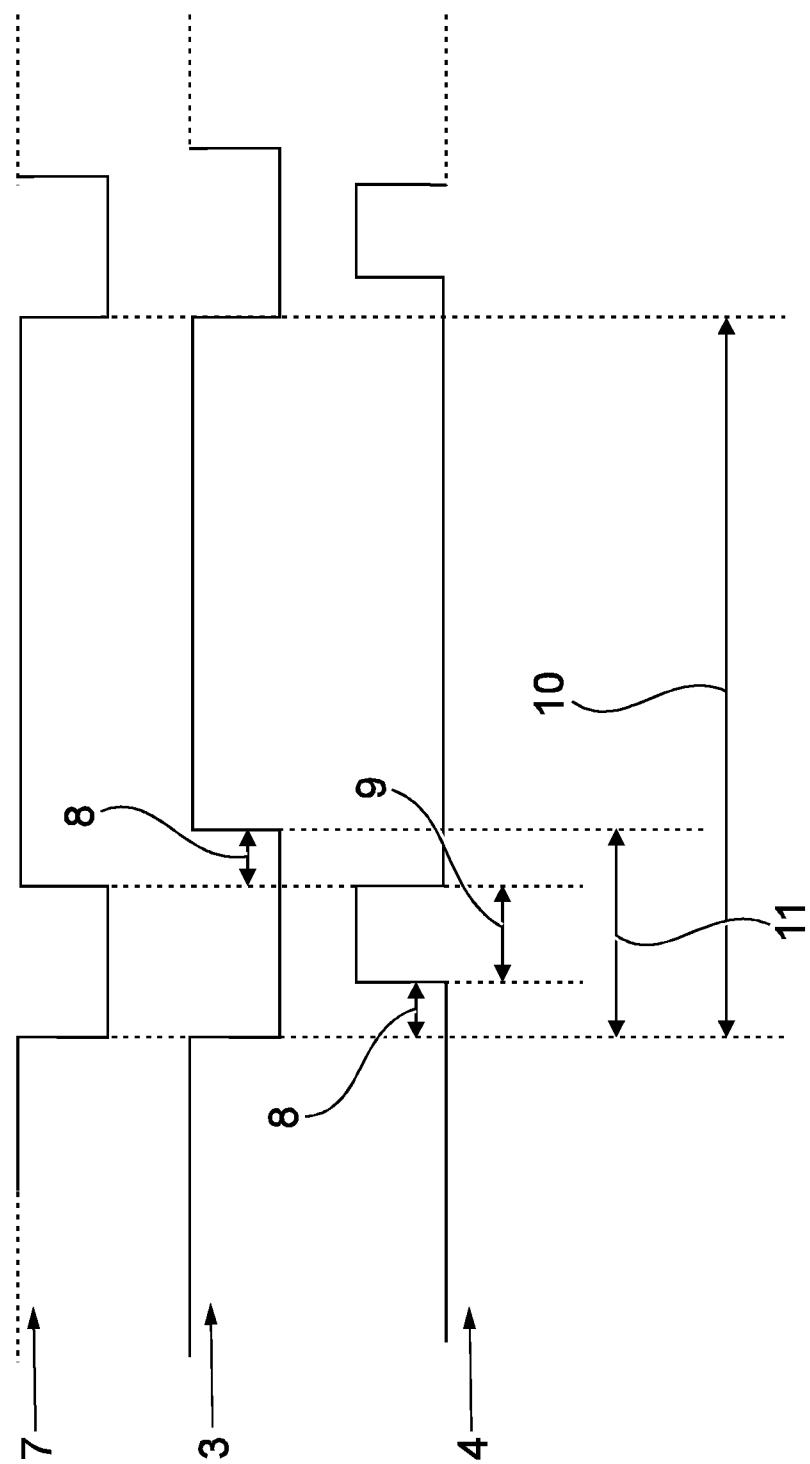


Fig. 4

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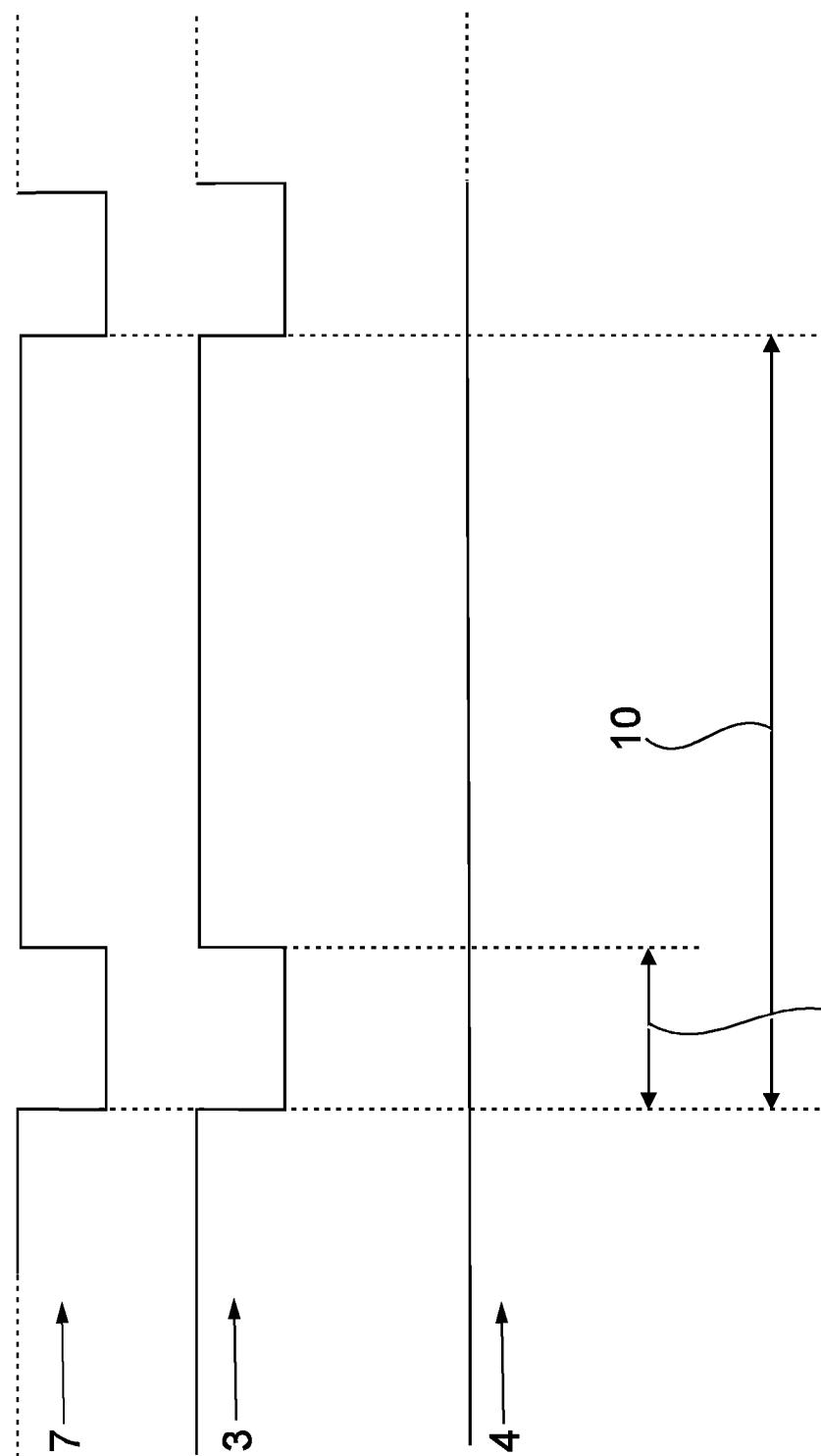


Fig. 5

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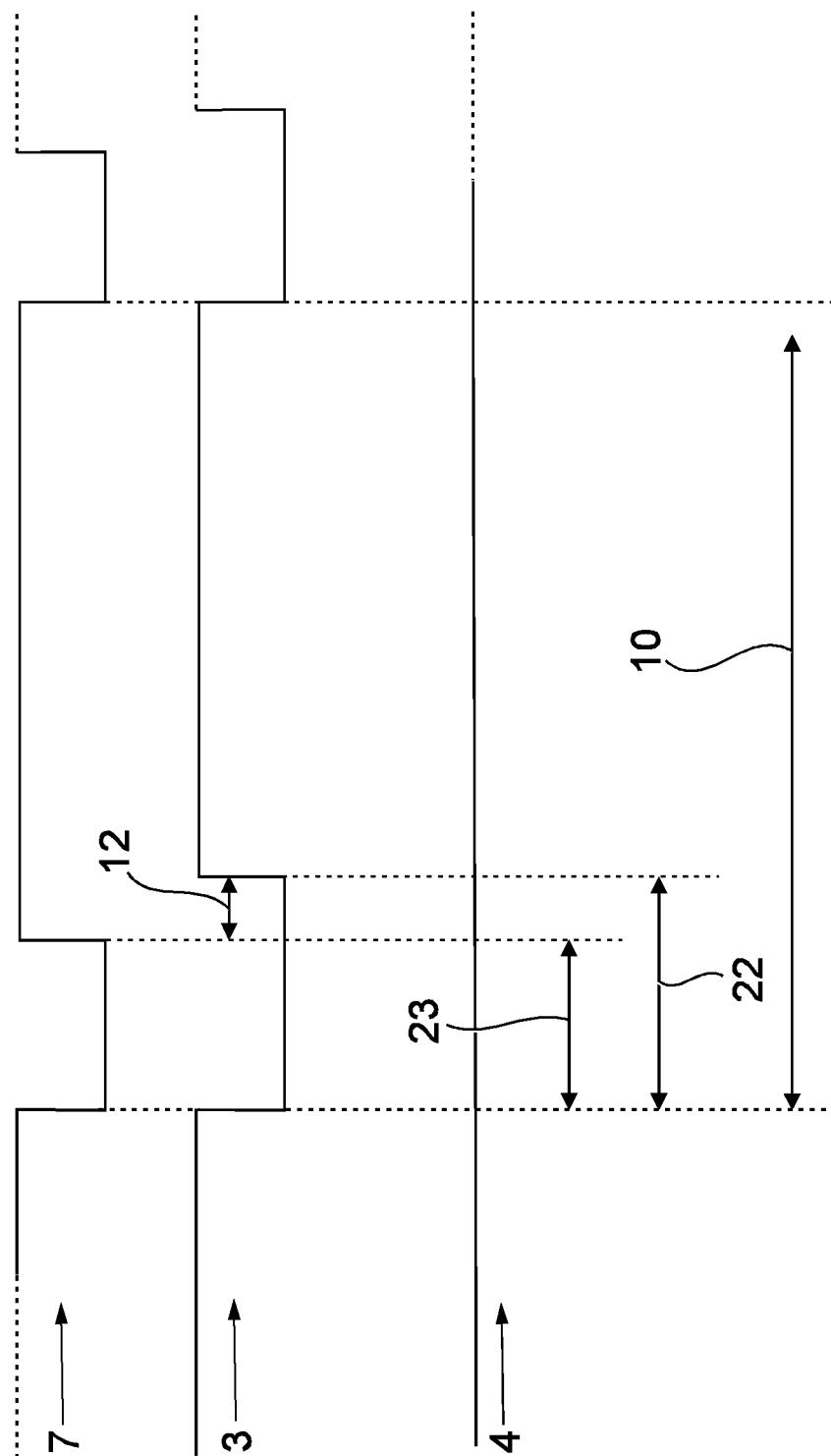


Fig. 6

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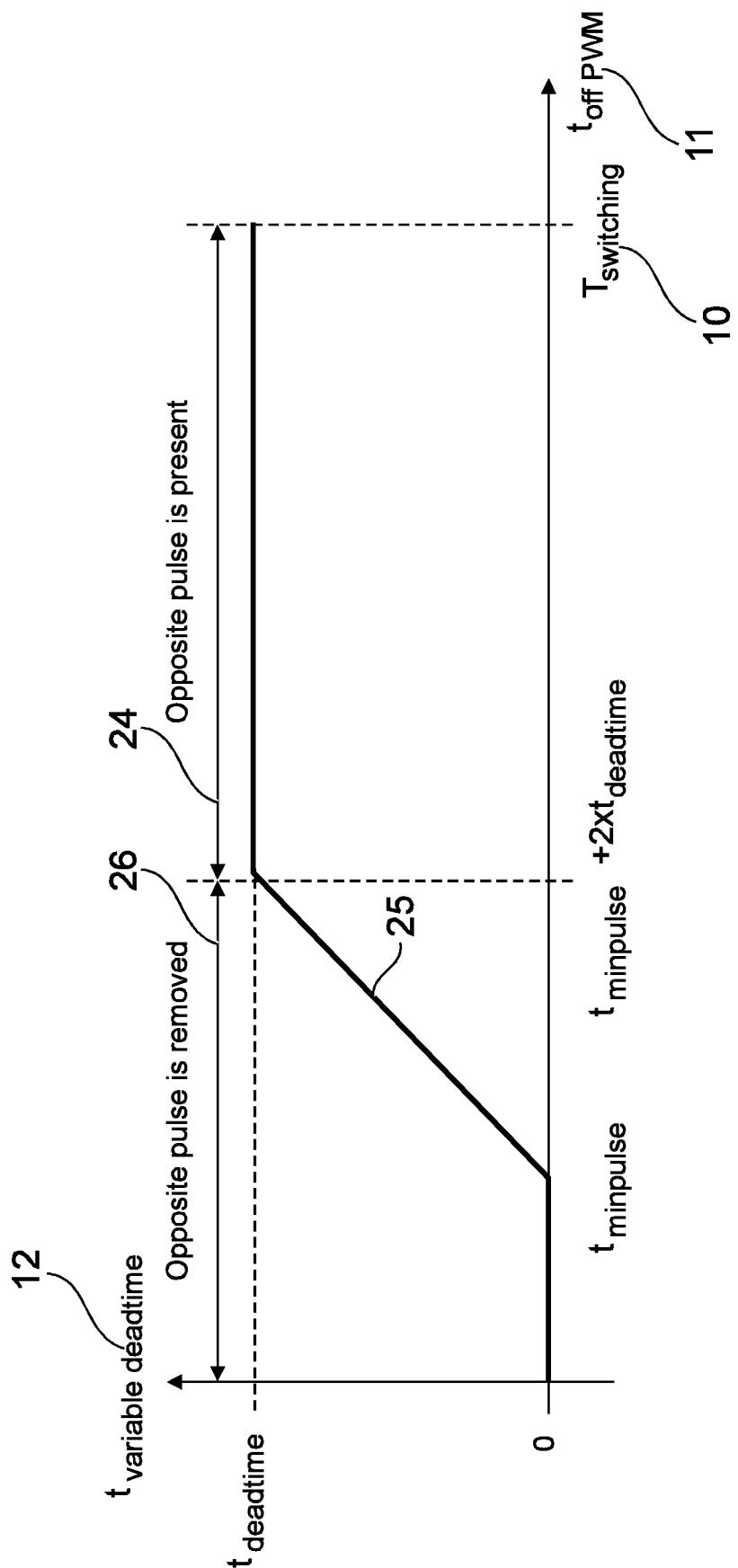


Fig. 7

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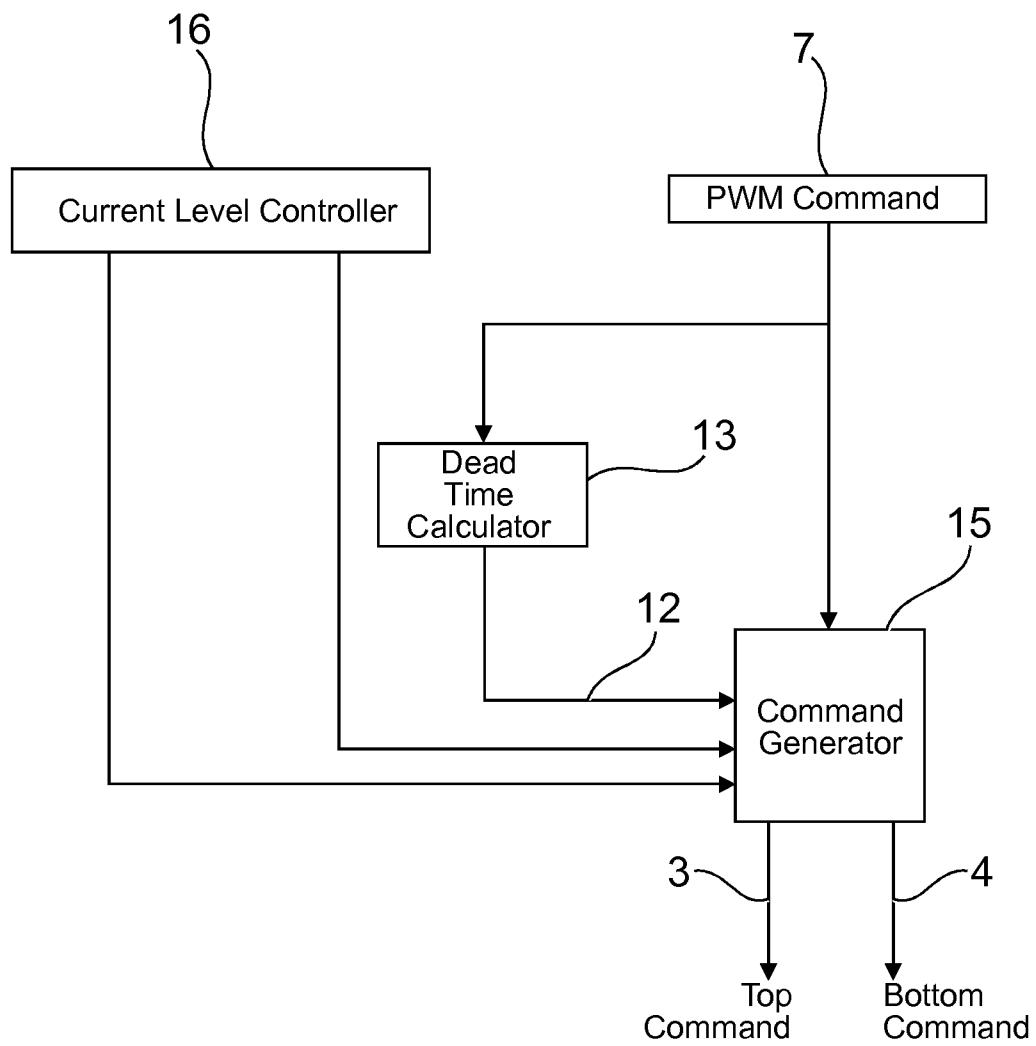


Fig. 8

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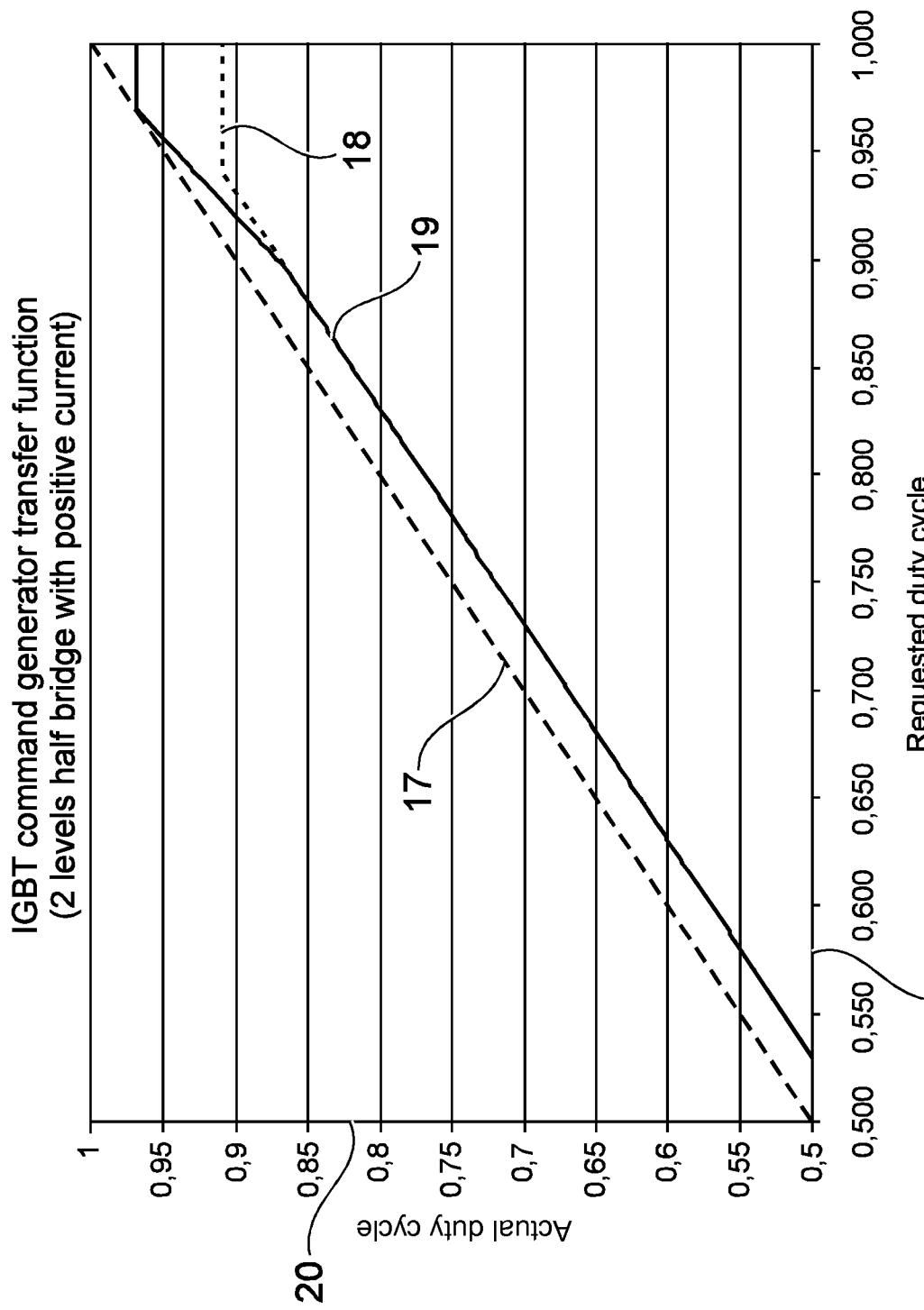


Fig. 9

# INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2012/00Q164

**A. CLASSIFICATION OF SUBJECT MATTER**

INV. H02M1/38

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal , PAJ, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 101 39 642 A1 (HERTY FRANK [DE]) 24 April 2003 (2003-04-24) A abstract; figures 1,2 ,4 paragraphs [0005] , [0007] , [0030] , [0042] - [0055] -----	1,2,8, 10-16 3-7,9
X	US 2004/027760 A1 (VILLARET YVES [IL]) 12 February 2004 (2004-02-12) figures 3-8 paragraphs [0003] , [0006] , [0007] , [0011] - [0018] , [0053] , [0054] , [0058] - [0064] , [0078] - [0096] ----- - / -	1,2,8, 10-16



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Date of the actual completion of the international search

Date of mailing of the international search report

8 November 2012

15/11/2012

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# INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 606 601 A2 (SIEMENS AG [DE]) 20 July 1994 (1994-07-20) figure 2 column 1, line 44 - column 2, line 49 column 3, lines 52-58 column 4, line 53 - column 5, line 38 -----	1-13,15., 16
A	US 2009/096502 A1 (MIYAMOTO NOBORU [JP] ET AL) 16 April 2009 (2009-04-16) figures 1,4,5 paragraphs [0025], [0026], [0028] - [0032], [0034], [0036], [0037], [0041] - [0045], [0050], [0051] -----	1-16

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/I B2012/00Q 164
---

Patent document cited in search report	Publication date	Patent family member(s)			Publication date
DE 10 139642	AI 24-04--2003	NON E			
-----					
us 2004027760	AI 12-02-2004	AU EP JP US Wo	2399902 A 1352458 A2 2004520790 A 2004027760 AI 0241085 A2		27-05-2002 15-10-2003 08-07-2004 12-02-2004 23-05-2002
-----					
EP 0606601	A2 20-07-1994	AT DE DE DK EP ES GR US	141728 T 430098 1 AI 59303500 D1 060660 1 T3 060660 1 A2 2090830 T3 3020838 T3 5515258 A		15-09-1996 21-07-1994 26-09-1996 07-10-1996 20-07-1994 16-10-1996 30-11-1996 07-05-1996
-----					
us 2009096502	AI 16-04--2009	DE JP JP US	102008036767 AI 4941223 B2 2009 100494 A 2009096502 AI		23-04-2009 30-05-2012 07-05-2009 16-04-2009
-----					