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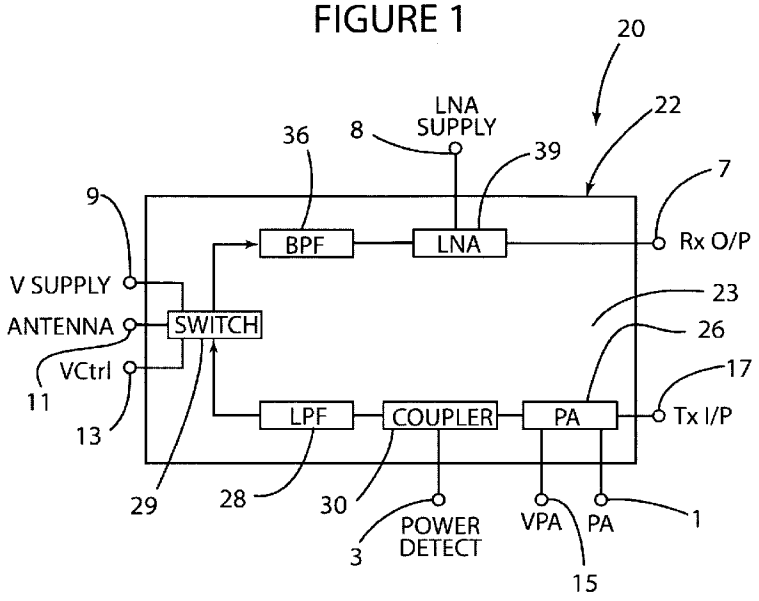
(54) Title: TIME DIVISION DUPLEX FRONT END MODULE

FIGURE 1



(57) Abstract: An RF module adapted for direct surface mounting to the top surface of the front end of the motherboard of a wireless base station such as, for example, a femtocell. The module comprises a printed circuit board having a plurality of direct surface mounted electrical components defining respective signal transmit and receive sections for RF signals. The signal transmit section is defined by at least a power amplifier, a coupler, and a lowpass filter. The signal receive section is defined by at least a receive bandpass filter and a low-noise amplifier. A lid covers selected ones of the electrical components except for at least the power amplifier. An RF switch is located between and interconnects the respective transmit and receive sections to an antenna pin.

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TIME DIVISION DUPLEX FRONT END MODULE

Cross-Reference to Related Applications

This application is a continuation-in-part non-provisional application which claims the benefit of U.S. Application Serial No. 11/452,800 filed on June 14, 2006; U.S. Application Serial No. 11/823,735 filed on June 28, 2007; and U.S. Provisional Application Serial No. 60/936,201, filed on June 19, 2007, the disclosures of which are explicitly incorporated herein by reference as are all references cited therein.

Field of the Invention

The invention relates to a module and, more particularly, to a time division duplex radio frequency (RF) module adapted for use on the front end of a cellular base station such as, for example, a WiMax wireless femtocell communication base station.

Background of the Invention

There are currently four types of cellular/wireless communication base stations or systems in use today for the transmission and reception of W-CDMA, UMTS, and WiMax based cellular/wireless communication signals, i.e., macrocells, microcells, picocells, and femtocells. Macrocells, which today sit atop cellular/wireless towers, operate at approximately 1,000 watts. The coverage of macrocells is in miles. Microcells, which are smaller in size than macrocells, are adapted to sit atop telephone poles, for example, and the coverage is in blocks. Microcells operate at approximately 20 watts. A smaller yet microcell requires about 5 watts of power to operate. Picocells are base stations approximately 8" x 18" in size, are adapted for deployment inside buildings such as shopping malls, office buildings or the like, and output about .25 watts of power. The coverage of a picocell is about 50 yards. Femtocells output about .10 watts of power and are used in the home.

All of the picocells and microcells in use today include a "motherboard" upon which various electrical components have been individually mounted by

the customer. A front end portion of the motherboard (i.e., the RF transceiver section thereof located roughly between the picocell antenna and mixers thereof) is currently referred to in the art as the "node B local area front end," i.e., a portion of the femtocell, picocell, or microcell on which all the radio frequency control electrical components such as, for example, the filters, amplifiers, couplers, inductors and the like have been individually mounted and interconnected.

While the configuration and structure of the current motherboards has proven satisfactory for most applications, certain disadvantages associated with the current front end RF configuration thereof include performance, the costs associated with a customer's placement of individual RF components onto the motherboard during assembly, and the space which such RF components occupy on such motherboards.

There thus remains the need for increased RF component performance and a reduction in both the cost of these motherboards and the space occupied by the RF components on such motherboards. The present invention provides a compact front end RF component module particularly adapted and structured for the transmission and reception of WiMax signals which addresses and solves the above-identified needs.

Summary of the Invention

The present invention relates generally to a radio frequency (RF) module adapted for use on the front end of a wireless base station such as a femtocell, picocell, or microcell base station. The RF module includes a printed circuit board/substrate having a plurality of electrical components mounted directly thereto and adapted to allow for the transmission and reception of wireless signals between the antenna of the cell on one end and the respective input and output pads on the motherboard of the cell at the other end.

A first section on the printed circuit board/substrate defines a transmit path for RF signals and includes at least the following electrical components mounted thereon: a power amplifier, a coupler and a lowpass filter.

The module includes a second section on the printed circuit board/substrate which defines a receive path for RF signals and includes at least the following electrical components mounted thereon: a receive bandpass filter and a low-noise amplifier.

An RF single pole double throw (SPDT) switch is located between and interconnects the respective transmit (Tx) and receive (Rx) sections to an antenna pin.

A lid is adapted to cover selected ones of the electrical components mounted to the printed circuit board. At least the power amplifier is preferably located outside the lid. A plurality of through-holes or vias located below the amplifier are adapted to define a sink for heat created by the power amplifier.

Other advantages and features of the present invention will be more readily apparent from the following detailed description of the preferred embodiment of the invention, the accompanying drawings, and the appended claims.

Brief Description of the Drawings

These and other features of the invention can best be understood by the following description of the accompanying FIGURES as follows:

FIGURE 1 is a simplified block diagram depicting the flow of wireless signals being transmitted and received through the various RF components defining the time division duplex front end module of the present invention;

FIGURE 2 is an enlarged simplified perspective view of a time division duplex front end module in accordance with the present invention;

FIGURE 3 is an enlarged simplified plan view of the front or top surface of the printed circuit board of the front end module of the present invention with the lid removed therefrom; and

FIGURE 4 is an enlarged simplified plan view of the back or bottom surface of the printed circuit board of the front end module of the present invention.

Detailed Description of the Preferred Embodiment

While this invention is susceptible to embodiments in many different forms, this specification and the accompanying FIGURES disclose only one preferred simplified embodiment as an example of the present invention which is adapted for use in a picocell. The invention is not intended, however, to be limited to the embodiment so described and extends, for example, to femtocells and microcells as well.

FIGURE 1 is a simplified block diagram of the RF (radio frequency) front end module, generally designated 20, constructed in accordance with the present invention and adapted for use in connection with a wireless base station including, for example, a WiMax femtocell, picocell, or microcell.

As described in more detail below, the TDD (time division duplex) WiMax front end module 20 utilizes filtering with two filters: a receive Rx bandpass filter 36, and a transmit Tx lowpass filter 28. The module 20 also includes a power amplifier (PA) 26, a low-noise amplifier (LNA) 39 and other appropriate RF components. In the embodiment shown, all of the appropriate RF components are of the discrete surface-mountable type.

Module 20 is adapted to replace all of the discrete RF components that would be typically individually mounted and used in a WiMax Node B local area front end. Module 20 allows customers to select different values for receiver sensitivity, selectivity, and output power. Moreover, module 20 is RoHS compliant and lead-free. Some of the features of the module 20 as introduced above and described in more detail below include the scalable power amplifier 26 capable of delivering about 25 dBm at the antenna port; the above-identified filters 28 and 36 offering excellent isolation and harmonic suppression; and the low noise amplifier 39.

Table 1 below summarizes the proposed operational parameters and characteristics of the time division duplex front end module of the present invention:

TABLE 1

Typical Specifications

Nominal channel bandwidth: 20 MHz

Modulation: 64 QAM
Antenna switching speed < 1 usec

TRANSMIT		RECEIVE	
Frequency range	2496 – 2692 MHz	Frequency range	2496 – 2692 MHz
PA supply voltage	5V	LNA supply voltage	3.3V
PA current drain	650 mA	LNA current drain	15 mA
Power @ antenna port	25 dBm	Noise figure	2.2 dB
EVM @ 25 dBm	2.5%	IIP3	3 dBm
Tx gain	23 dB	Rx gain	14 dB

Attenuation (.1 – 1796 MHz)	-45dB
2396 MHz	-27dB
2790 MHz	-27dB

Temp range: -40°C - 85°C

Referring now in particular to FIGURE 1, it is understood that module 20 is defined by a plurality of RF electrical components and pins associated with a substrate 22 and defining respective RF signal transmit and receive sections or paths. Initially, and as shown in FIGURE 1, the lower RF transmit section or path of module 20 includes a first Tx (transmit) signal input pin 17 adapted to be coupled to a corresponding Tx (transmit) signal pad on the motherboard (not shown) of a picocell or microcell. Pin 17 in turn is coupled to a Tx PA (transmit power amplifier) 26 which, in turn, is coupled to a coupler 30 which, in turn, is coupled to a Tx LPF (transmit low pass filter) 28.

VPA (power amplifier supply voltage) is adapted to be supplied to power amplifier 26 through pin 15. PA bias is adapted to be measured through pin 1 coupled to power amplifier 26. In accordance with the present invention, a portion of the transmit signal is split off from coupler 30 and passed to a power detect pin 3. The Tx LPF 28 is, in turn, coupled to an RF SPDT (single pole double throw) switch 29. The switch 29, in turn, is coupled

to an antenna via antenna pin 11. Voltage is supplied to the module 20 through the V supply (voltage supply) pin 9 coupled to switch 29. The voltage supplied to module 20 is controlled via and through V_{CTRL} (voltage control) pin 13, also coupled to the switch 29. In another embodiment, the V_{CTRL} pin 13 can be omitted and the switching function can be facilitated with the use of only one voltage input pin (i.e., pin 9).

All of the pins associated with the substrate 22, including antenna pin 11, extend between the top and bottom surfaces of the module 20 and are adapted to be direct surface mounted into coupling relationship with corresponding pads (not shown) of a picocell or microcell such as, for example, the antenna pad thereof to allow for the transmission of the signals which have passed through the RF signal transmission section of module 20.

Referring to FIGURES 1-4, it is thus understood that the Tx (transmit) RF wireless signal is adapted to travel from the femtocell/picocell/microcell motherboard into and up through the substrate 22 of module 20 via Tx input pin 17 extending between the lower and upper substrate surfaces, and then from Tx input pin 17 into and through power amplifier 26, coupler 30, lowpass filter 28, switch 29, antenna pin 11, and then back down through the substrate 22 via antenna pin 11 extending between the upper and lower substrate surfaces and into the motherboard antenna pad in direct surface contact with module antenna pin 11.

The top receive section or path of the signals being received (i.e., Rx signals) from the femtocell, picocell, or microcell antenna (not shown) and transmitted through the module 20 will now be described also with reference to FIGURES 1-4 which shows the Rx signal being transmitted and passed in a left to right, clockwise direction from the picocell or microcell antenna (not shown) through the module antenna pin 11 and then initially through the switch 29.

Switch 29 is, of course, adapted and structured as known in the art to allow the same to switch from the passage of Tx signals out of the module 20 through the antenna pin 11 to the passage of Rx signals into and through the module 20 from the antenna pin 11. Thus, and as shown in FIGURE 1, the Rx signal is adapted to pass and travel in a general clockwise direction

through the switch 29 and into Rx bandpass filter 36 and LNA (low noise amplifier) 39. Voltage is supplied to low noise amplifier 39 via LNA supply voltage pin 8 coupled thereto.

From the low-noise amplifier 39, the Rx signal then passes through Rx O/P (output) signal pin 7 which, in turn, is adapted to extend between the front and back surfaces 23 and 27 of the module 20 for direct surface coupling to the corresponding Rx output signal pad (not shown) on the motherboard of the picocell or microcell.

FIGURES 2-4 depict one simplified embodiment of a module 20 adapted and structured to be direct surface mounted to the front end of a WiMax TDD (time division duplex) femtocell, picocell, or microcell. It is understood, however, that the module embodiment of FIGURES 2-4 differs from the module embodiment of FIGURE 1 in that, in the FIGURES 2-4 embodiment, PA power is detected through the use of a VDET pin 3 instead of a coupler as in the FIGURE 1 embodiment.

By way of background, it is understood that module 20 of the present invention as depicted in FIGURES 2-4 measures about 19.0mm in width, 27.0mm in length, and 6.0mm max. in height (with the lid secured thereon), and is adapted to be mounted to the motherboard of a WiMax picocell measuring about 8 inches by 18 inches which, as described above, is adapted for use as a wireless signal transfer base station inside a building such as a shopping mall or office complex.

In accordance with the present invention and referring to FIGURES 2-4, module 20 initially comprises a printed circuit board or substrate 22 which, in the embodiment shown, is preferably made of multiple layers of GETEK® or the like dielectric material and is about 1mm (i.e., .040 inches) in thickness. Although not shown in any of the FIGURES, it is understood that predetermined regions of both the upper and lower surfaces 23 and 27 of the substrate 22 are covered with copper or the like material and solder mask material, both of which have been applied thereto and/or selectively removed therefrom as is known in the art to create the desired copper, dielectric, and solder mask regions and electrical circuits which interconnect the various

electrical components. The metallization system is preferably ENIG, electroless nickel/immersion gold over copper.

A lid 45 (FIGURE 2), which is adapted to cover a portion of the top surface 23 of the printed circuit board 22, is preferably brass with a Cu/Ni/Sn (copper/nickel/tin) plated material for ROHS compliance purposes. Lid 45 is adapted to act both as a dust cover and a Faraday shield.

As described above, generally rectangularly-shaped substrate 22 has top or front surface 23 (FIGURES 2 and 3), a bottom or back surface 27 (FIGURE 4), and an outer peripheral circumferential edge defining respective upper and lower faces or edges 42 and 44 and side faces or edges 46 and 48 (FIGURES 2-5). Although not described in any detail, it is understood that, in a preferred embodiment, substrate 22 will be comprised of a plurality of stacked laminate layers of suitable dielectric material sandwiched between respective layers of conductive material as is known in the art such as, for example, a bottom RF ground plane layer, an RF intermediate signal layer, a top RF ground layer, and a topmost DC/RF layer plus ground layer.

Castellations 35 (FIGURES 2-4) are defined and located about the outer peripheral edge of board 22. Castellations 35 define the various ground and DC voltage input/output pins of the module 20. Castellations 35 are defined by metallized semicircular grooves which have been carved out of the respective edges 42, 44, 46 and 48 and extend between the respective top and bottom surfaces 23 and 27 of the substrate 22. In the embodiment shown, the castellations 35 are defined by plated through-holes which have been cut in half during manufacturing of the substrates from an array. Castellations 35 extend along the length of the respective edges of substrate 22 in spaced-apart and parallel relationship. In the embodiment shown, the top substrate edge 42 defines seven spaced-apart castellations 35, the lower substrate edge 44 defines five spaced-apart castellations 35, the side substrate edge 46 defines three castellations 35, and the opposed side substrate edge 48 defines one castellation 35.

The outer surface of each of the respective castellations 35 is coated as by electroplating or the like, with a layer of copper or the like conductive material which is initially applied to all of the surfaces of the substrate 22

during the manufacturing of the substrate 22 as is known in the art and then removed from selected portions of the surfaces to define the copper coated castellations 35. Castellations 35 and, more specifically, the copper thereon creates an electrical path between top surface 23 and bottom or back surface 27 of substrate 22.

Although not shown, it is understood that the copper extends around both the top and bottom edges of each of the castellations 35 to define pads of copper or the like conductive material on the top surface 23 of substrate 22 and surrounding the top or front edge of each of the respective castellations 35; and a plurality of pads extending inwardly from the bottom or back edge of each of the castellations 35 on the bottom surface 27 of substrate 22 which allow the module 20 to be directly surface mounted by reflow soldering or the like, to corresponding pads located on the surface of the motherboard of the picocell (not shown).

Although not disclosed in any detail, it is understood that respective ones of the castellations define respective voltage input/output pins while other ones of the castellations 35 define pins adapted for direct coupling to the ground copper layer applied to both of the surfaces 23 and 27.

Conductive vias 38 defined in the board 22 define the respective RF component signal input/output and antenna pins 7, 11, and 17 of the module 20. Vias 38 extend through the substrate 22 between the substrate surfaces 23 and 27 thereof and, as known in the art, define an interior cylindrical surface which has been plated with copper or the like conductive material. In accordance with the present invention, the use of vias 38 which are spaced from the respective substrate edges instead of castellations 35 defined in respective substrate edges insures a constant 50-ohm characteristic impedance.

Pinouts 1 and 3 extend along the bottom longitudinal edge 44 of board 22. Pinout 7 extends along the side longitudinal edge 48. Pinouts 8, 9, and 13 extend along the top longitudinal edge 42 of board 22. Pinout 17 extends along the side longitudinal edge 46 of board 22.

With reference to FIGURES 2 and 3, power amplifier 26 (together with the other components which are part of the Tx signal path) is preferably

located in an area of the printed circuit board 22 not intended to be covered by the lid 45, to allow for the dissipation of heat created by the amplifier 26 and also to reduce the transfer of heat created by the amplifier 26 to any of the electrical components located under the lid 45.

More specifically, it is understood that, in the preferred embodiment, power amplifier 26 is generally centrally located on the left hand half of the top or front surface 23 of the substrate/board 22. Pinout 13 extends generally opposite the top edge of power amplifier 26 along longitudinal board edge 42. Pinouts 1 and 3 extend generally along the bottom edge of power amplifier 26 along the length of bottom longitudinal board edge 44. Pinout 17 extends generally opposite the left side edge of power amplifier 26 along (but spaced inwardly from) board side edge 46.

In the embodiment shown, a first set of appropriate resistors and capacitors 101, 102, 103, 104, 105, 106, and 107 are all generally located and fixed on the top or front surface 23 of board 22 generally below the power amplifier 26 and, more specifically, between the power amplifier 26 and the lower longitudinal edge 44 of board 22.

A second set of appropriate resistors, capacitors, and inductors 108, 109, 110, 111, 112, and 113 are all generally located and fixed on the top or front surface 23 of the board 22 to the left of the power amplifier 26 and, more specifically, between the power amplifier 26 and the left side longitudinal edge 46 of the board 22.

A third set of appropriate resistors and capacitors 114, 115, 116, and 117 are all generally located and fixed on the top or front surface 23 of the board 22 generally above the top edge of power amplifier 26 and, more specifically, between the power amplifier 26 and the top longitudinal edge 42 of board 22.

Tx low pass filter 28 is located and fixed on the left half of the top or front surface 23 of the board 22 generally between the right side edge of the power amplifier 26 and the left edge of the lid 45.

A fourth set of appropriate resistors, capacitors and inductors 118, 119, 120, and 121 are all located and fixed on the top surface 23 of the board 22 generally between the power amplifier 26 and the Tx low pass filter 28.

Capacitors 122 and 123 are located the top surface 23 of the board 22 generally above Tx low pass filter 28 and, more specifically, between the Tx low pass filter 28 and the top longitudinal edge 42 of board 22.

RF switch 29, Rx bandpass filter 36, and Rx low noise amplifier 39 are all generally located on the right half of the board 22 and adapted to be located below the lid 45. More specifically, Rx bandpass filter 36 is seated on and covers a substantial portion of the lower portion of the right half of the top or front surface 23 of the board 22. RF switch 29 and Rx low noise amplifier 39 are both generally located above the Rx bandpass filter 36 and, more specifically, between the top longitudinal edge of the Rx bandpass filter 36 and the top longitudinal edge 42 of the board 22.

Pinout 7 extending along (but spaced inwardly from) the board side edge 48 is located generally opposite the right side edge of the Rx low noise amplifier 39. Pinout 11 extending along (but spaced inwardly from) the board top longitudinal edge 42 is located generally opposite the top edge of the RF switch 29.

Appropriate capacitors 124, 125, and 126 surround RF switch 29. Appropriate capacitors, resistors, and inductors 127, 128, 129, 130, 131, 132, 133, and 134 surround Rx low noise amplifier 39.

Referring to FIGURES 2 and 3, lid 45 includes a top wall or roof 46, a first pair of respective opposed side walls 49a and 49b, and a second pair of respective opposed side walls 51a and 51b, all adapted to depend and extend generally perpendicularly downwardly from the peripheral edges of the roof 46 to define the lid when the walls are folded during assembly. Each of the walls 49a, 49b, 51a and 51b in turn defines a lower longitudinal terminal edge 53. The edge 53 of each of the side walls 49a and 49b in turn defines at least two spaced-apart tabs 50a and 50b projecting downwardly therefrom and adapted to be fitted into respective through-slots or castellations 37 defined in the top surface 23 of the board 22 for locating and securing the lid 45 to the board 22 in a grounded relationship with the board 22 wherein the edges 53 of the respective lid walls 49a, 49b, 51a and 51b are seated over respective elongate ground strips (not shown) defined on the board top surface 23, thus providing and defining a grounded lid 45.

As also shown in FIGURE 4, a plurality of through-holes or vias 136 are defined and formed on the board 22 beneath the region where the power amplifier 26 is seated on the board 22 to define a heat sink for the heat created by power amplifier 26. Through-holes 136 could be double-plated with copper or the like material for added thermal conductivity and likewise extend through the board 22.

The process for assembling a module 20 involves the following steps. After the substrate/board 22 has been fabricated, i.e., once all of the appropriate and desired copper castellations, copper strips, copper vias, copper pads, and copper through-holes have been formed thereon as known in the art, Ag/Sn (silver/tin) solder is screen printed onto a 2.6" by 4.6" printed circuit board array and, more particularly, onto the surface of each of the appropriate solder pads and strips defined on the array following the application of predetermined layers and strips of solder mask material as known in the art. Solder is applied to the surface of all of the designated copper strips, pads and regions and all of the desired and appropriate electrical components including all of the filters defining the module 20 are then appropriately placed and located on the array.

Although not described in any detail, it is understood that the particular selection, number, placement, and values of the appropriate resistors, capacitors, and inductors may vary depending upon the desired end application and performance characteristics of the module 20.

The lid 45 is then placed over the appropriate portion of the board 22 as described above into a soldered coupled relationship wherein the tabs 50a and 50b thereof are fitted into appropriate castellations/slots 37 defined in the board 22 thereby appropriately locating and securing the lid 45 to the board 22.

To complete the manufacturing process, the module 20 is then reflow soldered at a maximum temperature of 260°C so as to couple all of the components and lid 45 to the board. Finally, the array is diced up as is known in the art and the individual modules 20 are then final tested and subsequently "taped and reeled" and readied for shipment.

While the invention has been taught with specific reference to an embodiment of the module adapted for use on the front end of a picocell, it is understood that someone skilled in the art will recognize that changes can be made in form and detail such as, for example, to the selection, number, placement, interconnection values, and patterns of the various RF elements and circuits, without departing from the spirit and the scope of the invention as defined in the appended claims. The described embodiment is to be considered in all respects only as illustrative of one embodiment and not restrictive.

What is claimed is:

1. An RF module adapted for direct-surface mounting to the front end of the motherboard of a cell, the module comprising:

a substrate including top and bottom surfaces;

a first section on said substrate defining a transmit path for RF signals and including at least the following electrical components: a power amplifier, a coupler, and a lowpass filter;

a second section on said substrate defining a receive path for RF signals and including at least the following electrical components: a receive bandpass filter and a low-noise amplifier; and

an RF switch between and interconnecting said respective first and second sections to an antenna pin.

2. The RF module of claim 1 further comprising a lid adapted to cover at least said receive bandpass filter and said low-noise amplifier.

3. An RF module adapted for direct surface mounting to a front end of a motherboard of a wireless base station and adapted to transmit and receive RF signals, the module comprising:

a signal transmit section on a circuit board including at least a power amplifier, a coupler, and a lowpass filter; and

a signal receive section on said circuit board including at least a receive bandpass filter and a low-noise amplifier.

4. The RF module of claim 3 further comprising a lid adapted to cover selected ones of the electrical components mounted on said printed circuit board.

5. The RF module of claim 4, wherein at least said receive bandpass filter and said low-noise amplifier are located under said lid.

6. The RF module of claim 4, wherein said power amplifier is located outside said lid and said printed circuit board defines a plurality of through-holes located below said power amplifier.

7. The RF module of claim 3, wherein a switch is located between said respective signal transmit and receive sections.

8. An RF module adapted for direct surface mounting to a front end of a motherboard of a wireless base station, said module including a printed circuit board having a plurality of electrical components mounted thereon and adapted to allow for the transmission and reception of wireless signals between the antenna of said wireless base station on one end and the respective input and output pads on said motherboard of said wireless base station at the other end.

9. The RF module of claim 8 comprising at least a receive bandpass filter and a transmit lowpass filter all direct surface mounted to said printed circuit board of said module.

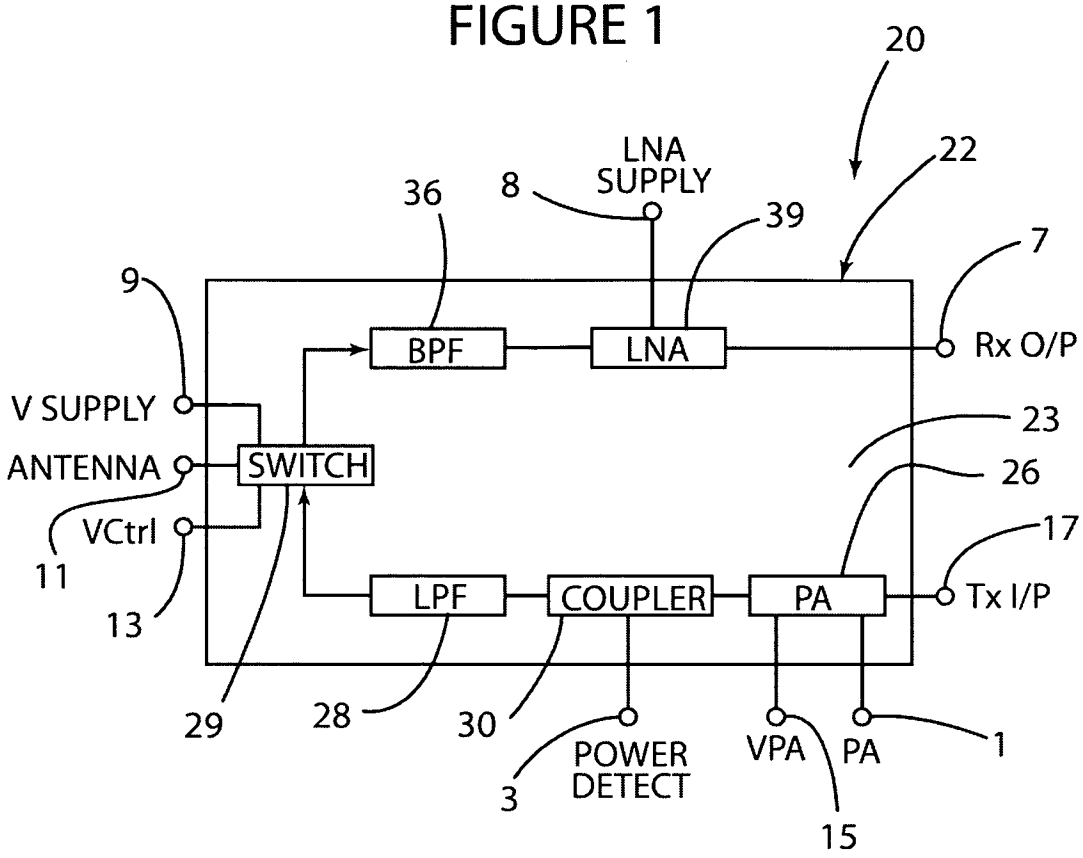
10. The RF module of claim 9 further comprising a power amplifier and a low-noise amplifier, both also direct surface mounted to said printed circuit board of said module.

11. The RF module of claim 10 wherein said power amplifier, a coupler, a lowpass filter and a switch define a transmit path for RF signals.

12. The RF module of claim 11 wherein said switch, said receive bandpass filter, and said low-noise amplifier define a receive path for RF signals.

13. The RF module of claim 12 further comprising a lid adapted to cover at least said low-noise amplifier and said receive bandpass filter.

FIGURE 1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VCtrl
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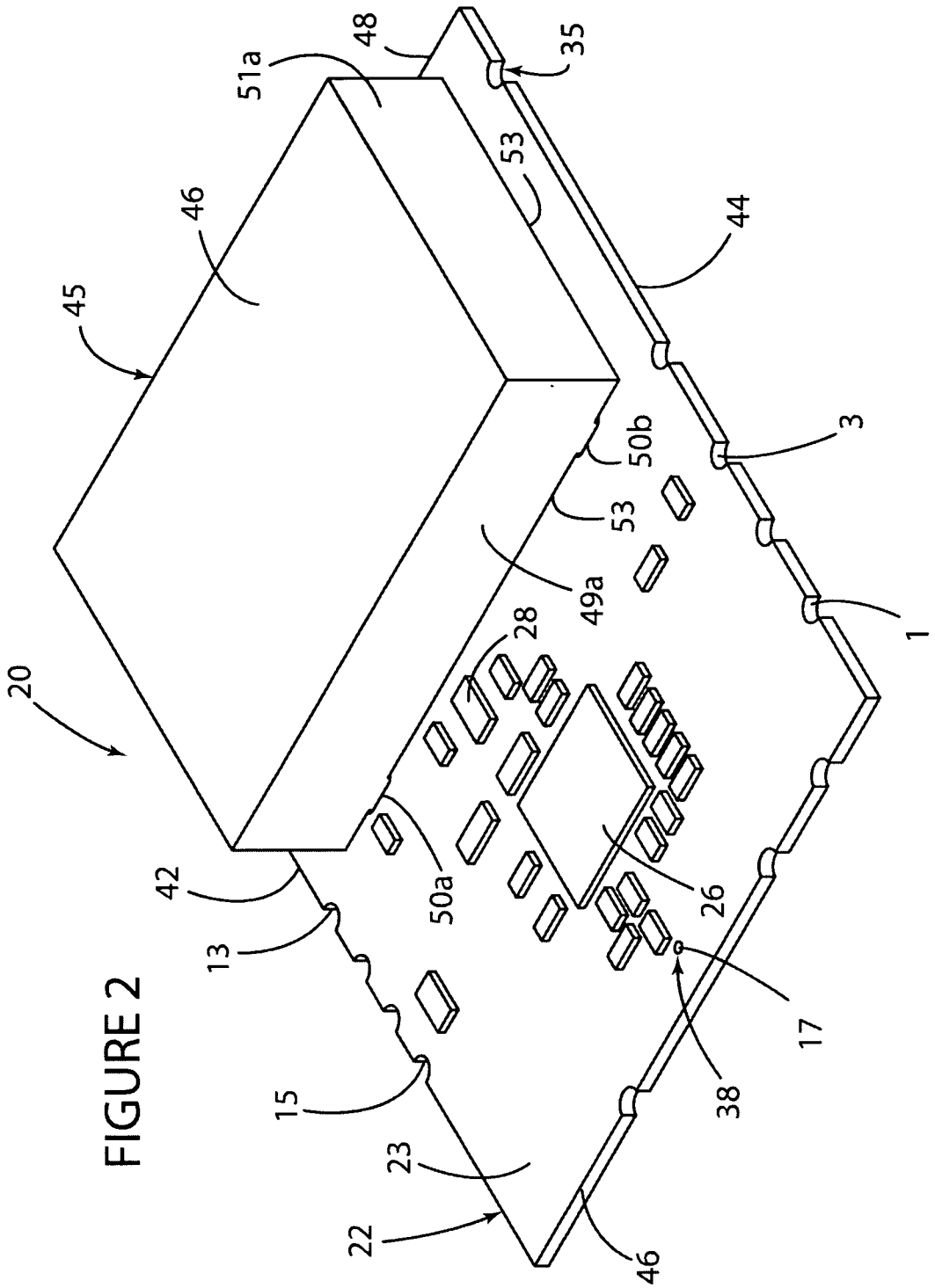
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46

FIGURE 2

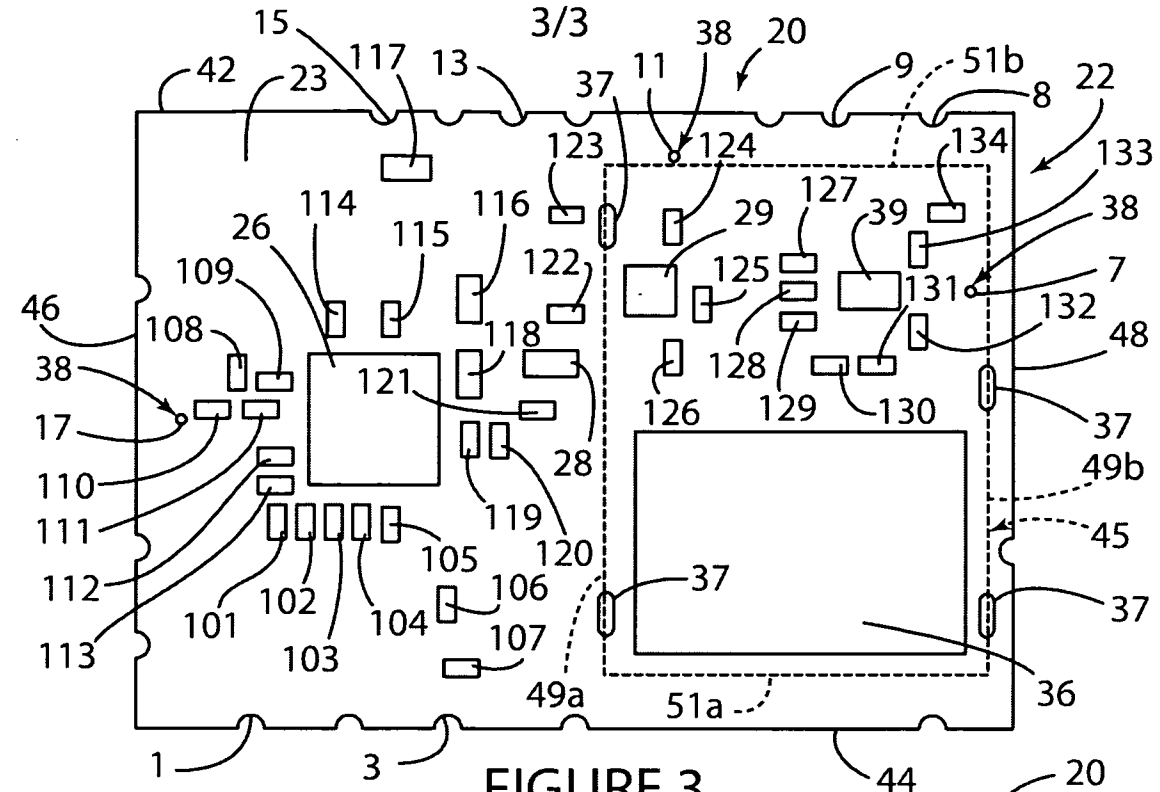

FIGURE 3

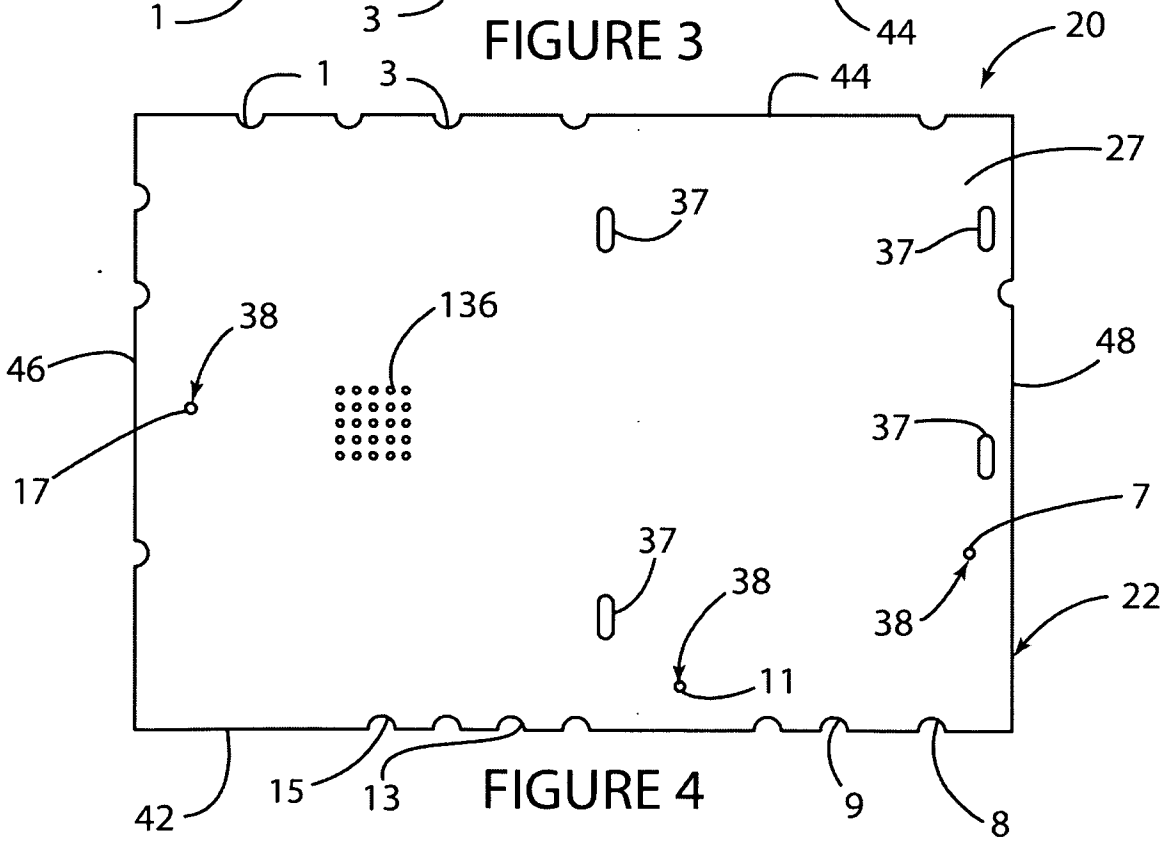

FIGURE 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/007542

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B1/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/043130 A1 (NAGAMORI HIROYUKI [JP] ET AL) 22 November 2001 (2001-11-22) paragraphs [0073] - [0078]; claim 21; figures 6-8	1-13
X	US 2004/240420 A1 (NAKAI SHINYA [JP]) 2 December 2004 (2004-12-02) paragraph [0170] - paragraph [0174]; figures 18-20	1-13
A	EP 0 736 978 A (LK PRODUCTS OY [FI]) 9 October 1996 (1996-10-09) abstract; claims 1-4; figures 1,9-15	1-13
A	WO 93/14573 A (MOTOROLA INC [US]) 22 July 1993 (1993-07-22) abstract; figures 1,2 page 1, line 14 - page 2, line 3	1-13

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 August 2008	10/09/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Kolbe, Werner

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/007542

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 310 705 B1 (LEE JUN-SUNG [KR] ET AL) 30 October 2001 (2001-10-30) abstract; figure 3	1-13
A	US 2005/104685 A1 (KUROKI HIROSHI [JP] ET AL) 19 May 2005 (2005-05-19) abstract; claim 1; figures 1-9	1-13
A	WO 01/05048 A (FILTRONIC LK OY [FI]; HAGSTROEM PANU [FI]) 18 January 2001 (2001-01-18) abstract; claim 1; figures 1-4	1-13

INTERNATIONAL SEARCH REPORT

Information on patent family members

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