AUTOMATIC BEAM STABILIZATION

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The present invention relates to cathode ray tube beam regulation and more especially to an arrangement for regulating the beam current in a cathode ray tube used to store binary information in an electrostatic memory system for a computer.

One problem associated with use of cathode ray tubes as storage elements in memory systems for electronic computers is the faulty operation of the memory due to a variation in tube beam current. In a typical memory system, a binary "1" is stored by directing the beam of electrons to a spot on the inner surface of the tube. The incident beam gives rise to secondary emission of electrons from the phosphor, and leaves a potential "well" which may be detected by directing the beam again at the particular storage spot. A pick up plate placed external to the glass face of the tube serves as one element of a capacitor, with the glass surface being the dielectric and the coating inside the tube being the other capacitor element. The size and shape of the electrical signal detected by the plate and delivered to an associated amplifier depends upon the size and shape of the potential well and the magnitude of the beam current, among other factors. For a complete description of an electrostatic memory see Williams, "Proceedings of The Institution of Electrical Engineers," vol. 96, No. 5, pp. 81—100.

The intensity of the beam current is normally controlled by the bias voltage on the grid of the cathode ray gun which forms and focuses the beam in the tube. Any change in the filament voltage of the tube will, of course, change the beam current. Likewise gun "drift," caused by heating of the parts of the tube during operation, will, by changing the relative positions of the tube elements, change the beam current appreciably. For example, even a 10% change in filament voltage may alter the beam current so appreciably that the size of the signal pulse may change by as much as 75%. It is therefore evident that the magnitude of the beam current must be very closely regulated.

Costly and elaborate filament current regulators might be desirable to maintain that variable constant, but in a memory system comprising some eighty cathode ray tubes, the space and cost requirements of such extra equipment is prohibitive. Moreover, filament current is only one of the several variables contributing to the signal detected from the storage tube, so that controlling it alone would not insure reliable memory operation.

Repealed contamination of spots adjacent any given memory location can cause the potential well to partially refill with the electrons emitted at the adjacent locations. After sufficient number of such read- arounds, any deep potential well, or "0" storage pattern, will appear to be the same as the partially refilled well, or "1" pattern. To allow for such effects in systems of the prior art, the output signal must be sampled only near its extreme positive excursion, above the amplitude of the signal from most refilled "0's." Yet the sampling amplitude should be kept low, because the beam intensity necessary to produce a large positive signal during the first half of the reading cycle for binary "1" unfortunately also produces a large positive signal during the second half of the reading cycle for binary "0." The resulting strobing amplitude setting has been a compromise which severely limits the number of consultations of closely adjacent spots (read- arounds) permissible before the information must be regenerated, and is susceptible to errors caused by even small changes in normal signal amplitude due to tube aging, amplifier drift, and so forth.

With a knowledge of the shortcomings of cathode ray tube utilization in the prior art, applicant has as a primary object of his invention provision of a novel method of and means for controlling the beam current intensity in a cathode ray tube memory system. A special object of the invention is provision of a more accurate, more flexible memory system utilizing cathode ray tubes as storage elements. A further object is to provide a novel mode of operation of cathode ray tube memory systems characterized by greater reliability in access to stored information.

Other objects and many advantages of the invention will be apparent from the following detailed description of a preferred embodiment thereof, when read together with the appended drawings, in which:

Figure 1 illustrates a logical block diagram of a memory system utilizing the present invention.

Figure 2 is a schematic circuit diagram showing a preferred design of a portion of the memory system of Figure 1.

Figure 3 is a pulse routine chart showing the relative sequence required for operation of a memory system constructed according to the invention, and

Figure 4 illustrates sample output waveforms of the binary signals from the tubes.

According to the present invention a binary "1" is recorded in a selected position of the matrix of possible storage spots on each tube. Deflection voltages are set up on the tube deflecting plates periodically to focus the beam on the selected position, and the beam is turned on to "sample" the spot. The signal obtained on the pickup plate is amplified and compared to a reference voltage. The output of the voltage comparison device is used to adjust incrementally the bias voltage on the cathode ray gun so as to rewire the input "1" signal at more nearly the correct amplitude. Errors due to changes in amplification or in beam intensity thus cause a self- adjustment tending to eliminate those errors.

Referring now to the logical diagram of Figure 1, a cathode ray tube 3, which may be of the type RCA 3J1P, forms the storage element. Pick up plate 4 is disposed over the face of the tube and is connected to the input of a wide-band amplifier 5 such as that described by Williams, supra. One output of the amplifier is coupled to Strobe gate 6, a logical "and" gate which may be enabled for a selected interval by a Strobe pulse on lead 10. The output of gate 6 is coupled to one input of a logical "or" gate 16, through which information may be fed into the storage system from lead 17. The output of gate 16 is utilized to set toggle 23, the output of which is coupled to the intensity grid 12 of tube 3 through logical "and" gate 8 and logical "or" gate 2. Gate 2 may also receive beam intensification pulses from lead 1, and transmits them to grid 12. Gate 8 is normally closed, but may be opened by an enabling voltage from toggle 23 so that it will pass rewrite Dash pulses from lead 9.

The output of amplifier 5 is also coupled to the automatic beam stabilization (A. B. S. hereinafter) circuit 13 through logical "and" gate 15 along lead 19, and that cir-
cuit is coupled to the cathode 22 to control the bias on tube 3, which may normally be about —90 volts. "And" gate 15 is enabled or disabled by the output of "and" gate 14, which is the frequency of one memory by the A. B. S. control and timing circuits and a pulse denoted AP from the memory system pulse generator on lead 24. A. B. S. timing is provided by clock 43, which may be a free-running multivibrator circuit, for example, having a frequency which is adjustable so that it may be set equal to or longer than the frequency of one memory by the A. B. S. control and timing circuit. Normally, three memory minor cycles are required for each A. B. S. cycle. Access to the memory is prevented, however, for only two minor cycles. The first minor cycle is required for synchronization, completing the memory cycle already begun, and preventing further execution of orders. The second minor cycle is required for writing a fresh "1" signal on the tubes of the memory at the selected location, and the third minor cycle is utilized for reading the "1" signal and regulating the beam current responsive to the amplitude of that signal. The pulse routine generator for the entire memory is coupled to the A. B. S. control circuit to deliver signals thereto and receive signals therefrom.

Zero location on the raster may be conveniently chosen for storage of the A. B. S. "1" charge pattern because to direct the beam to that location, no deflection signal from either the control counter or regenerator counter, which set up beam deflection voltages, is required. Therefore, the deflection counter may be cleared to zero during the A. B. S. cycle and the regenerator counter may be blocked temporarily without interfering with the A. B. S. operation.

Operation of a typical A. B. S. cycle and its relation to a major memory cycle may be understood from the pulse chain of Figure 3 and the logical diagram of Figure 1. An oscillator or memory clock 21 supplies the timing pulses through appropriate pulse generators 26-32, which receive clock pulses and produce rectangular control pulses of the proper amplitude, width, and frequency for the particular task to be done. Some of the output pulses from the generators begin at the same instance as the incident input pulse, such as pulses AP, TD, Dash, Dot, A, B, and C on leads 24, 30-35. Other output pulses begin at the end of the input pulse, such as the pulses on lead 36-41. Between A. B. S. memory cycles, the right-hand halves of the toggles are conducting, such that a "positive" (enabling) signal may be taken on the respective output leads therefrom, and a "negative" (disabling) signal from the left-hand halves of the toggles.

**Synchronization cycle**

At selected intervals, clock 43 will produce a pulse on lead 44, flipping toggle 45 so that the left side becomes conducting. "And" gate 46, normally disabled by the voltage on lead 47, thereby becomes enabled. The next Dash pulse occurring on lead 31 will then pass through gate 46 and flip toggle 49, changing the potential on lead 50 so as to disable or block "and" gate 51. When the subsequent "Dash end" pulse on lead 38 arrives at gate 51, it cannot pass through to trip pulse generators 30-32; therefore, pulses A, B, and C will not be produced. Because the pulse output A, B, C starts and controls the arithmetic cycle, no such cycle may be started by the computer while during an A. B. S. cycle. The signal on lead 59 is changed from "negative" to "positive" as toggle 49 flips, and "or" gate 56 delivers a corresponding "positive" signal on lead 57, actuating "and" gate 56 to enable "and" gate 58. "And" gates 56, 59 are also enabled by the "positive" signal on lead 59.

**Writing cycle**

A new cycle may be started by a memory clock signal, actualizing Dot pulse generator 27 and AP pulse generator 26. Since the "and" gate 53 is enabled, the pulse generated on lead 32 will pass through that gate, through "or" gate 56, travel along lead 1 to "or" gate 2, and through gate 2 to grid 12 of the tube 3 to intensify the electron beam. The Dot pulse from gate 56 is also sent along lead 65 to gate 66, but that gate is disabled by the "negative" signal on lead 67. Simultaneously with the Dot pulse, the AP pulse is generated on leads 24, 72, and delivered to "and" gates 14, 73. Gate 73 is enabled by a signal from the address toggle corresponding to zero position on the raster, so that the pulse passes through to gate 74. The Stroke pulse generator cycle. Normally, three memory minor cycles are required for each A. B. S. cycle. Access to the memory is prevented, however, for only two minor cycles. The first minor cycle is required for synchronization, completing the memory cycle already begun, and preventing further execution of orders. The second minor cycle is required for writing a fresh "1" signal on the tubes of the memory at the selected location, and the third minor cycle is utilized for reading the "1" signal and regulating the beam current responsive to the amplitude of that signal. The pulse routine generator for the entire memory is coupled to the A. B. S. control circuit to deliver signals thereto and receive signals therefrom.

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**Current regulation cycle**

The next pulse from clock 21 initiates another pulse train as shown in Figure 3 and described above. The Dot pulse from lead 1 will again intensify the beam in tube 3, causing a signal to appear at the output of amplifier 5. The Dot pulse will also travel along lead 65 and pass through enabled gate 66 to flip toggle 49 back to its normal position, changing the signal on lead 50 to enable gate 51, and changing the signal on lead 59 to disable gate 60. Simultaneously, AP and Stroke pulses are delivered to gates 14, 6, respectively, the former pulse passing gate 14 to enable gate 15. The amplifier output pulse is coupled back to open gate 15, and is passed to the A. B. S. circuit 15, where it causes an incremental adjustment in beam current tending to correct any departure of the amplifier signal from the selected amplitude, as is more fully described hereinafter. The subsequent AP End pulse from lead 68 will not pass gate 69, now blocked by the signal from toggle 49. Likewise the next TD pulse on lead 30 is blocked through the disabling of gate 60 by the signal on lead 59 from toggle 49. The following Dash pulse on lead 31 is also blocked at gate 46 by the disabling signal from toggle 45 on lead 47, but may pass simultaneously through open gate 62, gate 56, and gate 2.
and through open gates $g_9$, $g_8$ and gate $g_2$ to turn on the beam in tube 3 at the re-write position. Thus a fresh "1" signal is regenerated at the zero raster position. The following Dash End pulse is delivered to gate 51, which is now enabled by the signal on lead $g_9$, and passes along lead 52 to trip pulse generator 30 to produce the A pulse on lead $g_{33}'$ and a further trigger pulse on lead $g_{39}$. Generators 31, 32 are triggered in sequence to produce the B and C pulses, which, together with pulse A, start a new scanning cycle in the arithmetic unit of the associated computer.

Referring now to Figure 2, a preferred embodiment of the A.B.S. circuit is illustrated. Cathode ray tube 3, including cathode 22 and intensity grid 12, is provided with a pickup plate 4 coupled to the input of amplifier 5. The output of the amplifier is coupled to the discriminator circuit shown in Figure 1 and also to the "and" gate 15 along lead 19. The logical gate 15 may comprise a difference amplifier circuit including twin-triode tube 70, potentiometer 71 in the grid return circuit of the left half of tube 70, and input leads 19, 71'. The right-hand grid of tube 70 is normally held at $+40$ volts by the output of gate 14 while the left-hand grid is held at ground or below, so that the right half of tube 70 conducts heavily and the left section is cut off. Potentiometer 71 may be adjusted to select the desired amplitude for the "1" signals since it determines the quiescence from which the left-hand grid of tube 70 is normalized at $+40$ volts. The signal developed on lead 19 during the AP pulse interval is greater than the bias voltage and therefore greater than the desired "1" amplitude, the left section of tube 70 will begin to conduct, cutting off the right section. When the pulse lead 19 decays away or the voltage on lead 71' is again raised to $+40$ volts, the right section will again conduct and the left section will be cut off. Therefore, a positive pulse of relatively short duration is formed on lead 72 by the switching action of tube 70.

This positive pulse is lengthened in two steps: it is R-C coupled to cathode follower 73 through a network 74, 75 of relatively long time constant, such as 470,000 ohms resistor 75 and .001 microfarad condenser 74. The distributed capacitance and Intercapacitance of the tube also contribute to the pulse lengthening and are indicated by dotted condenser 76. The output of tube 73 is coupled through condenser 77 to the grid of tube 78 for a second lengthening step. A source of regulated high negative voltage 79, which may be substantially $-2500$ volts, is provided with bleeder network 88. The grids of the plate, grid, and cathode voltages of tube 78 at point 81, potentiometer arm 82, and point 83, respectively.

A further negative supply 84 is floated on the high voltage supply 79 and utilized to supply energizing voltages to triode 85. The cathode of triode 85 is coupled to the most negative terminal of supply 84 which may be substantially $-2650$ volts with respect to ground, while the anode is coupled through 2000 ohm resistor 86 to point 83. The control grid of triode 85 is coupled through condenser 87 to a source of negative pulses designed to cut off current through the tube and through 100,000 ohm resistor 88 to point 83. 1 microfarad condenser 89 is coupled between points $g_1$ and $g_8$ on divider 89 and acts as a storage capacitor. A voltage large resistance 90, which may be 100 megohms, couples the cathode of tube 78 to point 83, and is shunted by large condenser 91, which may be 1 microfarad, to provide a very long time constant for lengthening or sustaining the input pulse from condenser 77 to tube 78. The cathode of tube 78 is coupled directly to the cathode 22 of tube 3, while the grid 12 of tube 3 is coupled directly to the anode of tube 85.

The intensity of beam current in tube 3 depends upon the bias voltage between grid 12 and cathode 22, which voltage is determined by the drop across resistor 86 plus the voltage across condenser 91. Tube 78 is normally cut off, despite the small positive grid bias from arm 82, because its cathode voltage is held up to the peak value of the incoming positive pulses by the large condenser 91 and also because of only a small amount of current, less than 5 milliamperes, flows through network 86 to establish the positive grid bias. Condenser 89 is provided as an accumulator to store up charge from the relatively small voltage drop due to the bleeder current. Tube 85 normally conducts heavily, because of the coupling resistor 88.

During the Current regulation cycle, described, a beam turn-on negative pulse applied to condenser 87 from gate 2 of the discriminator will drive the connected grid below cut off, stop conduction through tube 85, and raise the potential of lead 92 to that of supply terminal 83, which rise is sufficient to turn on the cathode-ray tube beam, the only remaining bias voltage being that on condenser 91. The resulting signal is detected, amplified, and if too large, will cause a positive signal input to tube 78. That tube will begin to conduct heavily as condenser 89 discharges through the tube, thereby further charging up condenser 91. Thus the cathode-ray tube bias is increased by a voltage determined by the amount of charge transferred between condensers 89, 91. It is apparent that condenser 91 will continuously discharge through resistor 90, so that the presence of a positive pulse input to tube 78 at the appropriate A.B.S. sampling time allows a reduction of the charge on the condenser and a reduction in cathode-ray tube bias. Thus signals which are too small to switch the current through tube 70 will result in a greater beam current.

The setting of arm 82 determines the firing voltage of tube 78, and thereby determines the duration of the period of tube conduction responsive to a positive input pulse, so that it also determines the increment of charge per cycle transferred to condenser 91 to change the bias voltage.

Having described his invention, applicant claims as novel:

1. An improved memory system of the type utilizing a cathode ray tube for storage of binary information, a storage surface in said tube, means for forming a beam in said tube and directing it toward said surface, and a pickup plate disposed adjacent the tube face, comprising means for storing binary reference signal in a predetermined raster position of said tube face, means for forming said beam periodically to said position to sample the information stored, means for amplifying the signal induced in said plate when said beam is directed to said location, bias circuit connected between the cathode and control grid of said tube, means for continuously decreasing the bias voltage across said circuit to increase the intensity of said beam, and means for periodically decreasing the intensity of said beam comprising normally disabled circuit means for deriving a signal proportional to the difference in amplitude of two input signals and provided with a first input coupled to said amplifying means, a second input, and an output coupled to said bias circuit to increase the bias voltage responsive to said derived signal, a source of reference potential coupled to said second input, and means for periodically enabling said circuit means to turn on said beam at said predetermined position.

2. In a memory system comprising a cathode ray tube, a pick up plate coupled to the screen thereof, an amplifier coupled to said plate, means for establishing an electron beam within said tube, electrodes for deflecting said beam about said tube to a raster of position responsive to a source of control voltages, and means for determining the intensity of said beam, the improvement comprising a grid driver stage provided with input and output circuits, said output circuit being coupled to said grid for determining the voltage impressed thereon, a difference amplifier having two input circuits and an output circuit, said output circuit being coupled to the input of said driver stage, one input being coupled to said amplifier output circuit, first and second sources of reference potentials.
coupled respectively to said input circuits of the difference amplifier a source of reference voltage pulses coupled to the other input of the driver stage, a clock pulse generator coupled to said sources of reference pulses for timing said pulses, and means responsive to said clock pulse generator for periodically directing said beam to a selected raster position to produce a reference signal for said difference amplifier.

3. In a cathode ray tube storage system including a storage tube provided with a control grid and a cathode, a pickup device, and an amplifier, the improvement comprising: means for producing an electrical impulse of magnitude proportional to the deviation of the amplitude of the output of signal over a standard amplitude; a first pulse lengthening circuit coupled to said pulse producing means to sustain the crest amplitude of said pulse; a second pulse lengthening circuit provided with a storage condenser and coupled to said first lengthening circuit to further sustain the crest amplitude of said pulse; a bias circuit comprising a first resistor connected in series with said storage condenser between the cathode and control grid of said storage tube; a source of current and a switching device connected in series across said first resistor to normally supply a bias current therethrough; means for periodically cutting off current flow through said first resistor to reduce said bias and turn on said cathode ray beam; and a discharge resistor connected in shunt with said storage condenser to continuously lower the bias voltage on said cathode ray tube, actuation of said second lengthening circuit responsive to a signal greater than said standard amplitude increasing the charge stored on said condenser, thereby increasing the bias on said cathode ray tube.

4. In a cathode ray tube storage system a bias network comprising first and second resistances connected in series between the grid and cathode of said tube and a storage condenser connected in parallel with said second resistor; first and second current switching devices connected respectively to said resistors, said first device being normally conducting and said second device being normally non-conducting; respective voltage sources connected to energize said switching devices; a second condenser coupled to one of said sources for charging therefrom; means for periodically interrupting the current through said first switching device and its associated resistor, thereby lowering the bias voltage and turning on the cathode ray beam; circuit means responsive to the amplitude of the signal voltage produced by said beam turn on for actuating said second switching device only if said signal is greater than a pre-determined magnitude; said second condenser being coupled in series with said second switching device and its resistor to charge said first condenser while current flows through said second device, the increased charge on said storage condenser increasing the bias voltage of said tube and reducing the beam current thereof.

5. In an improved memory system of the type comprising a cathode ray tube, a source of electrons, a storage surface, means for accelerating a beam of electrons toward said storage surface, means including a bias voltage for cutting off said beam, means for directing said beam about said surface to discrete raster of points, in response to a series of order voltages, a pickup electrode adjacent said surface, and an amplifier coupled to said electrode, the improvement comprising: means for periodically interrupting said directing means, means for establishing a selected order voltage on said directing means to direct said beam to a selected raster point after each interruption, means for establishing a selected charge pattern on said surface at said selected point, means for re-intensifying said beam at said point to produce a signal responsive to interrogation of said charge pattern, a source of reference voltage, means for comparing said signal and said voltage to produce a correction signal, means for continuously decreasing the magnitude of said bias voltage, and means for incrementally increasing the magnitude of said bias voltage responsive to each said correction signal to control said beam intensity.

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