Title: THERMAL RESISTOR IN MTJ STACK DESIGN

Abstract: Disclosed are magnetic tunnel junction (MTJ) devices, computing devices, and related methods. An MTJ device includes an MTJ body, an electrode, and a thermal resistor. The thermal resistor is operably coupled between the MTJ body and the electrode. The thermal resistor includes at least one conductive region including an electrically conductive material. A computing device includes a memory device including at least one MTJ device, which in turn includes at least one thermal resistor between an MTJ body and at least one of a pair of electrodes. A method of forming an MTJ device includes forming an MTJ body, forming at least one electrode, and forming at least one electrically conductive thermal resistor between the MTJ body and the at least one electrode.
THERMAL RESISTOR IN PMTJ STACK DESIGN

Background

[0001] Magnetic tunnel junction (MTJ) devices (e.g., perpendicular MTJ devices, or equivalently PMTJ devices) leverage quantum mechanical effects of placing a thin electrically insulating material between two ferromagnets. Specifically, in MTJ devices, electrons tunnel from one ferromagnet to the other through the electrically insulating material. A direction of polarization of at least one of the two ferromagnets can be independently controlled. When the directions of polarization of the two ferromagnets are the same, an electrical resistance across the MTJ device is relatively low. When the directions of polarization of the two ferromagnets are different (e.g., opposite), the electrical resistance across the MTJ device is relatively high.

[0002] One example of an MTJ device is a spin-transfer torque (STT) memory storage unit, which is the basic storage unit used in STT random access memory (STT-RAM, or STT-MRAM) devices. In STT-RAM devices, different states, including a parallel state (in which the two ferromagnets are polarized in the same direction) and an antiparallel state (in which the two ferromagnets are polarized in opposite directions) can be set by applying different electrical currents. The state can then be read by measuring the electrical resistance (e.g., by applying an electrical read current and measuring a resulting voltage drop) of the MTJ device. If the measured resistance is relatively high, it can be determined that the MTJ device is in the antiparallel state. If the measured resistance is relatively low, it can be determined that the MTJ device is in the parallel state. Different logic levels (e.g., logic levels "1" and "0") can be assigned to each of the parallel and antiparallel states, enabling digital information to be stored in arrays of MTJ devices.

Brief Description of the Drawings

[0003] FIG. 1 is a simplified cross-sectional view of an example MTJ device.

[0004] FIG. 2 is a simplified cross-sectional view of an MTJ device, according to some embodiments.

[0005] FIG. 3 is a simplified cross-sectional view of another MTJ device, according to some embodiments.
FIG. 4 is a simplified cross-sectional view of yet another MTJ device, according to some embodiments.

FIG. 5 is a simplified block diagram of a memory device, according to some embodiments.

FIG. 6 is a simplified flowchart illustrating a method of forming an MTJ device, according to some embodiments.

FIG. 7 illustrates an interposer that includes one or more embodiments discussed herein.

FIG. 8 illustrates a computing device, according to some embodiments.

Detailed Description

Disclosed herein are MTJ devices, computing systems, and related methods that use thermal resistors to retain at least a portion of heat generated within MTJ devices, thereby reducing a magnitude of control currents for switching the MTJ device between different operational states. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. It will be apparent to one skilled in the art, however, that the disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the disclosure. The order in which the operations are presented in the description, however, should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation. Rather, in some embodiments, the order may be modified.

The terms "over," "under," "between," and "on" as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be
directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0014] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator (SOI) substructure (e.g., silicon-on-glass (SOG), silicon-on-sapphire (SOS), etc.). In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the disclosure.

[0015] One or more MTJ devices (e.g., STT-RAM storage units) may be fabricated on or in a substrate. In various implementations, the MTJ devices may be described as a stack of different functional regions. This geometric structure should not, however, be interpreted as limiting. As will be apparent to those skilled in the art, MTJ devices may be formed horizontally, radially, or otherwise, as well as vertically.

[0016] FIG. 1 is a simplified cross-sectional view of an example MTJ device 100. The MTJ device 100 includes a stack 180 including an MTJ body 190 operably coupled between electrodes 110, 170. The MTJ body 190 includes an oxide region 140 including an oxide material (e.g., magnesium oxide (MgO)) between a reference region 150 and a free region 130. The reference region 150 and the free region 130 each include ferromagnets. By way of non-limiting example, the free region 130 may include a cobalt iron barium (CoFeB) stack including a metallic insert between two
CoFeB regions. Also by way of non-limiting example, the reference region may include CoFeB.

[0017] The electrodes 110, 170 include electrically conductive material (e.g., titanium, aluminum, copper, tungsten, polysilicon, alloys, etc.). The electrodes 110, 170 are configured to conduct control currents I_c through the MTJ body 190. A direction of a magnetic polarization of the free region 130 may be controllable through application of the control currents I_c through the MTJ body 190. Also, a read of a current state (e.g., a parallel state, an antiparallel state) of the MTJ body 190 may be determined through application of the control currents I_c through the MTJ body 190.

[0018] In some embodiments, the stack 180 includes a cap region 120 including a metal (e.g., MgO). The cap region 120 is configured to improve operational stability of the MTJ device 100. In some embodiments, the stack 180 includes a synthetic antiferromagnet (SAF) region 160 including a magnet (e.g., layers of cobalt platinum). The SAF region 160 is also configured to improve operational stability of the MTJ device 100.

[0019] In order to switch the operation state of the MTJ body 190 between the parallel and antiparallel states, the control current I_c is controlled to exceed certain thresholds. These threshold current levels can often exceed a capacity that transistors have for supplying currents. An increased temperature of the MTJ body 190, however, decreases the threshold current levels for switching the MTJ body 190 between the parallel and antiparallel states. As current passes through the MTJ body 190, the oxide region 140 produces some heat. Much of this heat generated by the oxide region 140, however, escapes through the conductive regions (e.g., the cap region 120, the SAF region 160, and the electrodes 110, 170) of the MTJ stack 180. As a result, the MTJ device 100 may draw more current than a transistor is capable of supplying.

[0020] Disclosed herein are MTJ devices including thermal resistors configured to retain heat within an MTJ body, decreasing threshold current levels for switching the MTJ body between operational states.

[0021] In some embodiments, disclosed herein is an MTJ device including an MTJ body. The MTJ body includes a free region, a reference region, and an oxide region.
The free region includes a ferromagnetic material, the reference region includes a ferromagnetic material, and the oxide region includes an oxide material between the free region and the reference region. The MTJ device also includes an electrode including electrically conductive material and a thermal resistor operably coupled between the MTJ body and the electrode. The thermal resistor includes at least one conductive region including electrically conductive material.

[0022] In some embodiments, disclosed herein is a method of forming an MTJ device. The method includes forming an MTJ body including a free region, a reference region, and an oxide region between the free region and the reference region. The method also includes forming at least one electrode including conductive material configured to conduct electrical current at least one of to or from the MTJ body. The method further includes forming at least one electrically conductive thermal resistor between the MTJ body and the at least one electrode.

[0023] In some embodiments, disclosed herein is a computing device including a memory device configured to electrically store data. The memory device includes at least one MTJ device including a pair of electrodes, an MTJ body including an oxide region between a reference region and a free region, the MTJ body between the pair of electrodes. The MTJ device also includes at least one thermal resistor including at least one electrically conductive region between the MTJ body and at least one of the pair of electrodes.

[0024] FIG. 2 is a simplified cross-sectional view of an MTJ device 200, according to some embodiments. The MTJ device 200 includes an MTJ stack 280 similar to the MTJ stack 180 of FIG. 1 except that the MTJ stack 280 includes a thermal resistor 202 ("thermal R" 202) configured to prevent at least a portion of heat generated by an MTJ body 290 of the MTJ device 200 from escaping the MTJ body 290. In other words, the cap region 220 is operably coupled between the free region 230 of the MTJ body 290 and the thermal resistor 202. As a result, an operational temperature of the MTJ device 200 is higher than an operational temperature of the MTJ device 100 of FIG. 1. Accordingly, lower magnitude control current Ic may be used to switch the operational state of the MTJ body 290 than that used to switch the operational state of the MTJ body 190 of FIG. 1.
In some embodiments, the thermal R 202 is at least about 100 Angstroms thick. In some embodiments, the thermal R 202 is less than or equal to about 500 Angstroms thick.

In some embodiments, the thermal R 202 includes at least one conductive region including an electrically conductive material. Interfaces between adjacent conductive materials (e.g., between the thermal R 202 and the electrode 210, between different conductive regions of the thermal R 202, etc.) introduce thermal boundary resistances. By way of non-limiting example, the thermal R 202 may include a single electrically conductive material that is different from a conductive material of the electrode 210. Accordingly, an interface between two different conductive materials is created at the interface between the electrode 210 and the thermal R 202.

Multiple resistances in series incur a relatively large thermal resistance, which leads to higher temperatures in the MTJ free region 230 during a write operation. By way of non-limiting example, the thermal R 202 itself may include multiple conductive regions (e.g., at least two), each of which includes a different one of at least two different electrically conductive materials. By way of non-limiting example, the at least two different electrically conductive materials may include at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO).

In embodiments where the thermal R 202 includes a multi-layer structure including at least two different conductive materials, the interfaces between the layers are designed to increase thermal resistance, thereby raising a temperature in the free region 230 and/or creating a thermal gradient across the MTJ stack 280. As a result, self-heating temperature rise caused by Joule heating across the oxide region 240 results from the thermal R 202, reducing the magnitude of the control current Ic to switch between operational states of the MTJ body 290. The greater the number of interfaces of different conductive layers of the thermal R 202, the greater the resulting thermal resistance without raising the overall electrical resistance.
[0029] The MTJ device 200 includes the MTJ body 290 including a reference region 250, a free region 230, and an oxide region 240 between the reference region 250 and the free region 230, similar to the reference region 150, the oxide region 140, and the free region 130 discussed above with reference to FIG. 1. The MTJ device 200 also includes electrodes 210, 270, similar to the electrodes 110, 170 of FIG. 1. In some embodiments, the MTJ device 200 further includes one or more of a cap region 220 and a SAF region 260, similar to the cap region 120 and the SAF region 160 of FIG. 1.

[0030] In some embodiments, a thermal R may be included between other components of the MTJ stack 280 other than, or in addition to, between the cap region 220 and the SAF region 260. Such thermal R may be included between any of the components shown in the MTJ stack 280. FIGS. 3 and 4 illustrate two such examples. As another non-limiting example, the SAF 260 may be operably coupled between the thermal R 202 and the electrode 270. As a further non-limiting example, the cap region 220 may be operably coupled between the thermal R 202 and the electrode 210. Other examples will be apparent to those of ordinary skill in the art in view of the disclosure.

[0031] FIG. 3 is a simplified cross-sectional view of another MTJ device 300, according to some embodiments. The MTJ device 300 includes an MTJ stack 380 that is similar to the MTJ stack 280 of FIG. 2 except that the MTJ stack 380 includes a thermal R 302 between the SAF region 260 and the electrode 270 in addition to the thermal R 202 between the cap region 220 and the electrode 210. With the additional thermal R 302, heat may be retained even better in the free region 230 of the MTJ device 300 than in the free region 230 of the MTJ device 200 of FIG. 2.

[0032] FIG. 4 is a simplified cross-sectional view of yet another MTJ device 400, according to some embodiments. The MTJ device 400 includes an MTJ stack 480 that is similar to the MTJ stack 280 of FIG. 2 except that the MTJ stack 380 includes a thermal R 402 between the SAF region 260 and the electrode 270 instead of the thermal R 202 between the cap region 220 and the electrode 210. In other words, the SAF region 260 is operably coupled between the reference region of the MTJ body and the thermal R 402.
FIG. 5 is a simplified block diagram of a memory device 500, according to some embodiments. The memory device 500 includes memory control circuitry 510 operably coupled to an array of cells 520. At least one of the cells in the array of cells 520 includes an MTJ device 200, 300, 400 (FIGS. 2, 3, and 4) including at least one thermal resistor 202, 302, 402 (FIGS. 2, 3, and 4), as discussed above.

The memory control circuitry 510 is configured to provide control currents $I_c$ (e.g., read currents, write currents, etc.) to the array of cells 520. Since at least one of the cells in the array of cells 520 includes a thermal resistor 202, 302, 402, the memory control circuitry 510 may be configured to provide write currents of less magnitude than if no thermal resistor 202, 302, 402 were included. Accordingly, in some embodiments, the memory control circuitry may supply write currents driven by a single transistor.

FIG. 6 is a simplified flowchart illustrating a method 600 of forming an MTJ device 200, 300, 400, according to some embodiments. Referring to FIGS. 2, 3, 4, and 6 together, the method 600 includes forming 610 an MTJ body 290 including a free region 230, a reference region 250, and an oxide region 240 between the free region 230 and the reference region 250.

The method 600 also includes forming 620 at least one electrode 210, 270 including conductive material configured to conduct electrical current at least one of the or from the MTJ body 290.

The method 600 further includes forming 630 at least one electrically conductive thermal resistor 202, 302, 402 between the MTJ body 290 and the at least one electrode 210, 270. In some embodiments, forming the at least one electrically conductive thermal resistor 202, 302, 402 includes forming a plurality of interfaces between different conductive materials of the thermal resistor 202, 302, 402. In some embodiments, forming a plurality of interfaces between different conductive materials includes forming the plurality of interfaces between at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), and tantalum nitride (TaN). In some embodiments, forming at least one electrically conductive thermal resistor 202, 302, 402 includes forming a plurality of electrically conductive thermal resistors 202, 302, 402.
FIG. 7 illustrates an interposer 1000 that includes one or more embodiments discussed herein. The interposer 1000 is an intervening substrate used to bridge a first substrate 1002 to a second substrate 1004. The first substrate 1002 may be, for instance, an integrated circuit die. The second substrate 1004 may be, for instance, a memory module (e.g., the memory device 500 of FIG. 5), a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1000 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1000 may couple an integrated circuit die to a ball grid array (BGA) 1006 that can subsequently be coupled to the second substrate 1004. In some embodiments, the first and second substrates 1002/1004 are attached to opposing sides of the interposer 1000. In other embodiments, the first and second substrates 1002/1004 are attached to the same side of the interposer 1000. And in further embodiments, three or more substrates are interconnected by way of the interposer 1000.

The interposer 1000 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer 1000 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer 1000 may include metal interconnects 1008 and vias 1010, including but not limited to through-silicon vias (TSVs) 1012. The interposer 1000 may further include embedded devices 1014, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1000.

In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer 1000.

FIG. 8 illustrates a computing device 1200, according to some embodiments. The computing device 1200 may include a number of components. In one
embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die, such as an SoC used for mobile devices. The components in the computing device 1200 include, but are not limited to, an integrated circuit die 1202 and at least one communications logic unit 1208. In some implementations the communications logic unit 1208 is fabricated within the integrated circuit die 1202 while in other implementations the communications logic unit 1208 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 1202. The integrated circuit die 1202 may include a CPU 1204 as well as on-die memory 1206, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM), SRAM, or spin-transfer torque memory (STT-MRAM) (e.g., such as the memory device 500 of FIG. 5).

[0043] Computing device 1200 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 1210 (e.g., DRAM), non-volatile memory 1212 (e.g., ROM or flash memory, the memory device 500 of FIG. 5, etc.), a graphics processing unit 1214 (GPU), a digital signal processor 1216, a crypto processor 1242 (e.g., a specialized processor that executes cryptographic algorithms within hardware), a chipset 1220, at least one antenna 1222 (in some implementations two or more antenna may be used), a display or a touchscreen display 1224, a touchscreen controller 1226, a battery 1229 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 1228, a compass (not shown), a motion coprocessor or sensors 1232 (that may include an accelerometer, a gyroscope, and a compass), a microphone (not shown), a speaker 1234, a camera 1236, user input devices 1238 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 1240 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). The computing device 1200 may incorporate further transmission, telecommunication, or radio functionality not already described herein. In some implementations, the computing device 1200 includes a radio that is used to communicate over a distance by modulating and radiating electromagnetic waves in
air or space. In further implementations, the computing device 1200 includes a transmitter and a receiver (or a transceiver) that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space.

[0044] The communications logic unit 1208 enables wireless communications for the transfer of data to and from the computing device 1200. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 1208 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Infrared (IR), Near Field Communication (NFC), Bluetooth, and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1200 may include a plurality of communications logic units 1208. For instance, a first communications logic unit 1208 may be dedicated to shorter range wireless communications such as Wi-Fi, NFC, and Bluetooth and a second communications logic unit 1208 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0045] In some embodiments, the processor 1204 of the computing device 1200 includes one or more devices, such as MTJ devices 200, 300, 400, that are formed in accordance with embodiments disclosed herein. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0046] The communications logic unit 1208 may also include one or more devices, such as MTJ device 200, 300, 400, that are formed in accordance with embodiments disclosed herein.

[0047] In further embodiments, another component housed within the computing device 1200 may contain one or more devices, such as MTJ device 200, 300, 400, that are formed in accordance with implementations disclosed herein.
In various embodiments, the computing device 1200 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a dumbphone, a tablet, a tablet/laptop hybrid, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1200 may be any other electronic device that processes data.

Examples

The following is a list of example embodiments that fall within the scope of the disclosure. In order to avoid complexity in providing the disclosure, not all of the examples listed below are separately and explicitly disclosed as having been contemplated herein as combinable with all of the others of the examples listed below and other embodiments disclosed hereinabove. Unless one of ordinary skill in the art would understand that these examples listed below, and the above disclosed embodiments, are not combinable, it is contemplated within the scope of the disclosure that such examples and embodiments are combinable.

Example 1: A magnetic tunnel junction (MTJ) device, including: an MTJ body, including: a free region including a ferromagnetic material; a reference region including a ferromagnetic material; and an oxide region including an oxide material between the free region and the reference region; an electrode including electrically conductive material; and a thermal resistor operably coupled between the MTJ body and the electrode, the thermal resistor including at least one conductive region including an electrically conductive material.

Example 2: The MTJ device of Example 1, wherein the at least one conductive region of the thermal resistor includes at least two conductive regions, each conductive region of the at least two conductive regions including a different one of at least two different electrically conductive materials.

Example 3: The MTJ device of Example 2, wherein the at least two different electrically conductive materials include at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO).
[0053] Example 4: The MTJ device according to any one of Examples 1-3, further including a synthetic antiferromagnet (SAF) operably coupled between the reference region of the MTJ body and the thermal resistor.

[0054] Example 5: The MTJ device according to any one of Examples 1-4, further including a synthetic antiferromagnet (SAF) operably coupled between the thermal resistor and the electrode.

[0055] Example 6: The MTJ device according to any one of Examples 1-5, further including a cap region including an electrically conductive material operably coupled between the free region of the MTJ body and the thermal resistor.

[0056] Example 7: The MTJ device according to any one of Examples 1-6, further including a cap region including an electrically conductive material operably coupled between the thermal resistor and the electrode.

[0057] Example 8: The MTJ device according to any one of Examples 1-7, further including: another electrode including electrically conductive material and located opposite the electrode across the MTJ body; and another thermal resistor operably coupled between the MTJ body and the other electrode, the other thermal resistor including at least one other conductive region including an electrically conductive material.

[0058] Example 9: The MTJ device according to any one of Examples 1-8, wherein at least one of the free region and the reference region includes a metallic insert region between two CoFeB regions.

[0059] Example 10: The MTJ device according to any one of Examples 1-9, wherein the oxide region includes magnesium oxide (MgO).

[0060] Example 11: The MTJ device according to any one of Examples 1-10, further including at least one other thermal resistor configured to retain heat generated by current passing through the MTJ body.

[0061] Example 12: A method of forming a magnetic tunnel junction (MTJ) device, the method including: forming an MTJ body including a free region, a reference region, and an oxide region between the free region and the reference region; forming at least one electrode including conductive material configured to conduct electrical current at least one of to or from the MTJ body; and forming at least one
electrically conductive thermal resistor between the MTJ body and the at least one electrode.

[0062] Example 13: The method of Example 12, wherein forming the at least one electrically conductive thermal resistor includes forming a plurality of interfaces between different conductive materials.

[0063] Example 14: The method of Example 13, wherein forming a plurality of interfaces between different conductive materials includes forming the plurality of interfaces between at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO).

[0064] Example 15: The method according to any one of Examples 12-14, wherein forming at least one electrically conductive thermal resistor includes forming a plurality of electrically conductive thermal resistors.

[0065] Example 16: A computing device, including: a memory device configured to electrically store data, the memory device including: at least one magnetic tunnel junction (MTJ) device including: a pair of electrodes; an MTJ body including an oxide region between a reference region and a free region, the MTJ body between the pair of electrodes; and at least one thermal resistor including at least one electrically conductive region between the MTJ body and at least one of the pair of electrodes.

[0066] Example 17: The computing device of Example 16, further including at least one device selected from the group consisting of: a processor mounted to a substrate, a graphics processing unit, an antenna within the computing device, a display on the computing device, a battery within the computing device, a power amplifier within the processor, and a voltage regulator within the processor.

[0067] Example 18: The computing device according to any one of Examples 16 and 17, wherein the at least one thermal resistor is less than or equal to about 500 Angstroms thick.

[0068] Example 19: The computing device according to any one of Examples 16-18, wherein the at least one thermal resistor is at least about 100 Angstroms thick.

[0069] Example 20: The computing device according to any one of Examples 16-18, wherein the memory device includes a spin-transfer torque (STT) random access memory device.
Example 21: A method of operating a magnetic tunnel junction (MTJ) device, the method including: applying an electrical control current to an electrode of the MTJ device, the electrode including electrically conductive material, the electrical control current configured to at least one of control and detect an operational state of an MTJ body of the MTJ device; and preventing heat generated by the MTJ body responsive to the electrical control current from escaping the MTJ body using a thermal resistor operably coupled between the MTJ body and the electrode, the thermal resistor including at least one conductive region including an electrically conductive material.

Example 22: The method of Example 21, wherein preventing heat generated by the MTJ body from escaping the MTJ body using a thermal resistor including at least one conductive region includes preventing the heat from escaping using a thermal resistor including at least two conductive regions, each conductive region of the at least two conductive regions including a different one of at least two different electrically conductive materials.

Example 23: The method of Example 22, wherein preventing the heat from escaping using a thermal resistor including at least two conductive regions the at least two different electrically conductive materials includes preventing the heat from escaping using a thermal resistor including at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO).

Example 24: The method according to any one of Examples 21 and 23, wherein preventing heat generated by the MTJ body from escaping the MTJ body includes preventing the heat from escaping using a thermal resistor separated from the MTJ body by a synthetic antiferromagnet (SAF).

Example 25: The method according to any one of Examples 21-24, wherein preventing heat generated by the MTJ body from escaping the MTJ body includes preventing the heat from escaping using a thermal resistor separated from the electrode by a synthetic antiferromagnet (SAF).

Example 26: The method according to any one of Examples 21-25, wherein preventing heat generated by the MTJ body from escaping the MTJ body includes
preventing the heat from escaping using a thermal resistor separated from the MTJ body by a cap region including an electrically conductive material.

[0076] Example 27: The method according to any one of Examples 21-26, wherein preventing heat generated by the MTJ body from escaping the MTJ body includes preventing the heat from escaping using a thermal resistor separated from the electrode by a cap region including an electrically conductive material.

[0077] Example 28: The method according to any one of Examples 21-27, further including: conducting the electrical control current with another electrode including electrically conductive material and located opposite the electrode across the MTJ body; and preventing the heat generated by the MTJ body from escaping the MTJ body using another thermal resistor operably coupled between the MTJ body and the other electrode, the other thermal resistor including at least one other conductive region including an electrically conductive material.

[0078] Example 29: The method according to any one of Examples 21-28, further including conducting the electrical control current to the MTJ device including a free region, a reference region, and an insulating region between the free region and the reference region, at least one of the free region and the reference region including a metallic insert region between two CoFeB regions.

[0079] Example 30: The method of Example 29, wherein the insulating region includes magnesium oxide (MgO).

[0080] Example 31: The method according to any one of Examples 21-30, further including preventing heat generated by the MTJ body from escaping the MTJ body using at least one other thermal resistor configured to retain heat generated by current passing through the MTJ body.

[0081] Example 32: A magnetic tunnel junction (MTJ) device, including: an MTJ body including a free region, a reference region, and an oxide region between the free region and the reference region; at least one electrode including conductive material configured to conduct electrical current at least one of to or from the MTJ body; and at least one electrically conductive thermal resistor between the MTJ body and the at least one electrode.
Example 33: The MTJ device of Example 32, wherein the at least one electrically conductive thermal resistor includes a plurality of interfaces between different conductive materials.

Example 34: The MTJ device of Example 33, wherein the plurality of interfaces between the different conductive materials include interfaces between at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO).

Example 35: The MTJ device according to any one of Examples 32-34, wherein the at least one electrically conductive thermal resistor includes a plurality of electrically conductive thermal resistors.

Example 36: A method of assembling a computing device, the method including: providing a memory device configured to electrically store data, the memory device including: at least one magnetic tunnel junction (MTJ) device including: a pair of electrodes; an MTJ body including an oxide region between a reference region and a free region, the MTJ body between the pair of electrodes; and at least one thermal resistor including at least one electrically conductive region between the MTJ body and at least one of the pair of electrodes.

Example 37: The method of Example 36, further including adding at least one device selected from the group consisting of: a processor mounted to a substrate, a graphics processing unit, an antenna within the computing device, a display on the computing device, a battery within the computing device, a power amplifier within the processor, and a voltage regulator within the processor.

Example 38: The method according to any one of Examples 36 and 37, wherein providing a memory device including at least one thermal resistor includes providing the memory device including at least one thermal resistor that is less than or equal to about 500 Angstroms thick.

Example 39: The method according to any one of Examples 36-38, wherein providing a memory device including at least one thermal resistor includes providing the memory device including at least one thermal resistor that is at least about 100 Angstroms thick.
Example 40: The method according to any one of Examples 36-39, wherein providing a memory device includes providing a spin-transfer torque (STT) random access memory device.

Example 41: A non-transitory computer-readable storage medium including computer-readable instructions stored thereon, the computer-readable instructions configured to instruct a processor to perform at least a portion of the method according to any one of Examples 12-15, 21-31, and 36-40.

Example 42: A means for performing the method according to any one of Examples 12-15, 21-31, and 36-40.

The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.
Claims

1. A magnetic tunnel junction (MTJ) device, comprising:

   an MTJ body, comprising:
   a free region including a ferromagnetic material;
   a reference region including a ferromagnetic material; and
   an oxide region including an oxide material between the free region and the reference region;

   an electrode comprising electrically conductive material; and

   a thermal resistor operably coupled between the MTJ body and the electrode, the thermal resistor including at least one conductive region including an electrically conductive material.

2. The MTJ device of claim 1, wherein the at least one conductive region of the thermal resistor includes at least two conductive regions, each conductive region of the at least two conductive regions including a different one of at least two different electrically conductive materials.

3. The MTJ device of claim 2, wherein the at least two different electrically conductive materials include at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO).

4. The MTJ device of claim 1, further including a synthetic antiferromagnet (SAF) operably coupled between the reference region of the MTJ body and the thermal resistor.

5. The MTJ device of claim 1, further including a synthetic antiferromagnet (SAF) operably coupled between the thermal resistor and the electrode.

6. The MTJ device of claim 1, further including a cap region comprising an electrically conductive material operably coupled between the free region of the MTJ body and the thermal resistor.

7. The MTJ device of claim 1, further including a cap region comprising an electrically conductive material operably coupled between the thermal resistor and the electrode.
8. The MTJ device according to any one of claims 1-7, further comprising:
   another electrode comprising electrically conductive material and located opposite the electrode across the MTJ body; and
   another thermal resistor operably coupled between the MTJ body and the other electrode, the other thermal resistor including at least one other conductive region including an electrically conductive material.
9. The MTJ device according to any one of claims 1-7, wherein at least one of the free region and the reference region includes a metallic insert region between two CoFeB regions.
10. The MTJ device according to any one of claims 1-7, wherein the oxide region includes magnesium oxide (MgO).
11. The MTJ device according to any one of claims 1-7, further comprising at least one other thermal resistor configured to retain heat generated by current passing through the MTJ body.
12. A method of forming a magnetic tunnel junction (MTJ) device, the method comprising:
   forming an MTJ body including a free region, a reference region, and an oxide region between the free region and the reference region;
   forming at least one electrode including conductive material configured to conduct electrical current at least one of to or from the MTJ body; and
   forming at least one electrically conductive thermal resistor between the MTJ body and the at least one electrode.
13. The method of claim 12, wherein forming the at least one electrically conductive thermal resistor comprises forming a plurality of interfaces between different conductive materials.
14. The method of claim 13, wherein forming a plurality of interfaces between different conductive materials comprises forming the plurality of interfaces between at least two of carbon (C), tungsten (W), tungsten nitride (WN), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), indium gallium zinc oxide (IGZO), and indium tin oxide (ITO).
15. The method of claim 12, wherein forming at least one electrically conductive thermal resistor comprises forming a plurality of electrically conductive thermal resistors.

16. A computing device, comprising:
   a memory device configured to electrically store data, the memory device including:
   at least one magnetic tunnel junction (MTJ) device including:
   a pair of electrodes;
   an MTJ body including an oxide region between a reference region and a free region, the MTJ body between the pair of electrodes; and
   at least one thermal resistor comprising at least one electrically conductive region between the MTJ body and at least one of the pair of electrodes.

17. The computing device of claim 16, further comprising at least one device selected from the group consisting of:
   a processor mounted to a substrate, a graphics processing unit, an antenna within the computing device, a display on the computing device, a battery within the computing device, a power amplifier within the processor, and a voltage regulator within the processor.

18. The computing device according to any one of claims 16 and 17, wherein the at least one thermal resistor is less than or equal to about 500 Angstroms thick.

19. The computing device according to any one of claims 16 and 17, wherein the at least one thermal resistor is at least about 100 Angstroms thick.

20. The computing device according to any one of claims 16 and 17, wherein the memory device comprises a spin-transfer torque (STT) random access memory device.
FIG. 1
FIG. 2
FIG. 3
FIG. 4
FIG. 7
A. CLASSIFICATION OF SUBJECT MATTER
H01L 43/02(2006.01)i, H01L 43/10(2006.01)i, H01L 43/12(2006.01)i, G11C H/16(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L 43/02; H01L 43/08; G11C 11/16; H01L 29/82; H01L 43/10; G11B 5/127; H01L 21/00; G11C 11/00; H01L 43/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: MTJ, free region, reference region, oxide region, electrode, thermal resistor, ferromagnetic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>US 2015-0076485 A1 (MICRON TECHNOLOGY, INC.) 19 March 2015 See paragraphs [0012], [0019], [0021], [0026], [0047] - [0049], [0056], [0066], [0087]; and figures 1, 5.</td>
<td>1-20</td>
</tr>
<tr>
<td>Y</td>
<td>US 2010-0213558 A1 (JUN-SOO BAE et al.) 26 August 2010 See paragraphs [0038]- [0065]; and figure 2.</td>
<td>1-20</td>
</tr>
<tr>
<td>A</td>
<td>US 2005-0170533 A1 (HEON LEE et al.) 04 August 2005 See paragraphs [0034]- [0067]; and figures 4-10f.</td>
<td>1-20</td>
</tr>
<tr>
<td>A</td>
<td>US 2015-0214471 A1 (I I I HOLDINGS 3, LLC.) 30 July 2015 See paragraphs [0048]- [0095]; and figures 1-12B.</td>
<td>1-20</td>
</tr>
<tr>
<td>A</td>
<td>US 2009-0141543 A1 (CHIA-HUA HO et al.) 04 June 2009 See paragraphs [0029]- [0149]; and figures 1-1OD.</td>
<td>1-20</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C. See patent family annex.

Date of the actual completion of the international search 24 March 2017 (24.03.2017)
Date of mailing of the international search report 27 March 2017 (27.03.2017)

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongna-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Seong Woo
Telephone No. +82-42-481-3348

Form PCT/ISA/210 (second sheet) (January 2015)
<table>
<thead>
<tr>
<th>Patent document cited in search report</th>
<th>Publication date</th>
<th>Patent family member(s)</th>
<th>Publication date</th>
</tr>
</thead>
<tbody>
<tr>
<td>US 2015-0076485 Al</td>
<td>19/03/2015</td>
<td>CN 105531838 A</td>
<td>27/04/2016</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EP 3044816 Al</td>
<td>20/07/2016</td>
</tr>
<tr>
<td></td>
<td></td>
<td>KR 10-2016-0054538 A</td>
<td>16/05/2016</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TW 201530540 A</td>
<td>01/08/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>wo 2015-038378 Al</td>
<td>19/03/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 7732222 B2</td>
<td>08/06/2010</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 8035145 B2</td>
<td>11/10/2011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EP 2479787 A4</td>
<td>06/05/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 5578448 B2</td>
<td>27/08/2014</td>
</tr>
<tr>
<td></td>
<td></td>
<td>KR 10-2012-0083314 A</td>
<td>25/07/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2012-0230089 Al</td>
<td>13/09/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 8995179 B2</td>
<td>31/03/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>wo 2011-038373 Al</td>
<td>24/03/2011</td>
</tr>
<tr>
<td>US 2009-0141543 Al</td>
<td>04/06/2009</td>
<td>CN 101452990 A</td>
<td>10/06/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CN 101452990 B</td>
<td>20/08/2014</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TW 200926169 A</td>
<td>16/06/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TW 1361432 B</td>
<td>01/04/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 7688615 B2</td>
<td>30/03/2010</td>
</tr>
</tbody>
</table>