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(54) Title: METHOD FOR CONTROLLING SRAM DATA READ-WRITE, INTEGRATED CIRCUIT AND LIQUID CRYSTAL DISPLAY DEVICE WITH THE INTEGRATED CIRCUIT

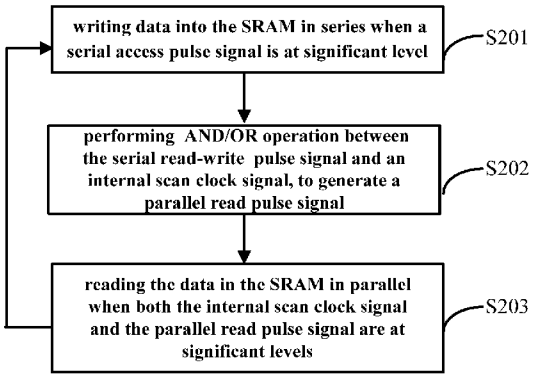

Fig.2

(57) Abstract: A method for controlling SRAM data read-write, an integrated circuit and a LCD device having the integrated circuit are provided. The method comprises the following steps: writing data into a SRAM in series when a serial read-write pulse signal is at valid level; performing AND operation or OR operation between the serial read-write pulse signal and an internal scan clock signal in the SRAM to generate a parallel read pulse signal, and setting the valid level of the parallel read pulse signal as reverse to the valid level of the serial read-write pulse signal; and reading out the data from the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at valid levels. By setting the valid level of the serial read-write pulse signal and the valid level of the parallel read pulse signal to occur in alternate, the method prevents time sequence conflict between serial read-write and parallel read, and thereby ensures correct data read-write.

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Method for Controlling SRAM Data Read-Write, Integrated Circuit and Liquid Crystal Display Device with the Integrated Circuit

Field of the Invention

The present invention pertains to semiconductor memory field, particularly relates to a method for controlling SRAM data read-write, an integrated circuit and a liquid crystal display device with the integrated circuit.

Background of the Invention

Today, in many middle-size or small-size liquid crystal display (LCD) devices, the driver chip has a built-in Static Random Read-write Memory (SRAM), which is configured to store various data and support 16-bit, 18-bit, or 24-bit serial data read-write and parallel read the stored data under control of row decoder, column decoder, write buffer and read/write circuit. Since the time sequence for serial read-write is provided by the read-write clock from an external Micro Control Unit (MCU), and the time sequence for parallel read is provided by the internal scan clock in the SRAM, there is possibility that serial read-write to a memory unit or byte in the SRAM is carried out while the sane memory unit or byte is read out in parallel. In usual, the read/write operation of SRAM is controlled with a read/write control bus, for example, for a 6-transistor (6T) SRAM, it is difficult to avoid the conflict between serial read-write and parallel read; especially, if serial write to a memory unit is carried out before the data is read from the memory unit in parallel, it is easy to result in data loss.

The solution for above problem in the prior art is to connect a First-In-First-Out (FIFO) circuit module between the SRAM and the MCU serially, such as the FIFO circuit module (hereinafter abbreviated as FIFO) shown in Fig.1. Actually, the so-called FIFO is a dual-port 8T SRAM. The fundamental principle of the solution shown in Fig.1 is: the external MCU writes the data serially to the FIFO through the DATA_BUS at its own serial writing clock rate (i.e., the external clock shown in Fig.1), and the SRAM reads the data sent by the MCU to the FIFO in parallel at its internal scan clock rate (i.e., the internal clock shown in Fig.1). Since a FIFO is used, the data written into the FIFO in the first will be read out by the SRAM in the first. If the FIFO is already full before the data in the FIFO is read out by the SRAM, FIFO will feed back a SRAM_BUSY signal to the MCU; then, the MCU will not further write data

into the FIFO, in order to avoid data loss.

Such a solution usually requires that the area of the FIFO must be very small, otherwise the data read-write rate will be limited. However, in a driver chip with a built-in SRAM in a LCD device, the area of the SRAM is usually accounts for 75% of the area of the entire driver chip; in addition, a 8T SRAM that serves as FIFO is much larger than a 6T SRAM; therefore, in terms of data read-write rate and FIFO area, the existing solution can't be used widely in small-size chips.

In general, the application of FIFO in the prior art causes larger driver chip area and therefore is adverse to large-scale application in chips. In addition, the cost and power consumption of such a driver chip are high.

Summary of the Invention

The object of the present invention is to provide a method for controlling SRAM data read-write, an integrated circuit and a LCD device with the integrated circuit, in order to eliminate the conflict of time sequence between serial read-write and parallel read and prevent large chip area caused by application of a FIFO circuit module.

The present invention provides a method for controlling SRAM data read-write, comprises following steps:

writing data into a SRAM in series when a serial read-write pulse signal is at valid level;

performing AND operation or OR operation between the serial read-write pulse signal and an internal scan clock signal in the SRAM to generate a parallel read pulse signal, and setting the valid level of the parallel read pulse signal as reverse to the valid level of the serial read-write pulse signal; and

reading out the data from the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at valid levels.

The present invention further provides an integrated circuit comprising a SRAM, wherein the integrated circuit further comprising:

a read-write control circuit, configured to receive a serial read-write pulse signal and an internal scan clock signal in the SRAM, perform AND operation or OR operation between the serial read-write pulse signal and the internal scan clock signal in the SRAM to generate a

parallel read pulse signal, and set the valid level of the parallel read pulse signal as reverse to the valid level of the serial read-write pulse signal, and trigger reading data from the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at valid levels.

The present invention yet provides a liquid crystal display (LCD) device, comprising a drive integrated circuit, wherein the drive integrated circuit is the integrated circuit provided in the present invention.

In the present invention, logical operation (AND operation or OR operation) between the serial read-write pulse signal from an external MCU and the internal scan clock signal in the SRAM is performed in an read-write control circuit, to obtain a parallel read pulse signal, which has the same waveform as the serial read-write pulse signal when the internal scan clock signal is at valid level; in that way, as long as the valid level of the parallel read pulse signal is set as reverse to the valid level of the serial read-write pulse signal, no time sequence conflict between serial read-write and parallel read will occur, and therefore the correctness of data read-write can be ensured.

Brief Description of the Drawings

Fig.1 is a schematic diagram of a solution that controls serial read-write asynchronous to parallel read in the prior art;

Fig.2 is a flow diagram of the method for controlling SRAM data read-write provided in the present invention;

Fig.3A is a schematic diagram of processing the internal scan clock signal and the serial read-write pulse signal with an AND gate to generate the parallel read pulse signal;

Fig.3B is a schematic diagram of processing the internal scan clock signal and the serial read-write pulse signal with an OR gate to generate the parallel read pulse signal;

Fig.4A is a timing sequence diagram of the signals shown in Fig.3A;

Fig.4B is a timing sequence diagram of the signals shown in Fig.3B;

Fig.5 is a signal timing sequence diagram in a preferred embodiment of the present invention;

Fig.6 is a schematic diagram of connection between the integrated circuit provided in the present invention and external components; and

Fig.7 is a structural diagram of the SRAM applied in the present invention.

Detailed Description of the Embodiments

In order to make the object, the technical solution, and the advantages of the present invention understood better, hereafter the present invention will be further detailed in the embodiments, with reference to the accompanying drawings. It is understood that the embodiments described here are only provided to explain the present invention, and shall not be deemed as constituting any limitation to the present invention.

Fig.2 shows a flow diagram of the method for controlling SRAM data read-write provided in the present invention. The method will be detailed as follows:

In step S201, when a serial read-write pulse signal is at valid level, the data are written into the SRAM.

The valid level of the serial read-write pulse signal can be set as high level or low level as required, which is to say, in step S201, the serial data read/write is performed during the serial read-write pulse signal (read-write clock signal of MCU) is at high level or low level.

In step S202, AND operation or OR operation is performed between the serial read-write pulse signal and the internal scan clock signal in the SRAM to generate a parallel read pulse signal, and the valid level of the parallel read pulse signal is set as reverse to the valid level of the serial read-write pulse signal.

Wherein, the AND operation/OR operation is accomplished with the AND gate shown in Fig.3A or the OR gate shown in Fig.3B. The internal scan clock signal and the serial read-write pulse signal are inputted to the two input terminals of the AND gate/OR gate, and the parallel read pulse signal is outputted from the output terminals of the AND gate/OR gate. The parallel read pulse signals obtained through AND operation/OR operation are shown in Fig.4A and Fig.4B respectively; wherein, the parallel read pulse signal shown in Fig.4A is obtained through AND operation, while the parallel read pulse signal shown in Fig.4B is obtained through OR operation.

The valid level of the internal scan clock signal can be set as high level or low level as

required. It is seen from Fig.4A and Fig.4B, during AND operation, the parallel read pulse signal is synchronous to the serial read-write pulse signal when the internal scan clock signal is at high level; whereas, in OR operation, the parallel read pulse signal is synchronous to the serial read-write pulse signal when the internal scan clock signal is at low level. Therefore, the level of the internal scan clock signal shall be set as its valid level when the waveforms are synchronous, i.e., during AND operation, the valid level of the internal scan clock signal is high level; and during OR operation, the valid level of the internal scan clock signal is low level.

In addition, in order to avoid conflict with the time sequence of serial read-write, it is required to set parallel data read being performed when the serial read-write pulse signal is not at its valid level, i.e., the valid level of the parallel read pulse signal must be set as reverse to the valid level of the serial read-write pulse signal. For the setting, there are four cases, as shown in Table 1:

Table 1

Case	Valid Level of Serial Read-write Pulse Signal	Valid level of Internal Scan Clock Signal	Logical Operation	Valid Level of Parallel Read Pulse Signal
1	Low	Low	OR	High
2	Low	High	AND	High
3	High	Low	OR	Low
4	High	High	AND	Low

Case 1: serial data read-write is performed when the external serial read-write pulse signal is at low level, while parallel read is performed when the internal scan clock signal is at low level. In that case, OR operation can be performed between the serial read-write pulse signal and the internal scan clock signal in an read-write control circuit to generate a parallel read pulse signal; specifically, the two clock signals are inputted to the OR gate circuit shown in Fig.3B, and the output signal from the OR gate circuit is taken as the parallel read pulse signal. In that case, the valid level of the parallel read pulse signal is high level, as shown in Fig.4B, when the internal scan clock signal is at low level, the valid level of the serial read-write pulse signal and the valid level of the parallel read pulse signal occur in alternate; therefore, conflict between serial read-write and parallel read can be avoided.

Case 2: serial data read-write is performed when the external serial read-write pulse signal is at low level, while parallel read is performed when the internal scan clock signal is at high level. In that case, AND operation can be performed between the external read-write clock signal and the internal scan clock signal in an read-write control circuit to generate a parallel read pulse signal; specifically, the two clock signals are inputted to the AND gate circuit shown in Fig.3A, and the output signal from the AND gate circuit is taken as the parallel read pulse signal. In that case, the valid level of the parallel read pulse signal is high level, as shown in Fig.4A, when the internal scan clock signal is at high level, the valid level of the serial read-write pulse signal and the valid level of the parallel read pulse signal occur in alternate; therefore, conflict between serial read-write and parallel read can be avoided.

Case 3: This case is essentially similar to Case 1, with the difference as: the valid levels of serial read-write pulse signal and parallel read pulse signal are reverse to those in Case 1; however, they also occur in alternate; therefore, this case will not be described any more.

Case 4: This case is essentially similar to Case 2, with the difference as: the valid levels of serial read-write pulse signal and parallel read pulse signal are reverse to those in Case 2; however, they also occur in alternate; therefore, this case will not be described any more.

In any of the above four cases, the read-write control circuit (such as the AND gate circuit and the OR gate circuit) can be arranged in a same integrated circuit as the SRAM. The integrated circuit can be used as a drive integrated circuit of a LCD device, and work with a MCU and some peripheral devices to constitute a driver module of the LCD, which controls serial data read-write from/to the SRAM and parallel data read from the SRAM, without the conflict of time sequence.

In step S203, when the parallel read pulse signal is at valid level, the data in the SRAM is read out in parallel. Since the serial read-write pulse signal is not at valid level when the parallel read pulse signal is at valid level, the case of synchronous serial read-write and parallel read will not occur.

In any of the four cases described in step S202, reading data in parallel is performed when the parallel read pulse signal is at valid level in step S203; then, step S201 is repeated to further perform serial data read-write, and then parallel data read will be performed again.

However, the serial read-write pulse signal is provided from an external MCU and the speed is very high, but the speed of the internal scan clock signal in SRAM is relatively low,

up to one third of the serial read-write speed at the most. Therefore, in a clock cycle of the internal scan clock, the valid level of the serial read-write pulse signal appears several times, as shown in Fig.4A and Fig.4B. However, since the SRAM scan address is constant in a same clock cycle of the internal scan clock, parallel data read for a same address will be performed in the same clock cycle; such repeated parallel read will cause severe waste in power consumption.

In order to reduce power consumption, the method provided in the present invention further comprises: reading twice consecutively for the same memory address during reading data from the SRAM in parallel. Fig.5 shows a timing sequence diagram in a preferred embodiment of the present invention, wherein, for example, in Case 1 described in step S202, the preferred embodiment employs a counter to count the pulse signals obtained by logical OR operation between the internal scan clock signal and the serial read-write pulse signal according to the clock signal of the counter, and count twice, i.e., count twice the high level of serial read-write pulse signal when the internal scan clock signal is at low level (valid level), so as to ensure correct data reading and reduce power consumption. The counter can be built in the drive integrated circuit of the LCD device. Wherein, the reason for counting twice is: in view that the serial read-write pulse signal and the internal scan clock signal are two irrelevant clock signals, it is difficult to ensure the counted first pulse is an entire high level pulse after logical OR operation, as shown in the timing sequence diagram in Fig.5; if the counter only counts once, it is difficult to ensure correct data reading; therefore, the counter must be configured to count twice the clock signal output from the OR gate circuit, to ensure the second high level signal counted by the counter is an entire pulse and ensure the data read out from the memory unit is correct after twice data reading operations.

Likewise, if the valid level of the serial read-write pulse signal and the valid level of the parallel read pulse signal are set as the valid level in Case 2, 3, or 4 described in step S202, the counter must be configured to count twice the pulse signal output from the logical gate circuit, respectively.

Fig.6 is a schematic diagram of the connection between the integrated circuit provided in the present invention and external components; for the convenience of description, only the parts related to the embodiment of the present invention are shown.

The integrated circuit provided in the present invention comprises a SRAM; wherein, the integrated circuit further comprises: a read-write control circuit, configured to receive a serial

read-write pulse signal and an internal scan clock signal in the SRAM, perform AND operation or OR operation between the serial read-write pulse signal and the internal scan clock signal in the SRAM to generate a parallel read pulse signal, set the valid level of the parallel read pulse signal as reverse to the valid level of the serial read-write pulse signal, and trigger reading data from the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at valid levels.

Wherein, as shown in Fig.6, an external MCU is directly connected to the SRAM, without the need for any FIFO circuit module in the prior art. The MCU performs serial data read-write through a DATA_BUS when the serial read-write clock signal is at valid level; the SRAM performs parallel data reading when both the internal scan clock signal and the parallel read pulse signal are at valid levels, and reads out the data into a data read-out latch.

The read-write control circuit mainly comprises a logical gate, which can be an AND gate circuit or an OR gate circuit with two input terminals and one output terminal, wherein, the two input terminals are configured to input the internal scan clock signal and the serial read-write pulse signal and the output terminal is configured to output the parallel read pulse signal. According to the Table 1 and the four cases described above, the AND gate circuit/OR gate circuit performs AND operation or OR operation between the internal scan clock signal and the serial read-write pulse signal to generate a parallel read pulse signal.

Corresponding to the preferred embodiment of the method described above, the read-write control circuit further comprises: a counter, configured to count the parallel read pulse signal, so as to control reading twice consecutively for the same address during parallel data reading. In this preferred embodiment, during the period the internal scan clock signal is at valid level, the non-valid level of the external serial read-write pulse signal is counted twice by the counter and taken as the parallel read pulse signal, so as to ensure correct parallel data read.

In another aspect of the present invention, a LCD device is provided, which comprises a drive integrated circuit, which can be the integrated circuit shown in Fig.6. Wherein, the SRAM can be built in the drive integrated circuit of the LCD device, while the MCU, driver chip, and some peripheral devices constitute the driver module of the LCD device. The MCU performs serial read-write to the data in the memory units of the SRAM when the serial read-write pulse is at valid level; the driver module of the LCD device reads the data stored in the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at valid levels, and display the data on the LCD screen. Wherein, the valid levels of the

serial read-write pulse signal, the internal scan clock signal, and the parallel read pulse signal are set as described above, and will not be detailed further here.

Fig.7 shows the structure of the SRAM applied in the present invention. The SRAM can comprise a plurality of memory units to constitute a matrix memory structure, as shown in Fig.7, wherein the box enclosed by dotted lines represents a memory unit, which is a 6T SRAM. Only one memory unit is shown in Fig.7, and if the SRAM comprises a plurality of memory units, the total storage capacity will be the product of the number of rows and the number of columns of the matrix. The so-called "parallel read" refers to read out a row of data selected in the word line; wherein, the pre-charge module is configured to pre-charge the bit lines on both ends to the same level; the sensitive comparator is configured to compare data according to the level difference between the bit lines during parallel data reading and store the data in a data read-out latch. The so-called "serial read-write" is to write the data items one by one serially through the data bus into the memory units selected by word line and bit line at the same time in the SRAM, or read the data items one by one from the memory units through the data bus and then send the data to the MCU, wherein, serial data reading also requires a sensitive comparator.

The integrated circuit provided in the present invention only comprises a simple logical gate circuit and a counter, except for a SRAM; therefore, the chip area is reduced greatly, and the cost and power consumption are reduced further.

While the present invention has been illustrated and described with reference to some preferred embodiments, the present invention is not limited to these. Those skilled in the art should recognize that various variations and modifications can be made without departing from the spirit and scope of the present invention as defined by the accompanying claims.

Claims

We claim:

1. A method for controlling SRAM data read-write comprises following steps:

writing data into a SRAM in series when a serial read-write pulse signal is at valid level;

performing AND operation or OR operation between the serial read-write pulse signal and an internal scan clock signal in the SRAM to generate a parallel read pulse signal, and setting the valid level of the parallel read pulse signal as reverse to the valid level of the serial read-write pulse signal; and

reading out the data from the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at valid levels.

2. The method according to claim 1, wherein the valid level of the internal scan clock signal is set according to whether the operation is AND operation or OR operation:

if AND operation is performed between the serial read-write pulse signal and the internal scan clock signal, setting high level as the valid level of the internal scan clock signal; and

if OR operation is performed between the serial read-write pulse signal and the internal scan clock signal, setting low level as the valid level of the internal scan clock signal.

3. The method according to claim 1 or 2, further comprises: reading twice consecutively for the same memory address during reading data from the SRAM in parallel.

4. An integrated circuit, comprises a SRAM, wherein the integrated circuit further comprises:

a read-write control circuit, configured to receive a serial read-write pulse signal and an internal scan clock signal in the SRAM, perform AND operation or OR operation between the serial read-write pulse signal and the internal scan clock signal in the SRAM to generate a parallel read pulse signal, and set the valid level of the parallel read pulse signal as reverse to the valid level of the serial read-write pulse signal, and trigger reading data from the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at valid

levels.

5. The integrated circuit according to claim 4, wherein the read-write control circuit comprises an AND gate circuit or an OR gate circuit with two input terminals and one output terminal, wherein the two input terminals are configured to input the internal scan clock signal and the serial read-write pulse signal, and the output terminal is configured to output the parallel read pulse signal.

6. The integrated circuit according to claim 5, wherein the valid level of the internal scan clock signal is set according to whether an AND gate circuit or an OR gate circuit is comprised by the read-write control circuit:

if the read-write control circuit comprises an AND gate circuit, the valid level of the internal scan clock signal is set as high level; and

if the read-write control circuit comprises an OR gate circuit, the valid level of the internal scan clock signal is set as low level.

7. The integrated circuit according to any one of claims 4-6, wherein the read-write control circuit further comprises:

a counter, configured to count the parallel read pulse signal, so as to control reading twice consecutively for the same address in parallel.

8. A liquid crystal display device, comprises a drive integrated circuit, wherein the drive integrated circuit is the integrated circuit described in any one of claims 4-7.

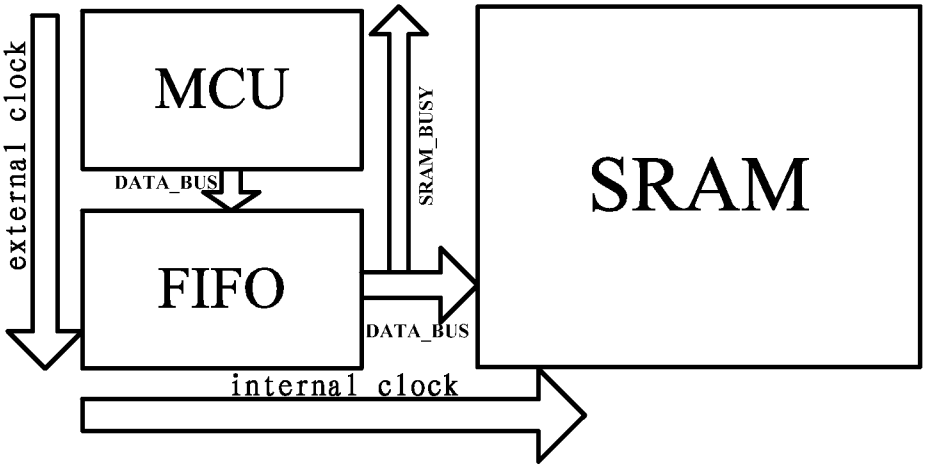
MCU
DATA_BUS
FIFO
external clock
SRAM_BUSY
SRAM
DATA_BUS
internal clock

Fig.1

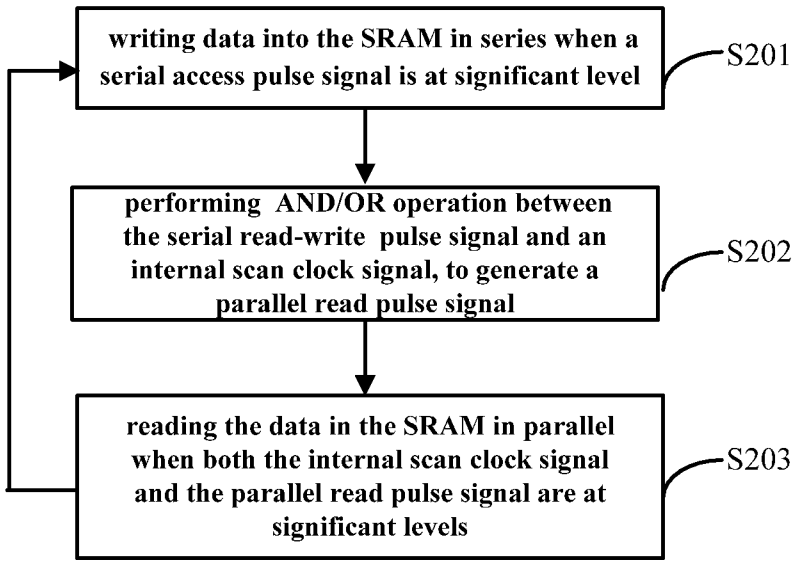
writing data into the SRAM in series when a serial access pulse signal is at significant level
S201
performing AND/OR operation between the serial read-write pulse signal and an internal scan clock signal, to generate a parallel read pulse signal
S202
reading the data in the SRAM in parallel when both the internal scan clock signal and the parallel read pulse signal are at significant levels
S203

Fig.2

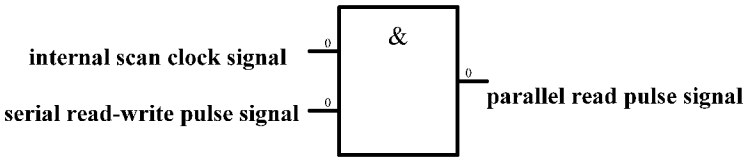
&
internal scan clock signal
serial read-write pulse signal
parallel read pulse signal

Fig.3A

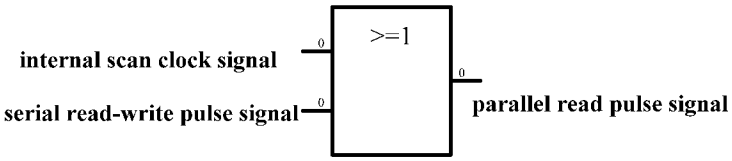
>=1
internal scan clock signal
serial read-write pulse signal
parallel read pulse signal

Fig.3B

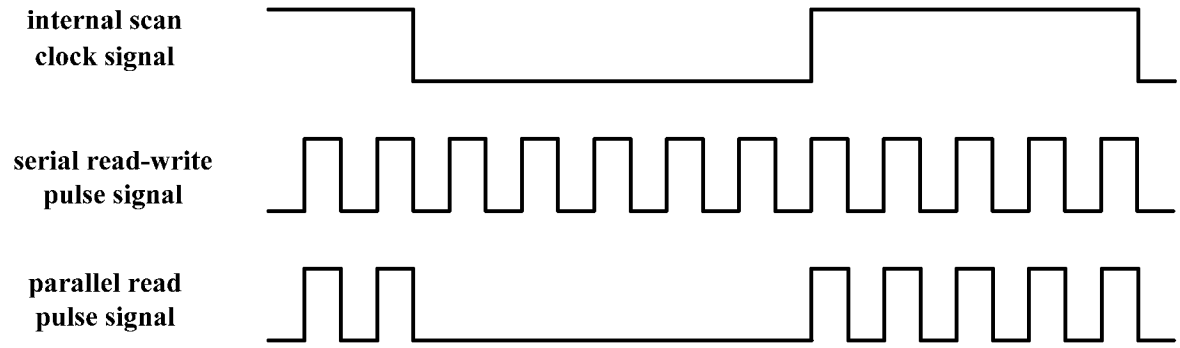
internal scan clock signal
serial read-write pulse signal
parallel read pulse signal

Fig.4A

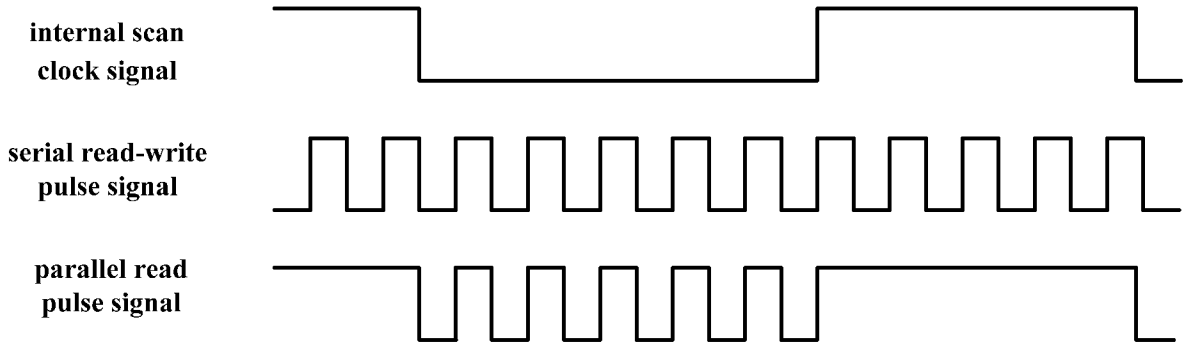
internal scan clock signal
serial read-write pulse signal
parallel read pulse signal

Fig.4B

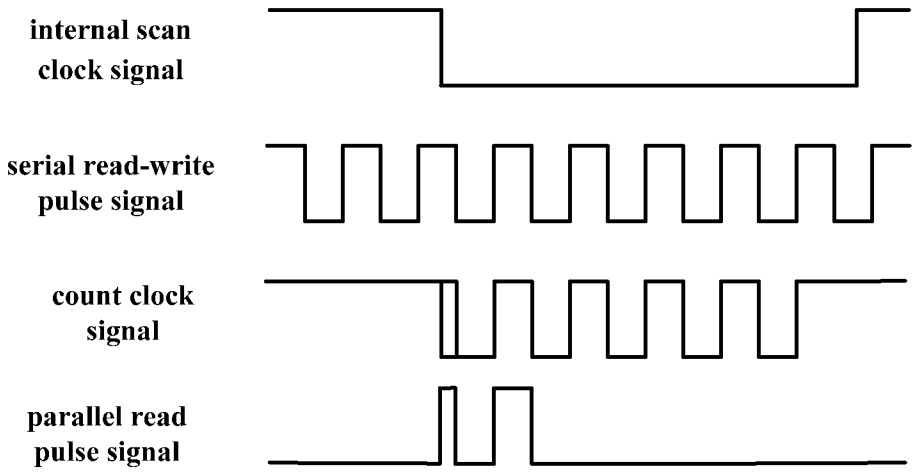
internal scan clock signal
serial read-write pulse signal
count clock signal
parallel read pulse signal

Fig.5

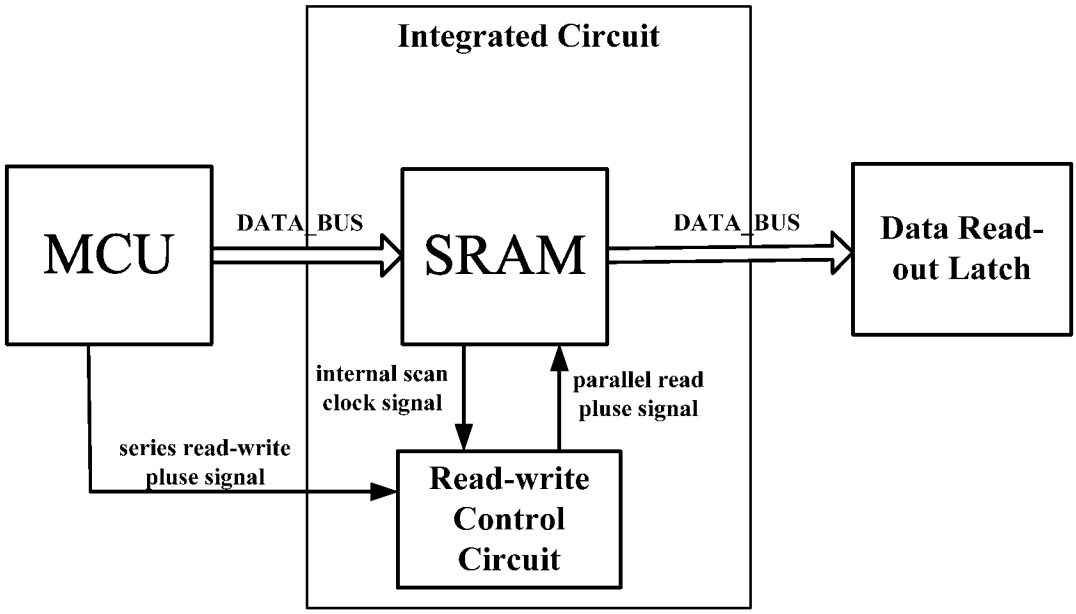
Integrated Circuit
MCU
DATA_BUS
SRAM
DATA_BUS
Data Read-out Latch
internal scan clock signal
parallel read pluse signal
series read-write pluse signal
Read-write Control Circuit

Fig.6

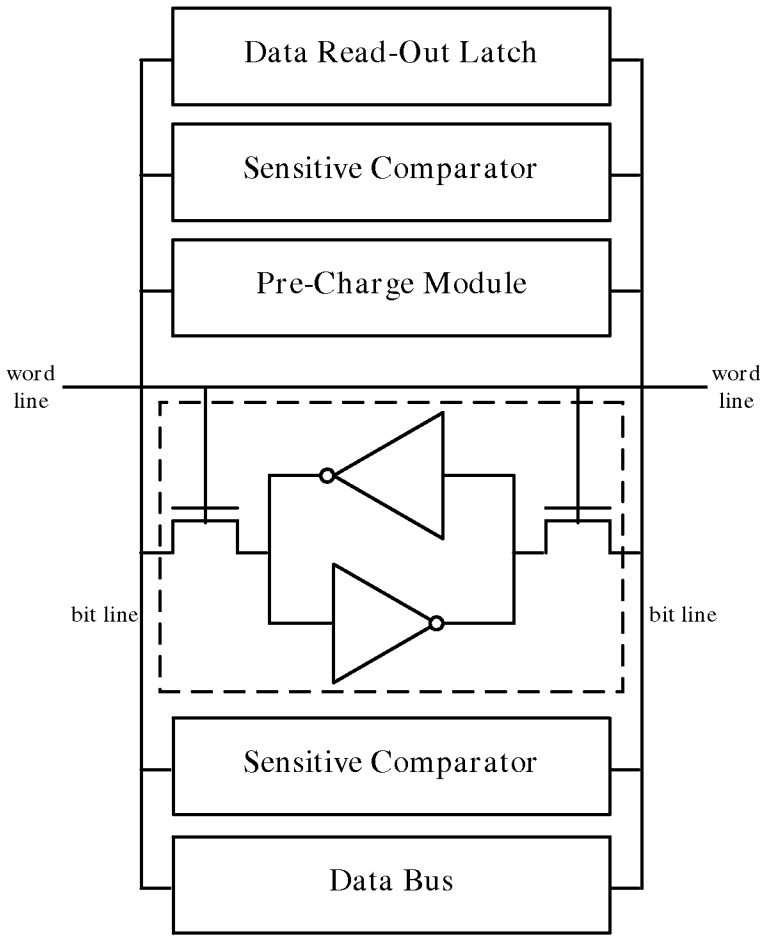
Data Read-Out Latch
Sensitive Comparator
Pre-Charge Module
word line
word line
bit line
bit line
Sensitive Comparator
Data Bus

Fig.7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2008/072208

A. CLASSIFICATION OF SUBJECT MATTER

see extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G11C 7/-;G11C 11/-;H01L 27/-;G02F 1/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC,WPI,PAJ,CNPAT,CNKI:

read+,writ+,pulse,signal,data,reverse,inversion,erroneous,error,collision,colliding,conflict+,avoidance,avoid,prevent+,control+,circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim
A	US 5,719,644A (Samsung Electronics Co.,Ltd(KR)) 17 Feb.1998(17.02.1998) the whole document, claims 1-19,figs.1-4	1-8
A	KR20070071158A (MAGNACHIP SEMICONDUCTOR LTD(KR)) 04 Jul.2007 (04.07.2007) the whole document	1-8
A	US 6,181,640B1(Hyundai Electronics Industries Co.,Ltd.(KR))30 Jan. 2001(30.01.2001) the whole document	1-8
A	US 2007/0195617A1(International Business Machines Corporation(US)) 23 Aug. 2007(23.08.2007) the whole document	1-8
A	JP2002-93173A(MITSUBISHI ELECTRIC CORP(JP))29 Mar. 2002(29.03.2002) the whole document	1-8
A	JP2002-25275A(TOKYO SHIBAURA ELECTRIC CO(JP)) 25 Jan. 2002(25.01.2002) the whole document	1-8

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 Nov. 2008(24.11.2008)	**11 Dec. 2008 (11.12.2008)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer YANG,Zifang Telephone No. (86-10)62411806

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2008/072208

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JP2002-25275A	25.01.2002	NONE	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2008/072208

CLASSIFICATION OF SUBJECT MATTER

G11C 7/00 (2006.01) i

G11C 11/34 (2006.01) i

H01L 27/00 (2006.01) n

G02F 1/13 (2006.01) n