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— *as to the identity of the inventor (Rule 4.17(i))*

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) Title: MEMRISTOR HAVING A TRIANGULAR SHAPED ELECTRODE

(57) Abstract: A memristor includes a first electrode having a triangular cross section, in which the first electrode has a tip and a base, a switching material positioned upon the first electrode, and a second electrode positioned upon the switching material. The tip of the first electrode faces the second electrode and an active region in the switching material is formed between the tip of the first electrode and the second electrode.

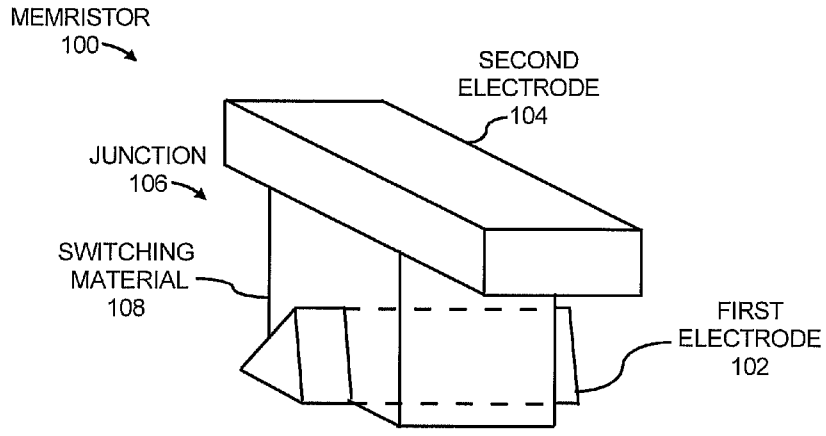


FIG. 1A

100 MEMRISTANCE
106 JONCTION
108 MATERIAU DE COMMUTATION
104 SECONDE ELECTRODE
102 PREMIERE ELECTRODE

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MEMRISTOR HAVING A TRIANGULAR SHAPED ELECTRODE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application has the same Assignee and shares some common subject matter with U.S. Patent Application Publication No. 20080090337 (Attorney Docket No. 200602631-1), filed on October 3, 2006, by R. Stanley Williams, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] Solid state memristive devices rely on the drift of mobile charge dopants upon the application of an electrical field, as discussed in the 20080090337 Patent Publication. These types of devices have been found to have promising properties in the fields of both digital and analog non-volatile electronic logic. To illustrate the potential of analog non-volatile electronic logic, synaptic computing has emerged as a potential technology that is enabled by the relatively small size, low cost, and low power consumption provided by solid state memristive devices.

[0003] Researchers have designed nano-scale reversible switches with an ON-to-OFF conductance ratio of 10^4. Crossbar circuitry is often constructed using these types of switches. A useful configuration of this crossbar circuitry is a latch, which is an important component for constructing logic circuits and communicating between logic and memory. Researchers have described logic families entirely constructed from crossbar arrays of switches, as well as hybrid structures using switches and transistors. The devices that are presently fabricated have room for improvement particularly in terms of cyclability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments are illustrated by way of example and not limited in the following figure(s), in which like numerals indicate like elements, in which:

[0005] FIG. 1A illustrates a perspective view of a memristor having a first electrode and a second electrode, according to an embodiment of the invention;

[0006] FIG. 1B illustrates a crossbar array employing a plurality of the memristors depicted in FIG. 1A, according to an embodiment of the invention;

[0007] FIG. 1C illustrates a perspective view of a memristor having a first electrode and a second electrode, according to another embodiment of the invention;

[0008] FIG. 1D illustrates a crossbar array employing a plurality of the memristors depicted in FIG. 1C, according to an embodiment of the invention;

[0009] FIG. 2A illustrates an enlarged, cross-sectional front view of the memristor depicted in FIG. 1C, according to an embodiment of the invention;

[0010] FIG. 2B illustrates a perspective view of a memristor having a plurality of first electrodes, according to an embodiment of the invention;

[0011] FIG. 3A illustrates a perspective view of a memristor, in which both the first electrode and the second electrode have triangular cross sections, according to an embodiment of the invention;

[0012] FIG. 3B illustrates a memristor in which the second electrode also includes a triangular cross section and is positioned in a substantially aligned arrangement with the first electrode, according to an embodiment of the invention; and

[0013] FIG. 3C illustrates a cross-sectional side view of a plurality of memristors, according to another embodiment.

DETAILED DESCRIPTION

[0014] For simplicity and illustrative purposes, the principles of the embodiments are described by referring mainly to examples thereof. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the embodiments. It will be apparent however, to one of ordinary skill in the art, that the embodiments may be practiced without limitation to these specific details. In other instances, well known methods and structures are not described in detail so as not to unnecessarily obscure the description of the embodiments.

[0015] Disclosed herein is a memristor having an electrode with a triangular cross section that improves the electrical field lines between electrodes and thus the performance of the memristor. More particularly, the triangular-shaped electrode of the memristor disclosed herein enables the drift of mobile charge dopants to be more focalized as compared with conventional memristive devices, which results in improved performance.

[0016] As used herein, the term "self-aligned" as applied to "junction" means that the junction that forms the switch and/or other electrical connection between two wires is created wherever two wires, either of which may be coated or functionalized, cross each other, because it is the act of crossing that creates the junction.

[0017] The term "self-assembled" as used herein refers to a system that naturally adopts some geometric pattern because of the identity of the components of the system; the system achieves at least a local minimum in its energy by adopting this configuration.

[0018] The term "singly configurable" means that a switch is able to change its state only once via an irreversible process such as an oxidation or reduction reaction; such a switch may be the basis of a programmable read only memory (PROM), for example.

[0019] The term "reconfigurable" means that a switch can change its state multiple times via a reversible process such as an oxidation or reduction;

in other words, the switch may be opened and closed multiple times such as the memory bits in a random access memory (RAM).

[0020] The term "configurable" means either "singly configurable" or "reconfigurable".

[0021] Micron-scale dimensions refer to dimensions that range from 1 micrometer to a few micrometers in size.

[0022] Sub-micron scale dimensions refer to dimensions that range from 0.1 nanometers to 50 nanometers (0.05 micrometers).

[0023] Micron-scale and submicron-scale wires refer to rod or ribbon-shaped conductors or semiconductors with widths or diameters having the dimensions of 0.04 to 10 micrometers, heights that can range from a few nanometers to a micrometer, and lengths of several micrometers and longer.

[0024] A memristor is a two-terminal dynamical electrical device that acts as a passive current limiter in which the instantaneous resistance state is a function of bias history. One embodiment of a memristor is a two-terminal device in which the electrical flux, or time intergral of the electric field, between the terminals is a function only of the amount of electric charge, or time intergral of the current, that has passed through the device.

[0025] A crossbar is an array of switches, here memristors, that can connect each wire in one set of parallel wires to every member of a second set of parallel wires that intersects the first set (usually the two sets of wires are perpendicular to each other, but this is not a necessary condition).

[0026] As used herein, the functional dimension of the device is measured in nanometers (typically less than 50 nm), but the lateral dimensions may be nanometers, sub-microns or microns.

[0027] The term "triangular" refers to shapes that are triangular and to shapes that are not perfectly triangular and thus may include any suitable shapes that have a base portion that is substantially larger than a tip portion, such shapes being considered as being substantially triangular. In this regard,

shapes that do not come to a point at their tips but whose tips are significantly smaller than the bases of the shapes are considered to be triangular.

[0028] With reference first to FIG. 1A, there is shown a perspective view of a memristor 100, according to an embodiment. It should be understood that the memristor 100 depicted in FIG. 1A may include additional components and that some of the components described herein may be removed and/or modified without departing from a scope of the memristor 100. It should also be understood that the components depicted in FIG. 1A are not drawn to scale and thus, the components may have different relative sizes with respect to each other than as shown therein.

[0029] As depicted in FIG. 1A, the memristor 100 includes a first electrode 102 connected to a second electrode 104. In addition, the first electrode 102 is in a crossed arrangement with the second electrode 104. One or both of the first electrode 102 and the second electrode 104 may be formed of metal or semiconductor materials. By way of particular example, both of the first electrode 102 and the second electrode 104 are formed of platinum.

[0030] A switch junction 106 is depicted as connecting the first electrode 102 to the second electrode 104. The switch junction 106 is composed of a switching material 108, which may be formed of a metal oxide, such as, TiO2. In one regard, the switching material 108 is configured to have a conductive channel formed into the material by a localized field-driven atomic modification. In another embodiment, the switching material 108 is formed of any suitable material that is formed of molecules having a switchable segment or moiety that is relatively energetically stable in two different states.

[0031] The first electrode 102 is also depicted as being positioned within the switching material 108. The first electrode 102 has a triangular cross section, with the base of the first electrode 108 situated away from the second electrode 104 and the top of the first electrode 102 facing toward the second electrode 104. Various aspects of the first electrode 102 will be discussed in greater detail herein below with respect to FIG. 2A.

[0032] With reference now to FIG. 1B, there is shown a crossbar array 120 employing a plurality of the memristors 100 shown in FIG. 1A, according to an embodiment. It should be understood that the crossbar array 120 depicted in FIG. 1B may include additional components and that some of the components described herein may be removed and/or modified without departing from a scope of the crossbar array 120.

[0033] As shown in FIG. 1B, a first layer 112 of approximately parallel first electrodes 102 is overlain by a second layer 114 of approximately parallel second electrodes 104. The second layer 114 is roughly perpendicular, in orientation, to the first electrodes 102 of the first layer 112, although the orientation angle between the layers may vary. The two layers 112, 114 form a lattice, or crossbar, with each second electrode 104 of the second layer 114 overlying all of the first electrodes 102 of the first layer 112 and coming into close contact with each first electrode 102 of the first layer 112 at respective junctions 106, which represent the closest contact between two of the first and second electrodes 102 and 104. The crossbar array 120 depicted in FIG. 1B may be fabricated from micron-, submicron or nanoscale-electrodes 102, 104, depending on the application.

[0034] Although the second electrodes 104 depicted in FIGS. 1A and 1B are shown with square or rectangular cross-sections, the second electrodes 104 may have circular, elliptical, or more complex cross-sections, such as, triangular cross-sections. The wires may also have many different widths or diameters and aspect ratios or eccentricities. The term "nanowire crossbar" may refer to crossbars having one or more layers of sub-microscale electrodes, microscale electrodes or electrodes with larger dimensions, in addition to nanowires.

[0035] An example of an alternate arrangement of the memristor 100' is depicted in FIGS. 1C and 1D. FIG. 1C contains many of the elements as those depicted in FIG. 1A and FIG. 1D contains many of the same elements as those depicted in FIG. 1B. As such, only those features that differ from FIGS. 1A and 1B, respectively, will be discussed with respect to FIGS. 1C and 1D. Similarly to FIGS. 1A and 1B, it should be understood that the memristor 100' depicted in

FIGS. 1C and 1D may include additional components and that some of the components described herein may be removed and/or modified without departing from a scope of the memristor 100'. It should also be understood that the components depicted in FIGS. 1C and 1D are not drawn to scale and thus, the components may have different relative sizes with respect to each other than as shown therein.

[0036] With reference first to FIG. 1C, there is shown a perspective view of a memristor 100', according to another embodiment. In addition to the elements depicted in the memristor 100 in FIG. 1B, the memristor 100' includes a third electrode 110. More particularly, the first electrode 102 is depicted in FIG. 1C as being positioned on top of the third electrode 110. In addition, the first electrode 102 is depicted as being oriented in the same direction as the second electrode 104. The orientation of the first electrode 102 may, however, be varied without departing from a scope of the memristor 100'.

[0037] In the memristor 100' depicted in FIG. 1C, the third electrode 110 may be connected to a voltage source and the first electrode 102 may be electrically connected to the third electrode 110 and may thus receive an electrical charge when the third electrode 110 receives an electrical charge. As such, the first electrode 102 may extend the same or nearly the same distance as the third electrode 110 (for instance, in configurations where the first electrode 102 is co-linear with the third electrode) or the first electrode 102 may extend for relatively short distances with respect to the third electrode 110.

[0038] Turning now to FIG. 1D, there is shown a crossbar array 120' employing a plurality of the memristors 100' shown in FIG. 1B, according to an embodiment. In contrast to the crossbar array 120 depicted in FIG. 1B, the first layer 112 of the crossbar array 120' depicted in FIG. 1D is depicted as including a plurality of approximately parallel third electrodes 110. Although not clearly shown, it should be understood that a plurality of the junctions 106 includes at least part of one or more first electrodes 102, as depicted in FIG. 1C.

[0039] The memristors 100 and 100' depicted in FIGS. 1B and 1D may be built at the micro- or nano-scale and used as a component in a wide variety

of electronic circuits. The memristors 100 and 100' may be used as the basis for memories, switches, and logic circuits and functions. When used as a basis for memories, the memristor 100 and 100' be used to store a bit of information, 1 or 0. When used as a switch, the memristors 100 and 100' may either be a closed or open switch in a cross-point memory. When used as a logic circuit, the memristors 100 and 100' may be employed as bits in a logic circuit that resembles a Field Programmable Gate Array, or as the basis for a wired-logic Programmable Logic Array. The memristors 100 and 100' disclosed herein are also configured to find uses in a wide variety of other applications.

[0040] With reference now to FIG. 2A there is shown an enlarged, cross-sectional front view of the memristor 100' depicted in FIG. 1C, according to an embodiment. Although particular reference is made to the memristor 100', the principles described below with respect to the memristor 100' and the first electrode 102 are equally applicable to the memristor 100 and the first electrode 102 depicted in FIG. 1A. In other words, the principles disclosed herein with respect to FIG. 2A may equally be applied to the memristor depicted in FIGS. 1A and 1B with the third electrode 110 removed.

[0041] As shown in FIG. 2A, an electric field 210 is created when a voltage is applied across the first electrode 102 and the second electrode 104. As discussed above with respect to FIG. 1C, the voltage may travel through the first electrode 102 from the third electrode 110. Field lines of the electric field 210 illustrate the intensity of the field between the first electrode 102 and the second electrode 104 when a voltage is applied across the electrodes. Initially the entire switching material 108 is nonconductive. As such, a forming process is required to form a conductive channel in the switching material 108 between the first electrode 102 and the second electrode 104. The forming process includes applying a sufficiently high (threshold) voltage across the first electrode 102 and the second electrode 104 for a sufficient length of time to cause the conductive channel in the switching material 108 to form. The threshold voltage and the length of time required for the forming process may depend upon the type of material used for the switching material 108, the first electrode 102 and the second electrode 104.

[0042] The conductive channel formed from the forming process is referred to herein as the active region 220 of the memristor 100'. In addition, the conductivity of the active region 220 may be modulated by applying different biases across the first electrode 102 and the second electrode 104. Thus, the memristor 100' is reconfigurable based upon the bias applied across the first electrode 102 and the second electrode 104. In other instances, the memristor 100' may include a switching material 108 that is singly configurable.

[0043] As shown in FIG. 2A, the triangular shape of the first electrode 102 localizes the formation of the conductive channel in the switching material 108 during the forming step. More particularly, the relatively sharper profile of the first electrode 102 as compared with the relatively flat profile of conventional electrodes creates a local field enhancement effect above the first electrode 102. As such, the electric field 210 at the tip of the first electrode 102 is much higher than if the same bias was applied across a flat shaped electrode. In addition to concentrating the electric field 210 during the electroforming step, the triangular shape of the first electrode 102 will also localize the electrochemical reaction that occurs between the first electrode 102 and the switching material 108 and will also localize the mechanical stress during deposition of the switching material 108, all of which may assist in localizing the electroforming of conductive channel in the switching material 108 at the desired location in the memristor 100'.

[0044] In a conventional memristor having a relatively flat profile, the conductive channel formed during a forming step may occur at any point along the junction of crossed electrodes. The location of an active region prior to the forming process in a conventional memristor is thus difficult to predict and thus the conventional memristors require that the memristors be spaced with a sufficient margin of error to prevent cross talk between the memristors. In the memristor 100', the conduction channel localization afforded by the triangular shape of the first electrode 102 improves the predictability of the spatial location of the active region 220. The memristors 100' disclosed herein are thus able to be spaced more closely together with reduced risk of cross talk as compared with the conventional memristors.

[0045] With reference now to FIG. 2B, there is shown a perspective view of a memristor 200 having a plurality of first electrodes 102, 102', according to an embodiment. It should be understood that the memristor 200 depicted in FIG. 2B may include additional components and that some of the components described herein may be removed and/or modified without departing from a scope of the memristor 200. For instance, the memristor 200 may include any number of first electrodes 102 positioned along the length of the third electrode 110. Alternatively, the third electrode 110 of the memristor 200 may be removed such that the first electrodes 102 form the first layer 112 of the crossbar array 120 depicted in FIG. 1B.

[0046] Although not shown in FIG. 2B, it should be noted that a second layer 114 of second electrodes 104 is positioned over the first electrodes 102 such that a different second electrode 104 is positioned over each of the first electrodes 102 and that the second electrodes 104 extend in a similar direction as the first electrodes 102. In the instance that the third electrode 110 is removed, such as in the case of FIGS. 1A and 1B, a second electrode 104 is positioned over both of the first electrodes 102 and extend substantially perpendicularly to the lateral direction of the first electrodes 102.

[0047] Generally speaking, the multiple first electrodes 102 have been depicted in FIG. 2B to more particularly denote various other aspects of the first electrodes 102. For instance, FIG. 2B shows that each of the first electrodes 102 has a length 222, a height 224, and a width 226. According to an embodiment, the heights 224 and the widths 226 of the first electrodes 102 is of the order of nanometers. In addition, the length 222 of the first electrode 102 is of the order of hundreds of nanometers to microns. According to an example, the first electrodes 102 are sized to have dimensions that are significantly larger than surface deformations on the second electrode 104 and the third electrode 110. In addition, a minimum lateral spacing 240 between the first electrodes 102 may be determined to be a minimum distance that substantially prevents crosstalk between the laterally spaced first electrodes 102. The minimum lateral spacing 240 may be substantially smaller, for instance, on the order of tens of nanometers to microns, than that allowed in memristors with conventional

electrodes because of the greater predictability of formation of the active region 204.

[0048] With reference now to FIG. 3A, there is shown a perspective view of a memristor 100", in which both the first electrode 102 and the second electrode 104 have triangular cross-sections, according to an embodiment. The memristor 100" includes all of the same elements as the memristor 100 depicted in FIG. 1A, with the only difference being the shape of the second electrode 104. In addition, as shown therein, the base of the second electrode 104 faces away from the first electrode 102 and the relatively sharp tip of the second electrode 104 faces toward the first electrode 102. In one regard, the electric field 210 forming the active region 220 between the first electrode 102 and the second electrode 104 may be further enhanced as compared with conventional memristor structures through the local field enhancement effect above the first electrode 102 and bellow the second electrode 104. In addition, the second electrode 104 having the triangular cross section has all of the same properties as those discussed above with respect to the first electrode 102.

[0049] Turning now to FIG. 3B, there is shown a memristor 300 in which the second electrode 104 also includes a triangular cross section and is positioned in a substantially aligned arrangement with the first electrode 102, according to an embodiment. It should be understood that the memristor 300 depicted in FIG. 3A may include additional components and that some of the components described herein may be removed and/or modified without departing from a scope of the memristor 300.

[0050] As shown in FIG. 3B, the second electrode 104 also has a triangular cross-sectional shape with the base of the second electrode 104 positioned on a fourth electrode 310 and the tip of the second electrode 104 facing the tip of the first electrode 102. In addition, the second electrode 104 extends in approximately the same direction as the first electrode 102. As such, one of the first electrode 102 and the second electrode 104 extends in the same direction as one of the third electrode 110 and the fourth electrode 310 and the

other of the first electrode 102 and the second electrode 104 extends perpendicularly to one of the third electrode 110 and the fourth electrode 310.

[0051] As an alternative to the configuration depicted in FIG. 3B, one of the third electrode 110 and the fourth electrode 310 and may be removed. In this configuration, the first electrode 102 or the second electrode 104 is configured to have voltage supplied directly therethrough.

[0052] FIG. 3C illustrates a cross-sectional side view of a plurality of memristors 300', according to a further embodiment. It should be understood that the memristors 300' depicted in FIG. 3C may include additional components and that some of the components described herein may be removed and/or modified without departing from a scope of the memristors 300'.

[0053] As shown therein, the memristors 300' are formed at junctions 106 between a first electrode 102 and a pair of fourth electrodes 310. As such, the view depicted in FIG. 3C is similar to a cross-sectional side view taken along multiple electrodes and junctions 106 in FIG. 1D, in which the fourth electrodes 310 form the second electrodes 104 depicted in FIG. 1D. In this regard, the second electrodes 104 may be positioned on alternating fourth electrodes 310 and the first electrode 102 may be positioned along the third electrode 110 to substantially be aligned with other alternating fourth electrodes 310.

[0054] It should be understood that the memristors depicted in the figures discussed above may be modified in various respects without departing from a scope of those disclosed memristors. By way of example, the switching material 108 may be composed of a dual layer structure as described in greater detail in the 20080090337 U.S. Patent Application Publication. As disclosed therein, the dual layer structure of the switching material enhances the switching properties and operation of devices using electrically actuated switches constructed therewith. That application for patent also describes a wide combination of materials than can be used to facilitate the switching process using the dual layer structure.

[0055] In one embodiment disclosed in that application for patent, the switching material comprises a thin titanium layer formed over a molecule

having a switchable segment or moiety that is relatively energetically stable in two different states. The switchable molecule and the thin titanium layer form the switch junction connecting the electrodes.

[0056] The memristors disclosed herein may be fabricated by modification of processes described in greater detail in that application for patent. For instance, the memristors may be manufactured through use of a wide range of material deposition and processing techniques. By way of particular example, the first electrode 102, and in certain instances, such as the configurations depicted in FIGS. 3A-3C, the second electrode 104, may be fabricated through use of fixed angle deposition of platinum or shadow mask evaporation. In addition, the third electrode 110 and the fourth electrode 310 may be fabricated using conventional techniques such as photolithography or electron beam lithography, or by more advanced techniques, such as imprint lithography.

[0057] Although a particular process for fabricating the memristors disclosed herein have been provided, it should be understood that other fabrication methods may also be used to fabricate the memristors.

[0058] What has been described and illustrated herein is an embodiment along with some of its variations. The terms, descriptions and figures used herein are set forth by way of illustration only and are not meant as limitations. Those skilled in the art will recognize that many variations are possible within the spirit and scope of the subject matter, which is intended to be defined by the following claims -- and their equivalents -- in which all terms are meant in their broadest reasonable sense unless otherwise indicated.

CLAIMS

What is claimed is:

1. A memristor comprising:

a first electrode having a triangular cross section, said first electrode having a tip and a base;

a switching material positioned upon said first electrode; and

a second electrode positioned upon said switching material, wherein the tip of the first electrode faces the second electrode, and wherein an active region in the switching material is formed adjacent to the tip of the first electrode.

2. The memristor of claim 1, further comprising:

a third electrode, wherein the base of the first electrode is in electrical contact with the third electrode.

3. The memristor of claim 1, wherein the second electrode comprises a triangular cross section having a tip and a base, and wherein the tip of the second electrode faces the tip of the first electrode.

4. The memristor of claim 1, wherein the second electrode comprises a triangular cross section having a tip and a base, said memristor further comprising:

a fourth electrode, wherein the base of the second electrode is in electrical contact with the fourth electrode.

5. The memristor of claim 4, wherein the second electrode is spaced from the first electrode such that switching material located adjacent to the tip of the second electrode forms a separate active region from the active region formed adjacent to the tip of the first electrode.

6. The memristor of claim 1, wherein the first electrode is elongated along at least one dimension.

7. The memristor of claim 1, wherein the first electrode comprises platinum and wherein the switching material comprises a metal oxide.

8. The memristor of claim 1, wherein the first electrode has a height, a width and a length, and wherein the height and the width are of the order of nanometers and wherein the length is of the order of hundreds of nanometers to microns.

9. A crossbar array composed of a plurality of memristors of claim 1, said crossbar array comprising:

a plurality of the first electrodes positioned approximately parallel with respect to each other, each of said plurality of first electrodes having the triangular cross section, with a tip and a base; and

a plurality of the second electrodes positioned approximately parallel with respect to each other and approximately perpendicularly with the plurality of first electrodes, wherein the tips of the plurality of first electrodes face respective ones of the plurality of first electrodes, wherein the switching material is positioned upon the plurality of first electrodes, and wherein active regions in the switching material are formed adjacent to the tips of the plurality of first electrodes.

10. The crossbar array of claim 9, further comprising:

a plurality of third electrodes, wherein the bases of the plurality of first electrodes are in electrical contact with respective ones of the plurality of third electrodes.

11. The crossbar array of claim 9, wherein the plurality of second electrodes comprise triangular cross sections, with respective tips and bases.

12. The crossbar array of claim 11, said crossbar array further comprising:

a plurality of fourth electrodes, wherein the bases of the plurality of second electrodes are in electrical contact with respective ones of the plurality of fourth electrodes.

13. The crossbar array of claim 12, wherein each of the plurality of second electrodes is spaced from a plurality of first electrodes such that switching material located adjacent to the tips of the plurality of second electrodes forms separate active regions from the active regions formed adjacent to the tips of the plurality of first electrodes.

14. The crossbar array of claim 9, wherein each of the plurality of first electrodes has a height, a width and a length, and wherein the height and the width are of the order of nanometers and wherein the length is of the order of hundreds of nanometers to microns.

15. A method for performing a forming process in order to initiate switching behavior in the memristor of claim 1, said method comprising:

impressing a threshold voltage through the tip of the first electrode, the switching material adjacent to the tip of the first electrode, and through the second electrode for a sufficient length of time to cause a predictable and discrete active region of high conductivity to form within the switching material adjacent to the tip of the first electrode.

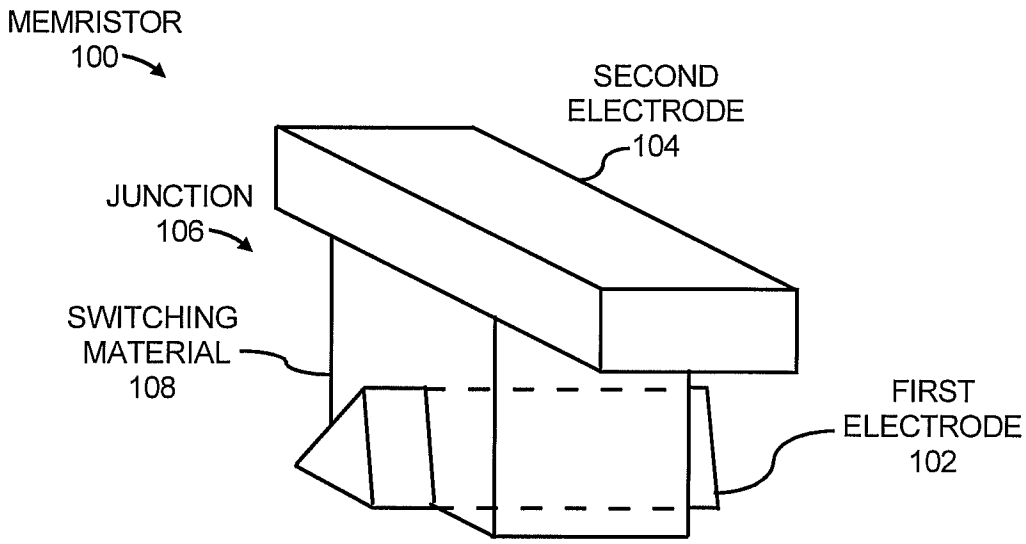

MEMRISTOR
100
SECOND
ELECTRODE
104
JUNCTION
106
SWITCHING
MATERIAL
108
FIRST
ELECTRODE
102

FIG. 1A

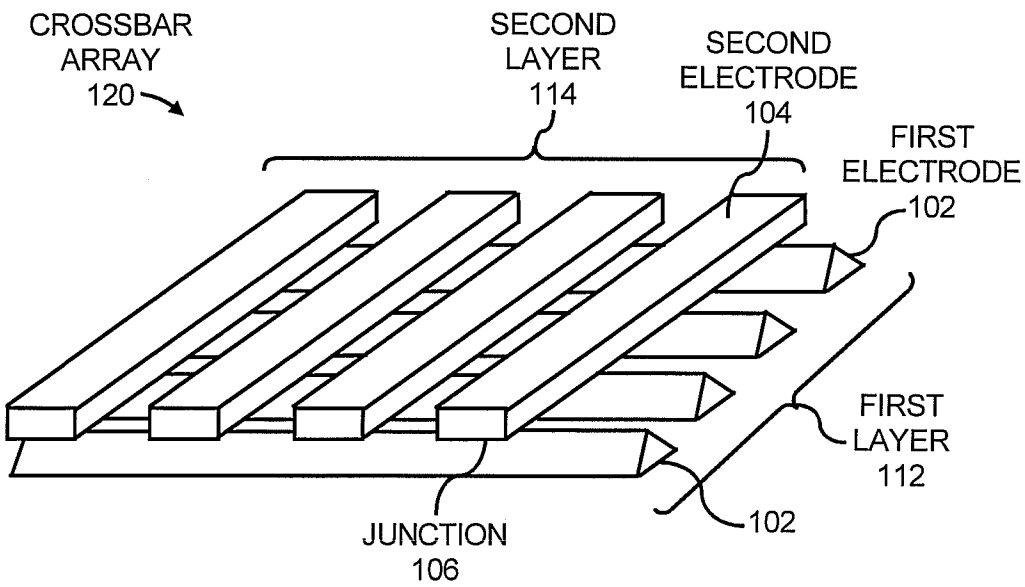

CROSSBAR
ARRAY
120
SECOND
LAYER
114
SECOND
ELECTRODE
104
FIRST
ELECTRODE
102
FIRST
LAYER
112
102
JUNCTION
106

FIG. 1B

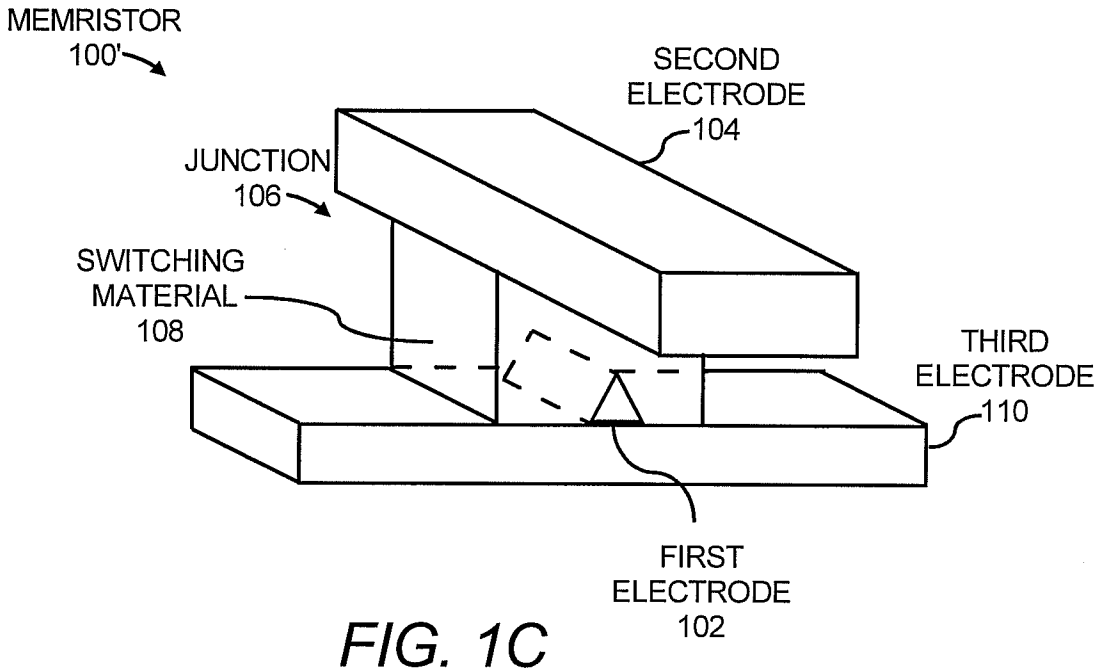

MEMRISTOR
100'
SECOND
ELECTRODE
104
JUNCTION
106
SWITCHING
MATERIAL
108
THIRD
ELECTRODE
110
FIRST
ELECTRODE
102

FIG. 1C

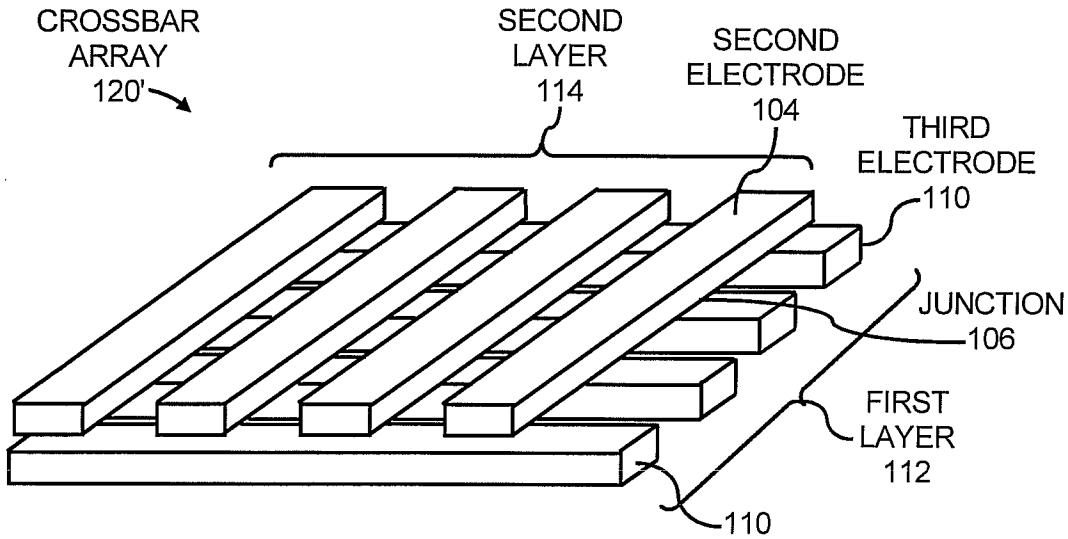

CROSSBAR
ARRAY
120'
SECOND
LAYER
114
SECOND
ELECTRODE
104
THIRD
ELECTRODE
110
JUNCTION
106
FIRST
LAYER
112
110

FIG. 1D

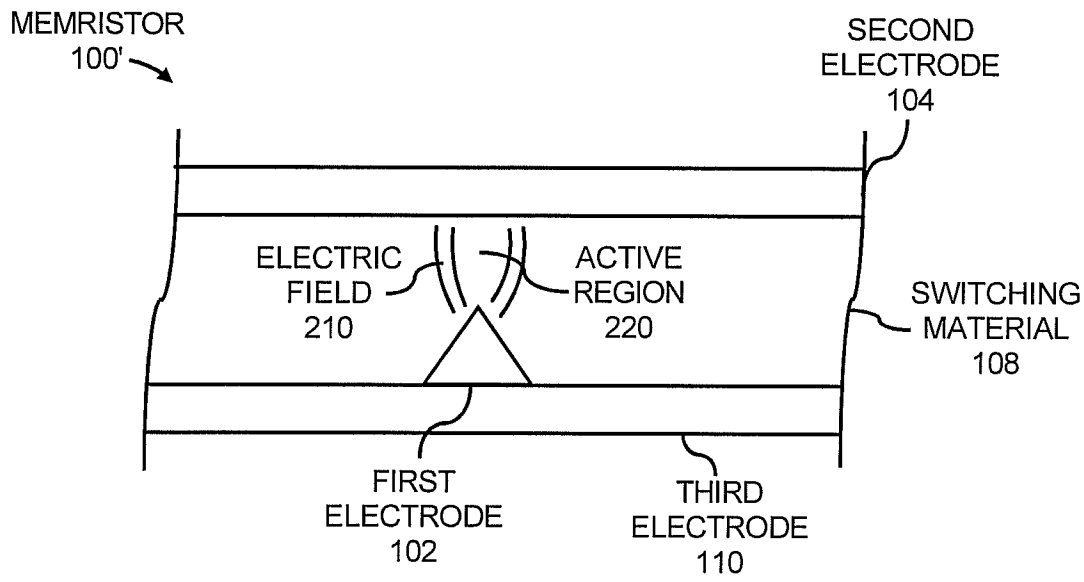

MEMRISTOR
100'
SECOND
ELECTRODE
104
ELECTRIC
FIELD
210
ACTIVE
REGION
220
SWITCHING
MATERIAL
108
FIRST
ELECTRODE
102
THIRD
ELECTRODE
110

FIG. 2A

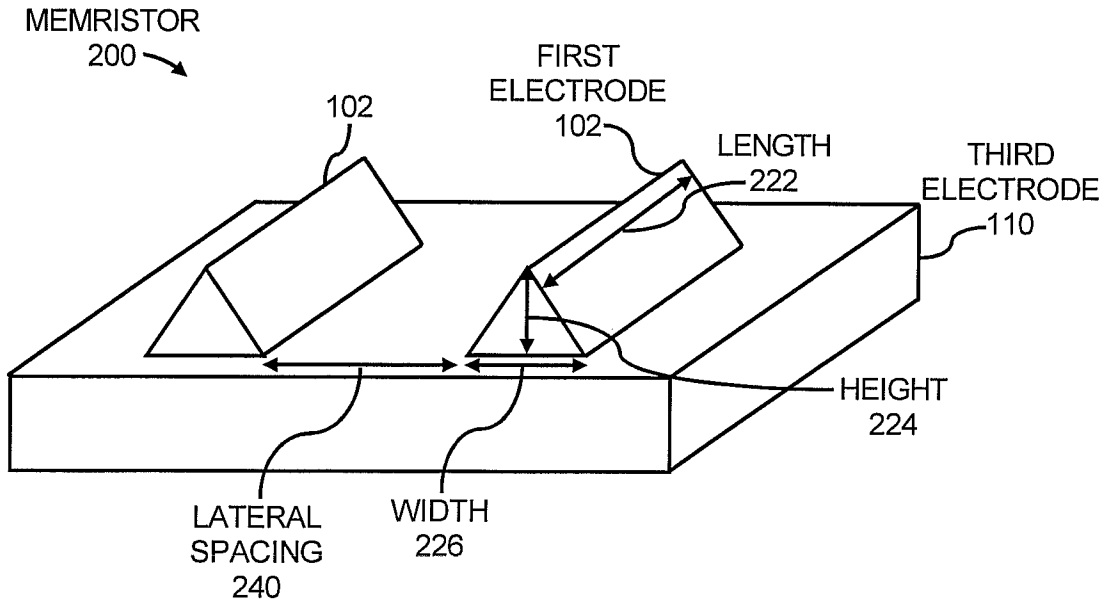

MEMRISTOR
200
102
FIRST
ELECTRODE
102
LENGTH
222
THIRD
ELECTRODE
110
HEIGHT
224
LATERAL
SPACING
240
WIDTH
226

FIG. 2B

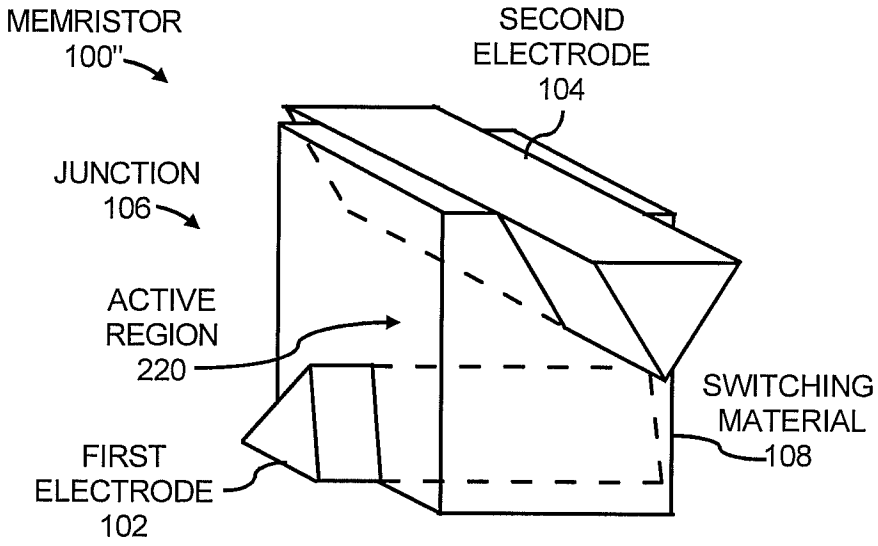

MEMRISTOR
100"
SECOND
ELECTRODE
104
JUNCTION
106
ACTIVE
REGION
220
SWITCHING
MATERIAL
108
FIRST
ELECTRODE
102

FIG. 3A

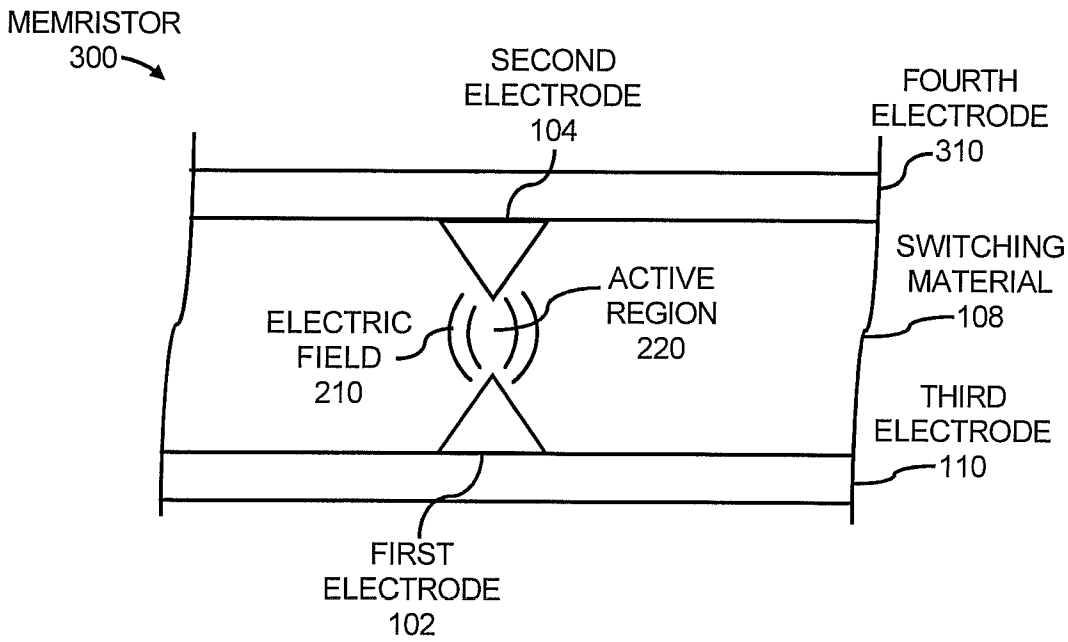

MEMRISTOR
300
SECOND
ELECTRODE
104
FOURTH
ELECTRODE
310
SWITCHING
MATERIAL
108
ACTIVE
REGION
220
ELECTRIC
FIELD
210
THIRD
ELECTRODE
110
FIRST
ELECTRODE
102

FIG. 3B

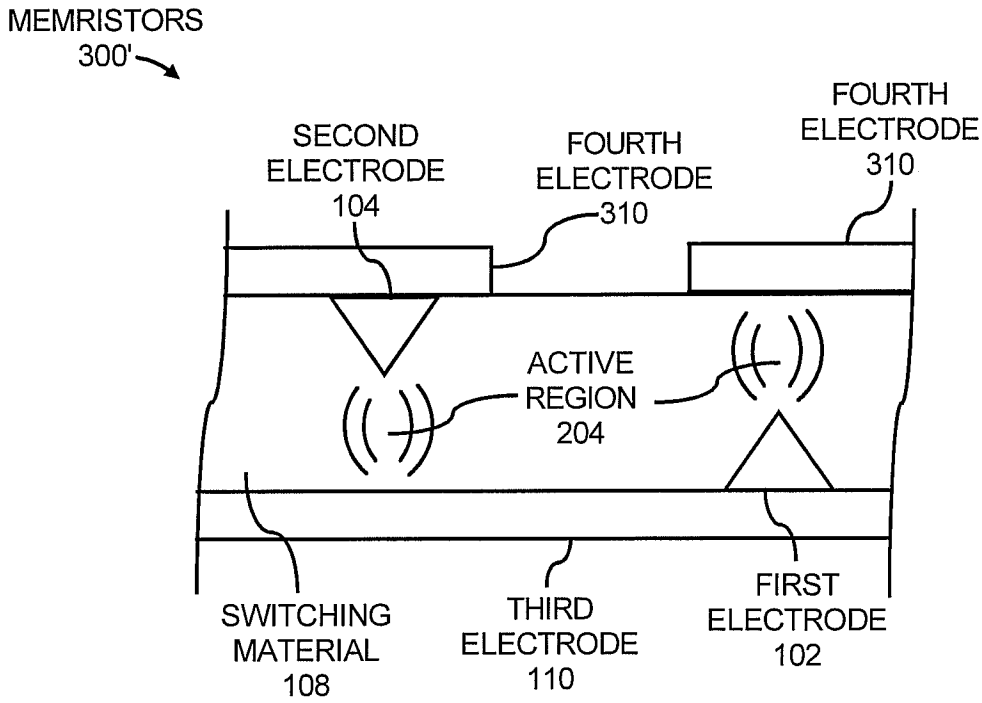

MEMRISTORS
300'
SECOND
ELECTRODE
104
FOURTH
ELECTRODE
310
FOURTH
ELECTRODE
310
ACTIVE
REGION
204
SWITCHING
MATERIAL
108
THIRD
ELECTRODE
110
FIRST
ELECTRODE
102

FIG. 3C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/030827

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2006.01)i, H01L 21/8247(2006.01)i, H01L 29/06(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC H01L 21/82, H01L 21/332, H01L 47/00, H01L 29/04, B32B 27/00, H01L 21/304, H01L 21/56, H01L 23/12, H01L 23/29

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: triangular, electrode, memristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2008/0206931 A1 (BREUIL, L. et al.) 28 August 2008 See abstract, paras.[0038]-[0039], [0041], and [0047], fig.3A and 4A	1-5, 9-13, 15 6-8, 14
A	US 2008/0090337 A1 (WILLIAMS, R. S.) 17 April 2008 See abstract, claim 1	1-15
A	US 6670628 B2 (LEE, H. et al.) 30 December 2003 See abstract, fig.5A, col.5 lines 35-50, claim 1	1-15
A	US 7374174 B2 (LIU, J. et al.) 20 May 2008 See abstract, fig.2, col.3 lines 52-67, col.4 lines 1-8, claim 1	1-15
A	JP 2005-28734 A (NITTO DENKO CORP.) 03 February 2005 See abstract, claim 1	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 AUGUST 2009 (26.08.2009)	**26 AUGUST 2009 (26.08.2009)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
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Facsimile No. 82-42-472-7140

Authorized officer

Park Ji Eun

Telephone No. 82-42-481-8537

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2009/030827

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