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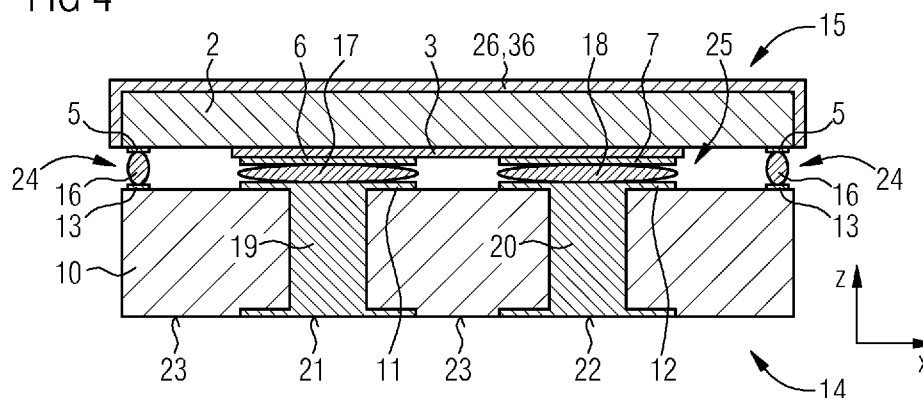
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(54) Title: LIGHT EMITTING ELEMENT WITH AN OPTOELECTRONIC SEMICONDUCTOR CHIP

FIG 4



(57) Abstract: A light emitting element with an optoelectronic semiconductor chip is provided, wherein the semiconductor chip has a substrate and a semiconductor structure, wherein the semiconductor structure is arranged with a mounting surface on a mounting surface of the substrate, wherein the semiconductor structure has a smaller mounting surface than the substrate, wherein a border area of the mounting face of the substrate circumvents the semiconductor structure, wherein the semiconductor structure is embodied to generate electromagnetic radiation, wherein on an upper side of the semiconductor structure electrical contacts are arranged, wherein the substrate is transparent for the radiation of the semiconductor structure, wherein the upper side of the semiconductor structure is arranged on a mounting side of a carrier, wherein the carrier comprises further electrical contacts on the mounting side, wherein the contacts of the semiconductor structure and the contacts of the carrier are connected, wherein between the mounting side of the carrier and the border area of the substrate a sealing member is arranged, wherein the sealing member seals a sealing area between the substrate and the carrier, wherein the semiconductor structure is arranged in the sealing area.



LIGHT EMITTING ELEMENT WITH AN OPTOELECTRONIC SEMICONDUCTOR CHIP

DESCRIPTION

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The invention refers to a light emitting element with an optoelectronic semiconductor chip and a method for producing a light emitting element with an optoelectronic semiconductor chip.

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In the state of the art it is known to provide a light emitting element with an optoelectronic semiconductor chip, wherein the semiconductor chip is arranged on a carrier. The semiconductor chip is covered by a plastic plate, a sapphire plate or a glass plate, wherein the epitaxial layer of the semiconductor chip is protected against environmental influences. Especially for semiconductor chips that emit ultraviolet radiation, a glass or a sapphire plate is used to protect the epitaxial layer since plastic could not withstand the ultraviolet radiation.

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The object of the invention is to provide an improved light emitting element with an optoelectronic semiconductor chip and to provide an improved method to produce a light emitting element with an optoelectronic semiconductor chip.

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The objects of the invention are solved by the independent claims.

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Further embodiments of the invention are disclosed in the dependent claims.

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A basic advantage is to provide a light emitting element with a simple structure that provides a protection of the epitaxial layer of the semiconductor structure with simple means.

A light emitting element with an optoelectronic semiconductor chip is provided. The semiconductor chip has a substrate and

a semiconductor structure. The semiconductor structure is arranged with a mounting surface on a mounting surface of the substrate. The semiconductor structure has a smaller mounting surface than the substrate. A border area of the mounting
5 face of the substrate circumvents the semiconductor structure. The semiconductor structure is embodied to generate electromagnetic radiation. On an upper side of the semiconductor structure electrical contacts are arranged. The substrate is transparent for the radiation of the semiconductor
10 structure. An upper side of the semiconductor structure is arranged on a mounting side of a carrier. The carrier comprises further electrical contacts on the mounting side, wherein the contacts of the semiconductor structure and the contacts of the carrier are connected. Between the mounting
15 side of the carrier and the border area of the substrate a sealing member is arranged. The sealing member seals a sealing area between the substrate and the carrier, wherein the semiconductor structure is arranged in the sealing area. Therefore the semiconductor structure is protected against
20 environment. For example, the sealing member is dust-tight and/or fluid-tight and/or gas-tight. In an embodiment, the sealing area is hermetically closed. The electromagnetic radiation may comprise visible light, infrared light or ultraviolet light. Furthermore, the further contact elements may
25 be guided through the carrier to a second contact side.

In a further embodiment, the sealing member comprises a ring, wherein the ring surrounds the semiconductor structure, wherein the ring is connected with the substrate and with the
30 carrier. The ring is a simple and reliably geometry for providing a sealing member. Furthermore the ring geometry can easily be formed.

In a further embodiment, the ring comprises metal. Metal provides suitable properties to form a robust sealing member.
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In a further embodiment, the ring comprises a first metal layer that is arranged on the substrate, wherein the ring

comprises a second metal layer that is arranged on the carrier, wherein the first and the second metal layer are connected. This embodiment can easily be produced and provides a reliable sealing member.

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In a further embodiment, between the first and second metal layer a third metal layer is arranged, wherein the third metal layer is connected with the first and the second metal layer. This embodiment provides a long time hermetic sealing member. In a further embodiment, the third metal layer is solder. This simplifies the process and provides a sufficient hermetic seal.

In a further embodiment, the sealing member comprises a sealing layer that fills up the sealing area. The sealing layer is a further appropriate sealing member that provides a sufficient sealing and a simple process. The sealing layer can be applied with a sealing ring. This increases the sealing stability and robustness.

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In a further embodiment, the sealing layer is made of silicone. Silicone can easily processed and provides sufficient sealing properties.

25 In a further embodiment, the substrate is at least partially covered with a protective layer. This improves a long time stability of the substrate.

In a further embodiment, the substrate comprises at least partially an anti-reflective coating. This improves the emitting of the radiation.

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In a further embodiment, the substrate comprises at least a self-cleaning coating. This feature maintains a long time clean surface of the substrate. Therefore, the emitting of the radiation is not blocked or reduced by a dirt layer.

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In a further embodiment, the self-cleaning coating is embodied to be activated by radiation of the semiconductor chip, especially by an ultraviolet light. This feature improves a simple structure and an efficient cleaning.

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In a further embodiment, the carrier comprises electronic circuit for controlling the semiconductor chip. This feature assists a compact and small light emitting element. Furthermore wiring work is reduced.

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In a further embodiment, the carrier is made of thinned silicon. The thinned silicon provides a thin carrier with a sufficient mechanical stability. Therefore the light emitting element can be produced with a small height.

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In a further embodiment, the semiconductor chip is embodied to generate ultraviolet radiation. The proposed sealing is for this type of semiconductor chip advantageous because the proposed sealing is long time robust and provides an hermetic sealing.

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It is a method proposed for producing a light emitting element with an optoelectronic semiconductor chip. A semiconductor chip with a substrate and a semiconductor structure is provided. The upper side of the semiconductor structure is laid on a mounting side of a carrier, wherein the carrier comprises further electrical contacts on the mounting side, wherein the contacts of the semiconductor structure and the contacts of the carrier are connected. Between the mounting side of the carrier and the border area of the substrate a sealing member is formed. The sealing member seals a sealing area between the substrate and the carrier. The semiconductor structure is arranged in the sealing area.

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The above-described properties, features and advantages of this invention and the way in which they are achieved will become clearer and more clearly understood in association with the following description of the exemplary embodiments

which are explained in greater detail in association with the drawings. Here in schematic illustration in each case:

Fig. 1 shows a view on a semiconductor chip.

Fig. 2 shows a schematic side view of the semiconductor chip.

Fig. 3 shows a top view on a carrier.

Fig. 4 shows a cross-sectional view of a light emitting element with a semiconductor chip and a carrier.

Fig. 5 shows a cross-sectional view of a light emitting element with a sealing layer.

Fig. 6 shows a cross-sectional view of a light emitting element with a protective layer.

Fig. 7 shows a cross-sectional view of a light emitting element with a rough surface.

Fig. 8 shows a cross-sectional view of a further light emitting element.

Fig. 9 shows a cross-sectional view of a light emitting element with electronic circuit.

Fig. 1 shows a schematic view on a semiconductor chip 15 with a substrate 2 in a y-x-plane. On a mounting surface 1 of the substrate 2 a semiconductor structure 3 is arranged. The semiconductor structure 3 has a smaller size than the substrate 2. A circumferential border area 4 of the mounting face of the substrate 2 is free from the semiconductor structure 3. On the border area 4 a first metal layer 5 is arranged. The first metal layer 5 surrounds the semiconductor structure 3. The first metal layer 5 is arranged with a given distance to the semiconductor structure 3.

The semiconductor structure 3 comprises a first and a second electrical contact 6, 7 that is arranged on a mounting surface 8 of the semiconductor structure 3. The semiconductor structure 3 is embodied to generate electromagnetic radiation for example ultraviolet light, visible light or infrared light. Depending on the used embodiment, the semiconductor structure comprises layers of semiconductor material that form a p/n layer interface that is embodied to generate the electromagnetic radiation. For example the semiconductor structure 3 is embodied as a light emitting diode structure. The semiconductor structure 3 may comprise a material system with gallium nitride or indium gallium nitride.

In the shown embodiment, the mounting surface 1 on the substrate 2 has a rectangular shape. Furthermore the mounting surface 8 of the semiconductor structure 3 has also a rectangular shape. Depending on the used embodiment, the substrate 2 and/or the semiconductor structure 3 may have a different shape for example a quadratic or a circular shape. However the mounting surface 8 of the semiconductor structure 3 is smaller than the mounting surface 1 of the substrate 2. This is necessary to provide an area for the first metal layer 5 that surrounds the semiconductor structure 3 with a given distance to the semiconductor structure 3.

The substrate 2 is made of material that is transparent for the electromagnetic radiation that is generated by the semiconductor structure 3. For example the substrate 2 is made of sapphire, silicon carbide, aluminium nitride, gallium nitride. The first metal layer 5 is embodied with a shape of four connected straight stripes. Depending on the used embodiment, the first metal layer 5 may also be embodied with the shape of a circular ring that surrounds the semiconductor structure 3.

Fig. 2 shows a side view of the semiconductor chip 15 with the substrate 2 and the semiconductor structure 3 in a z-x-

plane. The z axis and the y axis and the x axis constitute a rectangular coordinate system.

A thickness of the substrate 2 along the z axis is much larger than a thickness of the semiconductor structure 3 along the z axis. Furthermore, the first metal layer 5 has a thickness that is along the z axis smaller than a width along the x axis. Furthermore, the first metal layer 5 may have a smaller thickness along the z-axis compared to the thickness of the semiconductor structure along the z-axis.

Fig. 3 shows a view on a mounting surface 9 of a carrier 10 in a y-x-plane. The carrier 10 comprises on the mounting surface 9 two further electrical contacts 11, 12. Furthermore, a second metal layer 13 is guided along a border area on the mounting surface 9 of the carrier 10 surrounding the two further electrical contacts. The second metal layer 13 surrounds the further first and second electrical contacts 11, 12. The second metal layer 13 may have the same shape as the first metal layer 5 of the substrate 2. The second metal layer 13 may be made of the same material as the first metal layer 5 of the substrate 2. Furthermore, the further first and second electrical contacts 11, 12 may have the same size area as the first and second electrical contacts 6, 7 of the semiconductor structure 3. The carrier 10 may be embodied as a ceramic plate or a printed circuit board or a semiconductor plate.

Fig. 4 shows a cross sectional view in a z-x-plane of a light emitting element 14 that comprises the semiconductor chip 15 of Fig. 1 that is mounted on the carrier 10 of Fig. 3. The first and the second metal layer 5, 13 are connected by a third metal layer 16. The third metal layer 16 may comprise solder material for example AuSn or SnAgCu. Furthermore, the first and the second metal layer 5, 13 may be made of solder material for example AuSn or SnAgCu. Furthermore, the electrical contacts 6, 7 are connected with the further first and second electrical contacts 11, 12 by contact layers 17, 18.

The first and second contact layers 17, 18 may comprise solder for example AuSn or may be made of AuSn.

5 The further first and second electrical contacts 11, 12 are guided by via contacts 19, 20 to bottom contacts 21, 22 that are arranged at a bottom side 23 of the carrier 10. The first metal layer 5, the third metal layer 16 and the second metal layer 13 constitute a sealing member 24 that seals a sealing area 25 between the substrate and the carrier. The semiconductor structure 3 is arranged in the sealing area 25. The sealing member 24 constitutes a sealing ring, wherein the sealing ring surrounds the semiconductor structure 3. The sealing ring 24 seals the sealing area 25 from the environment. Depending on the used embodiment, the sealing ring 24 is embodied to hermetically seal the sealing area 25 from the environment. Therefore, the semiconductor structure 3 that may comprise epitaxial deposited semiconductor layers is protected against the environment. The electromagnetic radiation that is generated by the semiconductor structure 3 is emitted through the substrate 2. The sealing ring 24 provides an hermetic seal of the sealing area 25.

25 Depending on the used embodiment, the third metal layer 16 is omitted and the first and the second metal layer 5, 13 are connected directly for example hermetically. The connection between the first and the second metal layer 5, 13 may be formed by a metal bonding process.

30 The light emitting element 14 provides a robust package with hermetic requirements for the semiconductor structure 3. Especially by using sapphire as a substrate 2, the light emitting element 14 is extremely robust against environment. A protective layer 26 may be arranged on the surface of the substrate 2, especially if aluminium nitride or gallium nitride is used as substrate 2. The protective layer 26 may for example be made of silicon oxide. Furthermore, the protective layer 26 may also be embodied as an anti-reflective layer 36. Furthermore, only the anti-reflective layer 36 may be ar-

ranged on the surface of the substrate. However, depending on the used embodiment, the protective layer 26 can be omitted.

Fig. 5 shows a cross sectional view in an z-x-plane of a further embodiment of a light emitting element 14 that basically has the same structure as the embodiment of Fig. 4 comprising a semiconductor chip 15 with a substrate 2 and a semiconductor structure 3 and a carrier 10 with further electrical contacts 11, 12, via contacts 19, 20 and bottom contacts 21, 22. In contrast to the embodiment of Fig. 4, a sealing layer 27 is arranged between the mounting surface 1 of the substrate 2 and the mounting surface of the carrier 10 in the sealing area 25. The sealing layer 27 seals the whole semiconductor structure 3. The semiconductor structure 3 is for example hermetically encapsulated in the sealing layer 27. The sealing layer 27 may be made of silicone, epoxy or polymer or a hybrid material comprising silicone and epoxy material.

Depending on the used embodiment, additionally to the sealing layer 27 also a sealing ring 24 may be arranged as shown in Fig. 4 surrounding the sealing layer 27. In this embodiment, there is a double protection for the semiconductor structure 3 with a sealing layer 27 and a sealing ring 24. However the sealing ring 24 can be omitted.

Fig. 6 shows a further embodiment of a light emitting element 14 that is embodied as explained with regard to Fig. 4. However, additional to the embodiment of Fig. 4, the light emitting element 14 the substrate 2 is covered by a self-cleaning coating 28. The self-cleaning coating 28 may cover a top face 33 and all side faces 34,35 of the substrate 2. The self-cleaning coating 28 may for example comprise or be made of nano-layers of titanium oxide TiO₂. The self-cleaning coating 28 may be embodied to be actuated by radiation of the semiconductor structure 3 for example by ultraviolet light that is emitted by the semiconductor structure 3. The self-cleaning coating 28 improves a robustness of the light emitting element 14, wherein an organic deposition could be de-

composed with ultraviolet radiation using a photocatalytic cleaning process. This light emitting element 14 could be a part of a sensor inside an exhaust pipe of a combustion engine as the organic decomposition on the substrate 2 caused by incomplete combustion could be reduced significantly.

For example the light emitting element 14 may be arranged in an exhaust pipe of a car. The self-cleaning coating 28 can also be applied at a light emitting element 14 as shown in Fig. 5 that has a sealing layer 27.

Fig. 7 shows a cross sectional view in a z-x-plane of a further embodiment of a light emitting element 14, wherein the top face 33 of the substrate 2 comprises a rough surface 29 with a rough structure that increases light extraction from the substrate 2. The rough surface 29 may be embodied by recesses or projections with a shape of a pyramid or an inverted pyramid. Also other shapes for the recesses or projections are possible. For example, the rough surface 29 may comprise cylinder holes or rectangular holes to increase the light extraction from the substrate 2. The rough surface 29 may comprise micro pits or nano pits or micro structures or nano structures to enhance the light extraction.

Fig. 8 shows a schematic cross-sectional view in an z-x-plane of a further embodiment of a light emitting element 14 that is embodied as explained with regard to fig. 4. However in this embodiment the carrier 10 is embodied as a thin carrier 10, that is for example made of silicon. Furthermore, this embodiment may be processed by using a wafer bonding technology. The carrier 10 is embodied as an interposer with a thickness below 1 mm for example.

Fig. 9 shows a further cross-sectional view of a light emitting element 14 in an z-x-plane, wherein the light emitting element 14 is embodied as explained with regard to Fig. 4. In contrast to the light emitting element of Fig. 4 the carrier 10 comprises an electronic circuit 30 for example controlling

circuits or current sources for the semiconductor chip 15. The electronic circuit is electrically connected with the first and second bottom electrical contacts 21, 22. The electronic circuit 30 may comprise driver circuits and/or electric interface circuits. Furthermore, at the bottom side 23 of the carrier 10 an electrical connector 31 is arranged for connecting a cable to the light emitting element 14.

The semiconductor structure 3 may comprise an epitaxial semiconductor layer structure. The proposed light emitting element 14 provides a low-loss package especially for ultraviolet light emitting semiconductor diodes. A small and thin package can be achieved. Furthermore, a robust package with hermetic requirements is provided. Additionally, anti-reflective coating may be arranged on external surfaces of the substrate 2. This improves an overall package performance.

The protective layer 26 and/or the sealing layer 27 and/or the self-cleaning coating 28 and/or the rough surface 29 may be combined in any shown embodiments of the light emitting element 14.

The invention has been illustrated and described in detail with the aid of the preferred exemplary embodiments. Nevertheless, the invention is not restricted to the examples disclosed. Rather, other variants may be derived therefrom by a person skilled in the art without departing from the protective scope of the invention.

REFERENCE SYMBOLS

	1	mounting surface substrate
	2	substrate
5	3	semiconductor structure
	4	border area
	5	first metal layer
	6	first electrical contact
	7	second electrical contact
10	8	mounting surface semiconductor structure
	9	mounting surface carrier
	10	carrier
	11	further first electrical contact
	12	further second electrical contact
15	13	second metal layer
	14	light emitting element
	15	semiconductor chip
	16	third metal layer
	17	first contact layer
20	18	second contact layer
	19	first via contact
	20	second via contact
	21	first bottom electrical contact
	22	second bottom electrical contact
25	23	bottom side
	24	sealing ring
	25	sealing area
	26	protective layer
	27	sealing layer
30	28	self-cleaning coating
	29	rough surface
	30	electronic circuit
	31	connector
	32	cable
35	33	top face
	34	first side face
	35	second side face
	36	anti-reflective layer

CLAIMS

1. Light emitting element (14) with an optoelectronic semiconductor chip (15), wherein the semiconductor chip (15)
5 has a substrate (2) and a semiconductor structure (3),
wherein the semiconductor structure (3) is arranged with a mounting surface on a mounting surface (19) of the substrate (2), wherein the semiconductor structure (3) has a smaller mounting surface (8) than the substrate (2),
10 wherein a border area (4) of the mounting face (1) of the substrate (2) circumvents the semiconductor structure (3), wherein the semiconductor structure (3) is embodied to generate electromagnetic radiation, wherein on an upper side of the semiconductor structure electrical contacts (6, 7) are arranged, wherein the substrate (2) is transparent for the radiation of the semiconductor structure (3), wherein the upper side of the semiconductor structure is arranged on a mounting side (9) of a carrier (10), wherein the carrier (10) comprises further electrical contacts (11, 12) on the mounting side (9), wherein
15 the contacts (6, 7) of the semiconductor structure (3) and the contacts (11, 12) of the carrier (10) are connected, wherein between the mounting side (9) of the carrier (10) and the border area of the substrate a sealing member (5, 13, 16, 24, 27) is arranged, wherein the sealing member (5, 13, 16, 24, 27) seals a sealing area (25) between the substrate (2) and the carrier (10), wherein the semiconductor structure (3) is arranged in the sealing area (25).
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2. Light emitting element of claim 1, wherein the sealing member comprises a ring (24), wherein the ring (24) surrounds the semiconductor structure (3), wherein the ring (24) is connected with the substrate (2) and with the
35 carrier (10).
3. Light emitting element of claim 1 or 2, wherein the ring (24) comprises metal.

4. Light emitting element of claim 3, wherein the ring (24) comprises a first metal layer (5) that is arranged on the substrate (2), wherein the ring (24) comprises a second
5 metal layer (13) that is arranged on the carrier (10), wherein the first and the second metal layer (5, 13) are connected.
5. Light emitting element of claim 4, wherein between the
10 first and second metal layer (5, 13) a third metal layer (16) is arranged, wherein the third metal layer (16) is connected with the first and the second metal layer (5, 13).
- 15 6. The light emitting element of claim 5, wherein the third metal layer (16) is solder.
7. The light emitting element of any one of the preceding claims, wherein the sealing member comprises a sealing
20 layer (27) that fills up the sealing area (25).
8. The light emitting element of claim 7, wherein the sealing layer (27) is made of silicone.
- 25 9. The light emitting element of any one of the preceding claims, wherein the substrate (2) is at least partially covered with a protective layer (28).
10. The light emitting element of any one of the preceding
30 claims, wherein the substrate (2) comprises at least partially an anti-reflective coating (28).
11. The light emitting element of any one of the preceding
35 claims, wherein the substrate (2) comprises at least a self-cleaning coating (28).
12. The light emitting element of claim 11, wherein the self-cleaning coating (28) is embodied to be activated by ra-

diation of the semiconductor chip (15), especially by ultraviolet light.

13.The light emitting element, wherein the carrier (10) comprises electronic circuit (30) for controlling the semiconductor chip (15).

14.The light emitting element of any one of the preceding claims, wherein the carrier (10) is made of thinned silicon.

15.The light emitting element of any one of the preceding claims, wherein the semiconductor chip (15) is embodied to generate ultraviolet radiation.

16.Method for producing a light emitting element with an optoelectronic semiconductor chip, wherein a semiconductor chip with a substrate and a semiconductor structure is provided, wherein the semiconductor structure is arranged with a mounting surface on a mounting surface of the substrate, wherein the semiconductor structure has a smaller mounting surface than the substrate, wherein a border area of the mounting face of the substrate that circumvents the semiconductor structure, wherein the semiconductor structure is embodied to generate electromagnetic radiation, wherein on an upper side of the semiconductor structure electrical contacts are arranged, wherein the substrate is transparent for the radiation of the semiconductor structure, wherein the upper side of the semiconductor structure is laid on a mounting side of a carrier, wherein the carrier comprises further electrical contacts on the mounting side, wherein the contacts of the semiconductor structure and the contacts of the carrier are connected, wherein between the mounting side of the carrier and the border area of the substrate a sealing member is formed, wherein the sealing member seals a sealing area between the substrate and the carrier,

wherein the semiconductor structure is arranged in the sealing area.

FIG 1

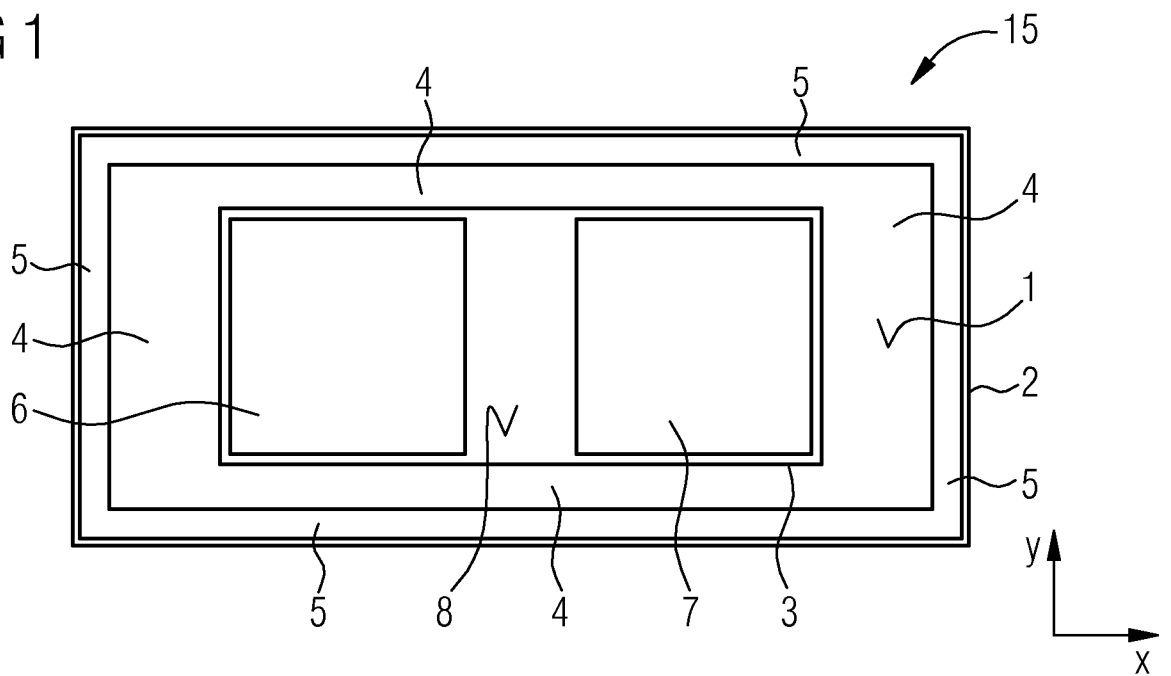


FIG 2

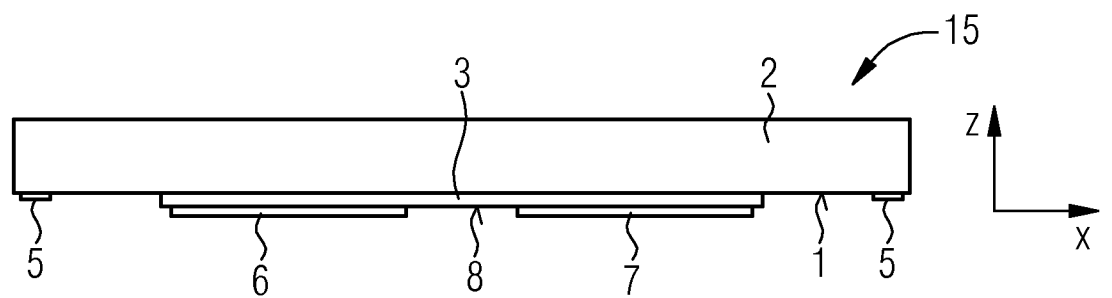


FIG 3

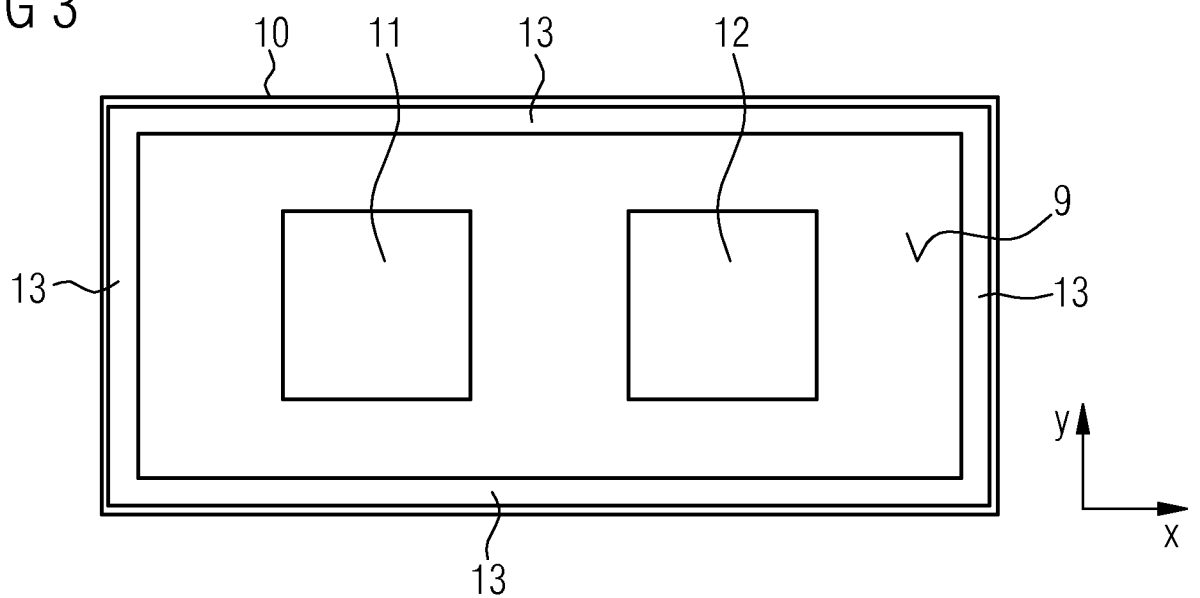


FIG 4

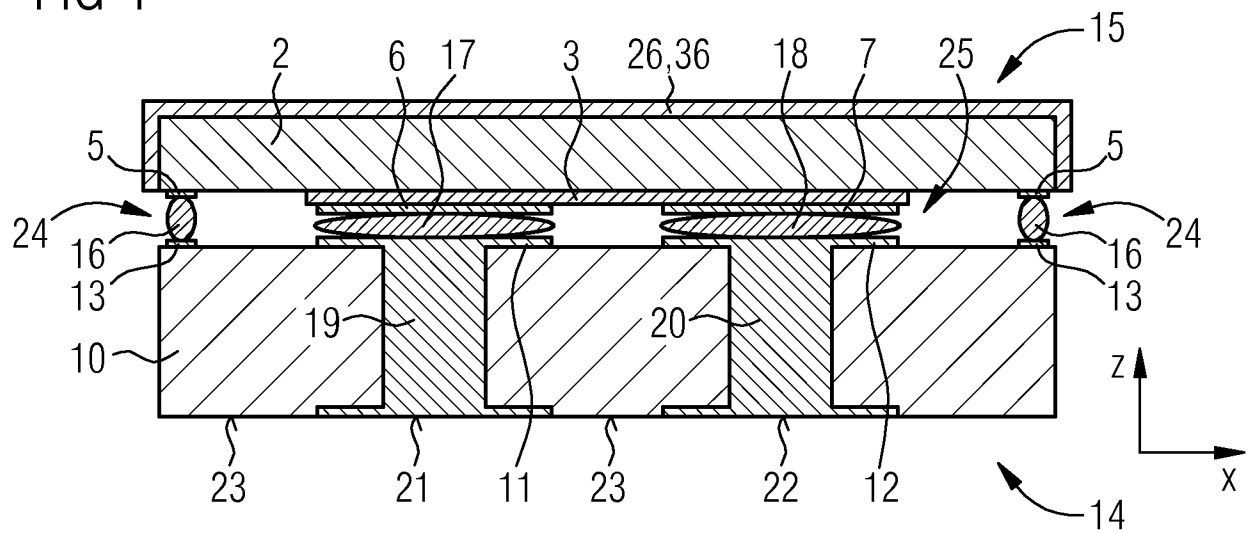


FIG 5

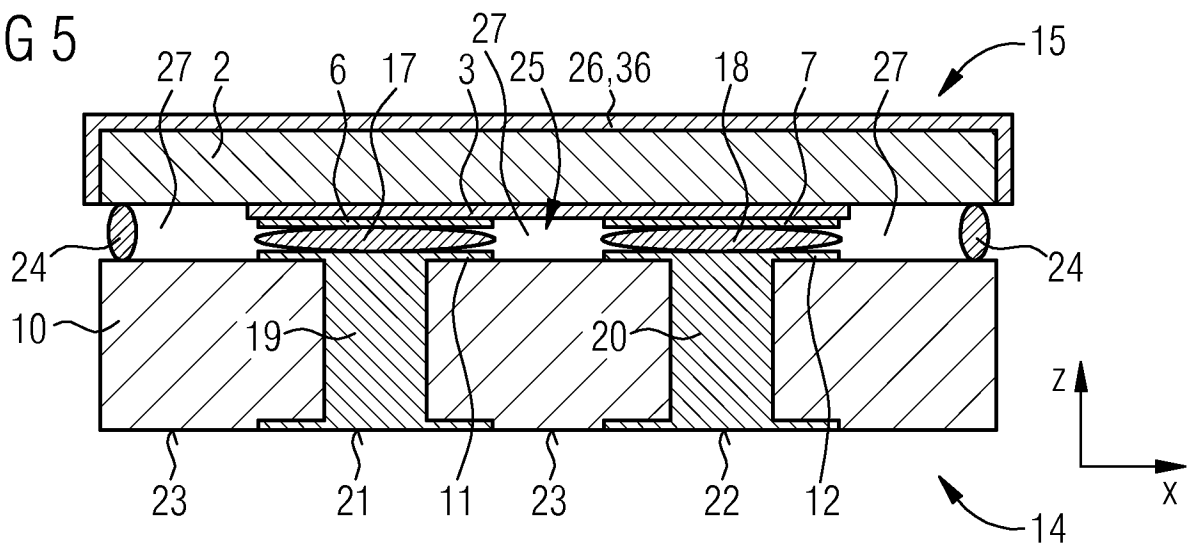


FIG 6

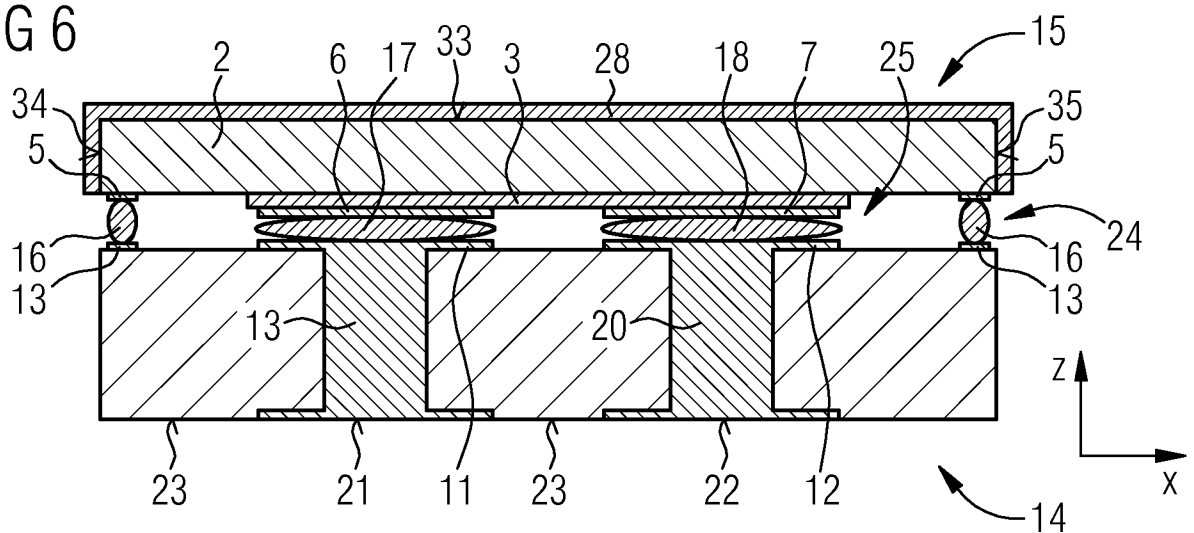


FIG 7

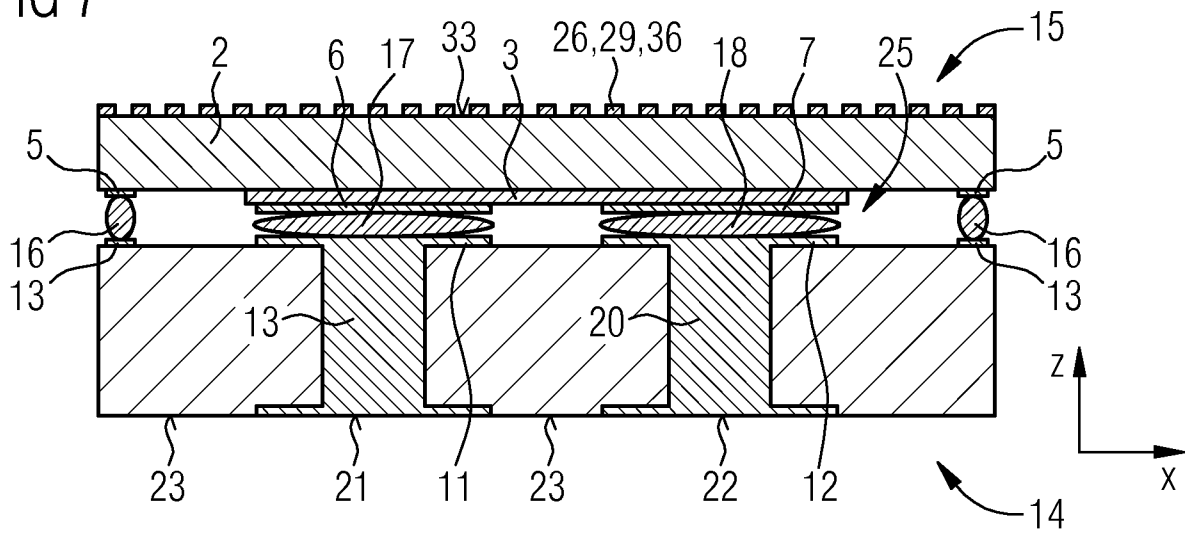


FIG 8

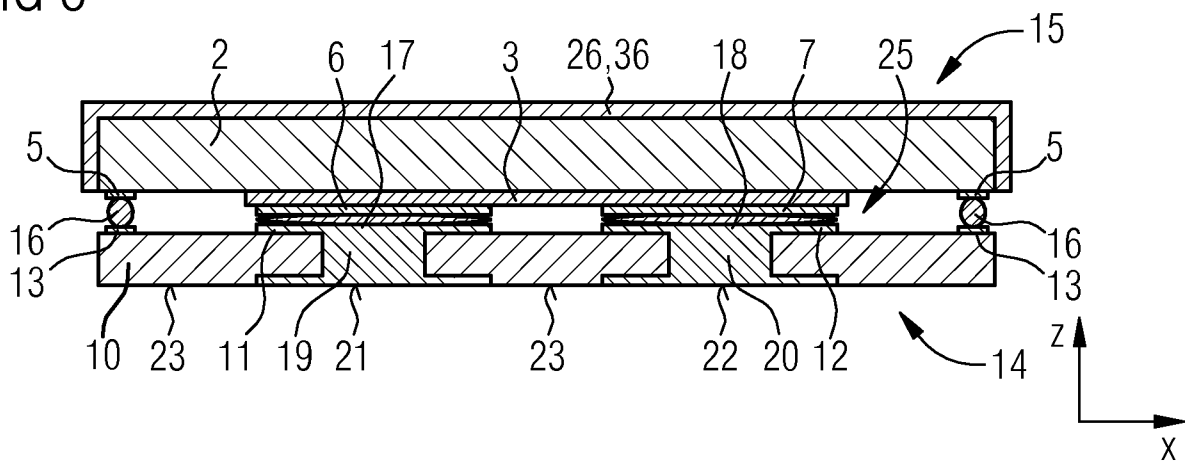
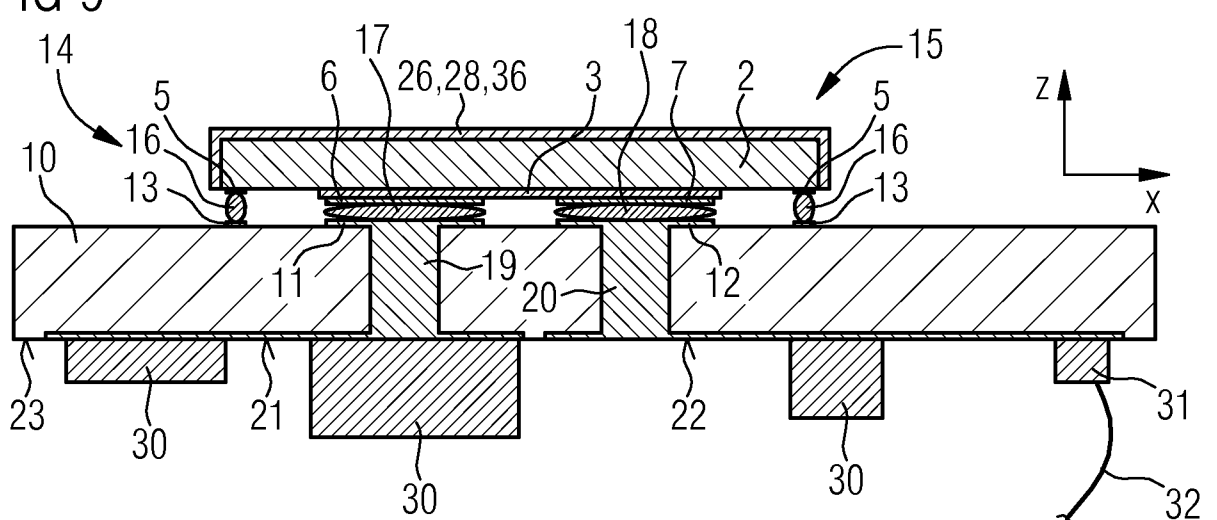


FIG 9



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/081927

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/52
ADD. H01L33/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/171277 A1 (SAITO SHINJI [JP]) 18 June 2015 (2015-06-18)	1-3,9, 10,13, 15,16 11,12
Y	abstract paragraphs [0069], [0071], [0073] - [0077]; figure 5 paragraph [0029] -----	
X	US 2012/241793 A1 (IN CHI HYUN [KR] ET AL) 27 September 2012 (2012-09-27) abstract paragraphs [0082] - [0087], [0098], [0104]; figure 6 ----- -/--	1,7,9, 10,13, 14,16



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

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Date of mailing of the international search report

18/07/2017

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/081927

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/026518 A1 (SUH DAE WOONG [KR] ET AL) 31 January 2013 (2013-01-31) abstract paragraph [0067]; figure 14 paragraph [0051] -----	1,7,8, 10,13,16
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