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(54) Title: PROBE ARRAY WAFER

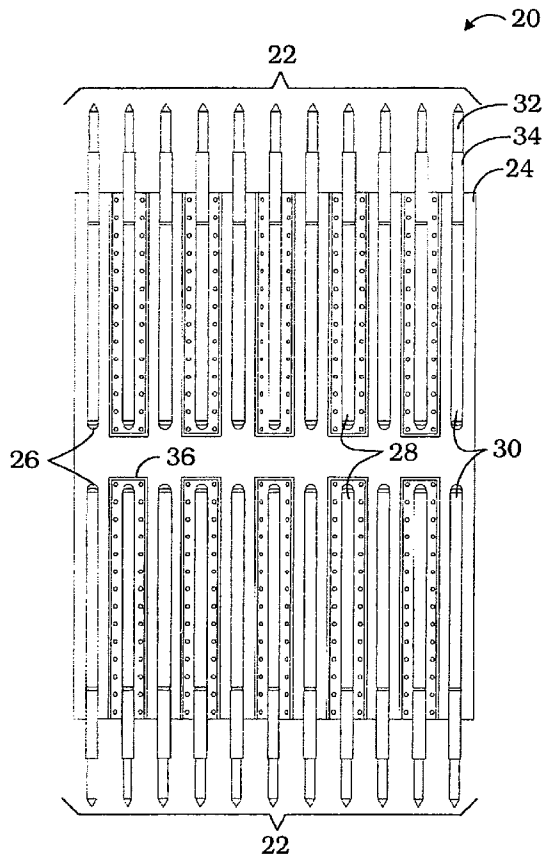

Fig. 1

(57) Abstract: A probe array wafer (20) includes a substrate (24) upon which a plurality of compliant probes (22, 28, 30) are mounted. Pairs of axially aligned probes (28) may be electrically connected together to provide a pass through power connection from the test equipment to the device under test. Likewise, pairs of axially aligned probes (28) may be electrically connected together to probe a ground connection from the test equipment to the device under test.

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PROBE ARRAY WAFER

FIELD OF THE INVENTION

[0001] The present invention relates to compliant probes and, more particularly, to integration of an array of compliant probes into a substrate to connect an array of pads between two circuit boards or electronic assemblies. The substrate enhances the electrical performance of the array of probes.

BACKGROUND

[0002] Interconnecting of two separate boards or components has been accomplished by an array of spring test probes installed into receptacles. The probes are press fit into a matrix of holes drilled in a block. The block is mounted to one circuit board with the probes perpendicular to the surface of the board to mate with a device under test or another circuit board to perform functional testing, parametric testing or burn-in testing, for example.

[0003] Difficulty in installing the probes in the substrate block and accurate location of the retaining holes increases the cost of producing the block of probes. The blocks are not readily adaptable for more complex applications such as testing with active or passive components coupled to the spring probes. Additionally, the block must fit the application and is therefore not adaptable for other applications not having the same probe pattern or probe number.

SUMMARY

[0004] A probe array wafer is provided which includes compliant probes mounted on the edges of an insulating substrate to electrically isolate the probes. The probes are pressed into grooves or slots in the insulating substrate or mounted to the surface of the substrate. For a single layer substrate, pairs of axially aligned probes may be electrically connected together to provide a pass through power connection from the test equipment to the device under test, for example. Likewise, pairs of axially aligned probes may be electrically connected together to provide a ground connection from the test equipment to the device under test. In addition to enabling high quality power distribution, such arrays of probes can also provide high bandwidth signal connections by using controlled impedance circuit board traces between opposing spring probes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Fig. 1 is a front elevation view of the probe array wafer of the present invention.

[0006] Fig. 2 is an end view of the probe array wafer of Fig. 1.

[0007] Fig. 3 is a side view of the probe array wafer of Fig. 1.

[0008] Fig. 4 is a front perspective view of the probe array wafer of Fig. 1.

[0009] Fig. 5 is a rear perspective view of the probe array wafer of Fig. 1.

[0010] Fig. 6 is a front elevation view of a probe array wafer with another compliant probe member.

[0011] Fig. 7 is a perspective view of a probe array wafer and a retainer cap.

[0012] fig. 8 is a partial exploded view of a probe array wafer and retaining block.

[0013] Fig. 9 is a perspective view of a plurality of probe array wafers secured in a retaining block.

DETAILED DESCRIPTION

[0014] Detailed embodiments of the invention are disclosed herein, however, it is to be understood that the disclosed embodiments are merely exemplary of the invention which may be embodied in various forms. Therefore, specific structural and functional details disclosed herein are not to be interpreted as limiting, but rather merely as a basis for teaching one skilled in the art to variously employ the present invention in any appropriate detailed form, and as a basis for the claims.

[0015] Referring to Figs. 1-5, a probe array wafer is generally indicated by reference numeral **20**. Probe array wafer **20** includes spring probes **22** mounted on an insulating substrate **24** to electrically isolate the probe 22. Spring probes **22** may be soldered or pressed into grooves or slots **26** in the insulating substrate **24**. For a single layer substrate **24**, pairs of axially aligned probes **28** may be electrically connected together to provide a pass through power connection from the test equipment (not shown) to the device under test (DUT) (not shown), for example. Likewise, pairs of axially aligned probes **30** may be electrically connected together to provide a ground connection from the test equipment to the DUT.

[0016] All probes **22** are generally coplanar and may be combined in various numbers according to the particular application and DUT. As shown, probes **22** are conventional single-ended compliant probes with a plunger **32** and a barrel **34**. A conductive film, solder or plate **36** may be applied around a groove **26** to provide electrical contact all along the barrel **34**. An insulating gap provides isolation or a probe from the surface metallization **36** that may connect to other probes.

[0017] Referring to Fig. 6, another probe array wafer is generally indicated by reference numeral **70**. Probe array wafer **70** includes an insulating substrate **72** and compliant probe members **74** and **76** extending from opposite edges **78** and **80** of the

substrate **72**. The compliant members may be bent metal, spring probes or other compliant probe. The probes **74** may be connected to the probes **76** using planes or traces in the circuit board (not shown). A multilayer substrate may be used to provide greater functional performance, such as low loop inductance, decoupling capacitance and controlled impedance signal connection in connecting probes along one edge o the substrate to the probes along the other edge.

[0018] Referring to Figs. 7-9, the probe array wafer **20** is mounted in a housing **40** and held in place by front **42** and rear **44** array caps. Alignment tabs **46** are provided along the upper and lower edges and on both sides of the housing **40** to align the array caps **42** and **44**. Array caps **42** and **44** are secured to the housing **40** with fasteners **48**.

[0019] Caps 42 and 44 may include alignment grooves or slots (not shown) which are adopted to receive the probe array wafers **20**. Caps **42** and **44** may also include spaced-apart apertures **52** which are in axial alignment with probes **22**. When the probe array wafer **20** is inserted into cap **44**, for example, the plungers **32** of each of the probes **22** extend through the apertures **52** and the free ends of barrels **34** fit snugly within the apertures **52**. The caps **42** and **44** keep the probe array wafers **20** aligned within the housing **40**.

[0020] One, two or more blocks of probe array wafers **20** may be assembled together within housing **40** and held in place by end caps **42** and **44**. The housing may then be mounted in an automatic test device for various test applications.

[0021] As illustrated in Figs. 1-5, the substrate **24** is a single layer. However, a multi-layer substrate may be used to provide other connectivity options or configurations between the probes **22**. For example, using a multi-layer substrate, a single probe on the test equipment side may be connected to two or more probes on the DUT side of the probe array wafer **20**. The multi-layer substrate provides design flexibility and enhanced electrical performance.

[0022] For a multilayer substrate, the loop inductance may be minimized by spacing the conductive power and ground planes as close together as possible, separated by a thin insulating layer. For a power distribution system of a digital circuit, capacitive decoupling may be accomplished by utilizing one or more surface mount decoupling capacitors sized to reduce noise in the PDS and achieve signal integrity. At low frequencies, a high capacitance applied across the power source will reduce the noise. At higher frequencies, decoupling is more effective with reduced parasitic inductance rather than high capacitance by using low inductance capacitors connected in parallel to achieve the desired decoupling capacitance.

[0023] Other electronic devices (not shown) may be integrated on a multi-layer substrate alone with probes **22**. Such electronic devices may include passive components such as resistors, capacitors or inductors to provide linear analog filtering, for example. Active filters may be included using a combination of passive and active components such as operational amplifiers. Digital filtering may be implemented using general purpose microprocessors or digital signal processors. Additional functionality may be implemented with use of microprocessors and DSPs. The electronic components may be surface mounted on the substrate using manufacturing techniques known in the art.

[0024] It is to be understood that while certain forms of this invention have been illustrated and described, is it not limited thereto except insofar as such limitations are included in he following claims.

CLAIMS

Having thus described the invention, what is claimed as new and desired to be secured by Letters Patent is:

1. An electrical probe assembly comprising:

an insulating substrate,

a plurality of compliant probes secured to said insulating substrate and arranged in two

generally aligned rows, each of said probes having a tip extending beyond an edge of said insulating substrate,

said tips of said plurality of compliant probes in said first row for contacting a test fixture, said tips of said plurality of compliant probes in said second row for contacting one or more devices under test,

whereas select ones of said plurality of probes in said first row are connected to select ones of said probes in said second row.

2. The electrical probe assembly as set forth in claim 1 wherein said plurality of probes are compliant spring probes.

3. The electrical probe assembly as set forth in claim 1 wherein said plurality of probes are compliant bent metal probes.

4. The electrical probe assembly as set forth in claim 1 further comprising a housing adapted to receive and secure a plurality of said substrates in an aligned and spaced apart relationship.

5. The electrical probe assembly as set forth in claim 4 further comprising a pair of end caps fastened to said housing, each of said end caps having a plurality of spaced

apart apertures axially aligned with said plurality of compliant probes extending from said substrates, said apertures adapted to receive said compliant probe tips therethrough.

6. The electrical probe assembly as set forth in claim 1 wherein said insulating substrate includes a plurality of spaced apart grooves each adapted to receive one of said compliant probes.

7. The electrical probe assembly as set forth in claim 1 wherein said insulating substrate includes two or more conducting layers.

8. The electrical probe assembly as set forth in claim 1 further comprising a passive electronic filter mounted to said substrate and in communication between one or more probes in said first row and one or more probes in said second row.

9. The electrical probe assembly as set forth in claim 1 further comprising an active electronic filter mounted to said substrate and in communication between one or more probes in said first row and one or more probes in said second row.

10. The electronic probe assembly as set forth in claim 1 further comprising a microprocessor mounted to said substrate and in communication between one or more probes of said first row and one or more probes of said second row.

11. The electrical probe assembly as set forth in claim 1 further comprising active and passive electronic components mounted to said substrate and in communication between one or more probes of said first row and one or more probes of said second row.

12. An electrical probe assembly comprising:

a housing having open ends,

a plurality of insulating substrates mounted ins aid housing,

a plurality of compliant probes secured toe ach of said insulating substrates and arranged in two generally aligned rows, each of said probes having a tip extending beyond an edge of said insulating substrate.

said tips of said plurality of compliant probes in said first row for contracting a test fixture, said tips of said plurality of compliant probes in said second row for contacting one or more devices under test, and

a pair of end caps, fastened to said open ends of said housing, each of said end caps having a plurality of apertures in axial alignment with said probe tips,

whereas select ones of said plurality of probes in said first row are connected to select ones of said probes in said second row, and whereas said probe tips extend through said apertures of said end caps.

13. The electrical probe assembly as set forth in claim 12 wherein said plurality of probes are compliant spring probes.

14. The electrical probe assembly as set forth in claim 12 wherein said plurality of probes are compliant bent metal probes.

15. The electrical probe assembly as set forth in claim 12 wherein each of said plurality of insulating substrates includes a plurality of spaced apart grooves each adapted to receive one of said compliant probes.

16. The electrical probe assembly as set forth in claim 12 wherein each of said insulating substrates includes one or more conducting layers.

17. The electrical probe assembly as set forth in claim 12 further comprising a passive electronic filter mounted to said substrate and in communication between one or more probes in said first row and one or more probes in said second row.

18. The electrical probe assembly as set forth in claim 12 further comprising an active electronic filter mounted to said substrate and in communication between one or more probes in said first row and one or more probes in said second row.

19. The electronic probe assembly as set forth in claim 12 further comprising a microprocessor mounted to said substrate and in communication between one or more probes in said first row and one or more probes og said second row

20. The electronic probe assembly as set forth in claim 12 further comprising active and passive electronic components mounted to said substrate and in communication between one or more probes of said first row and one or more probes in said second row.

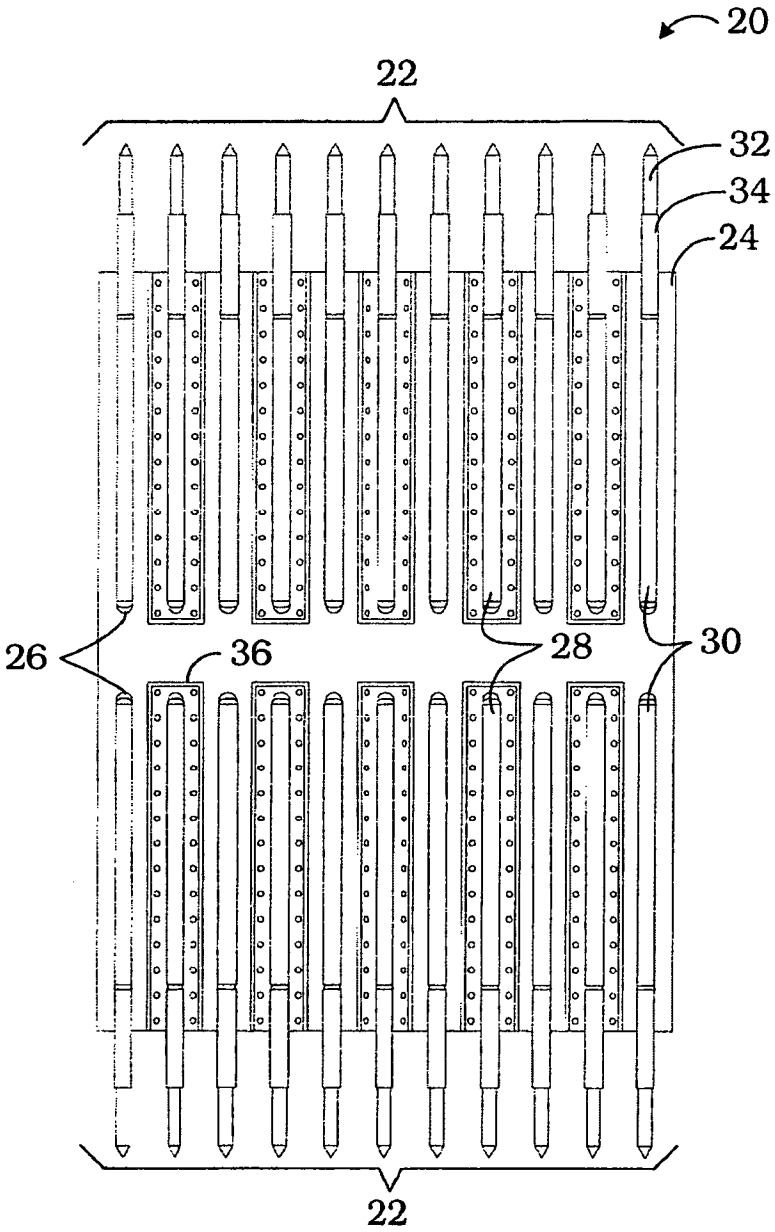

Fig. 1

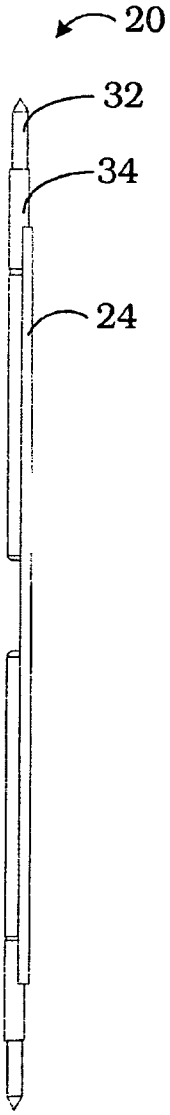

Fig. 3

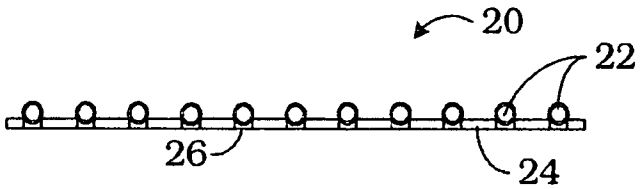

Fig. 2

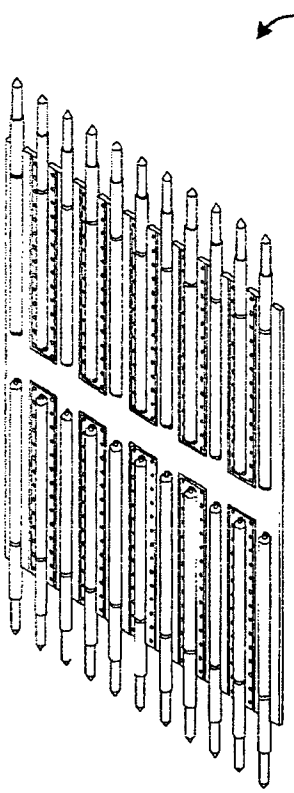

Fig. 4

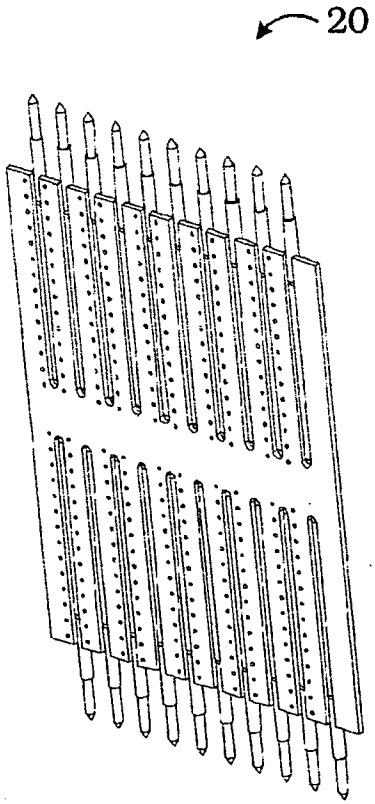

Fig. 5

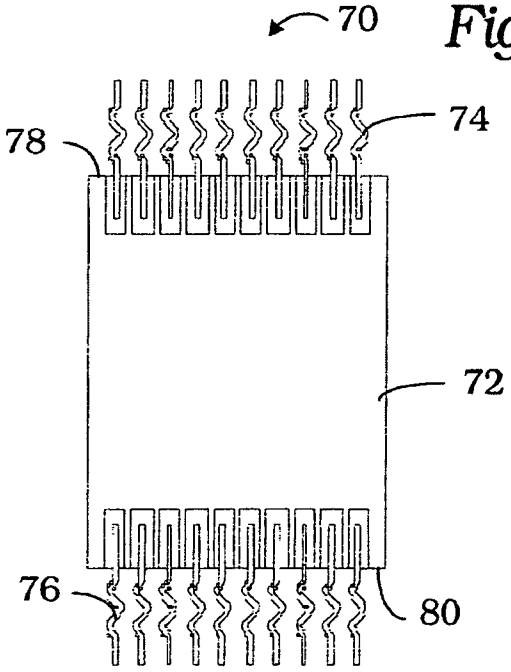

Fig. 6

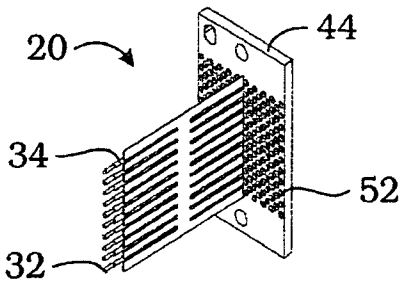

Fig. 7

Fig. 8

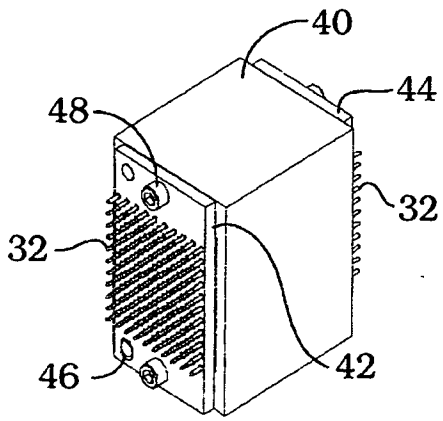

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US07/76841

A. CLASSIFICATION OF SUBJECT MATTER
IPC: **G01R 31/02**(2006.01)

USPC: 324/754
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 324/754

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,359,452 B2 (MOZZETTA et al) 19 March 2002 (19.03.2002), figs 2-3, col. 4, line 5 - col. 6, line 35.	1-2, 6 --- 4, 7-11
Y	US 5,276,395 (MALLOY et al) 4 January 1994 (04.01.1994), figs. 1-4, col. 5, lines 7-65.	4
Y	US 5,639,385 (MCCORMICK et al) 17 June 1997 (17.06.1997), fig. 3A, col. 12, lines 12-62.	7
Y	US 4,780,670 (CHERRY et al) 25 October 1988 (25.10.1988), fig. 2, col. 3, lines 12-64.	8-11
A	US 5,134,363 (LANG-DAHLKE et al) 28 July 1992 (28.07.1992), col. 2, lines 8-65.	
A	US 4,862,075 (CHOI et al) 29 August 1989 (29.08.1989), col. 3, lines 55-68.	

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search
09 June 2008 (09.06.2008)

Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US07/76841

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,352,061 (MATRONE et al) 28 September 1982 (28.09.1982), col. 2, lines 58 - col. 4, line 9.	
A	US 4,931,726 (KASUKABE et al) 5 June 1990 (05.06.1990), col. 7, lines 10-48.	
A	US 6,570,399 B2 (YEGHIAYAN et al) 27 May 2003 (27.05.2003), col. 7, lines 1-15.	
A	US 4,506,215 (COUGHLIN et al) 19 March 1985 (19.03.1985), col. 4, lines 13-57.	
A	US 4,833,402 (BOEGH-PETERSEN et al) 23 May 1989 (23.05.1989), col. 12, line 14 - col. 13, line 20.	