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Controlled RAM signal processor

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GBA 2015847

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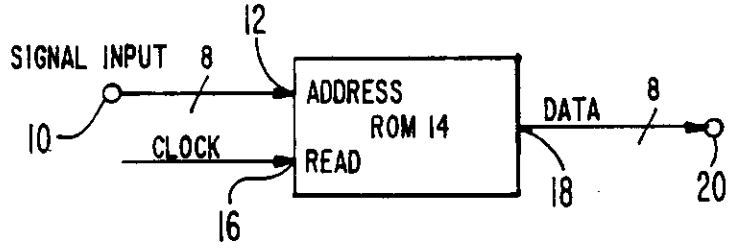

Fig. 1
PRIOR ART

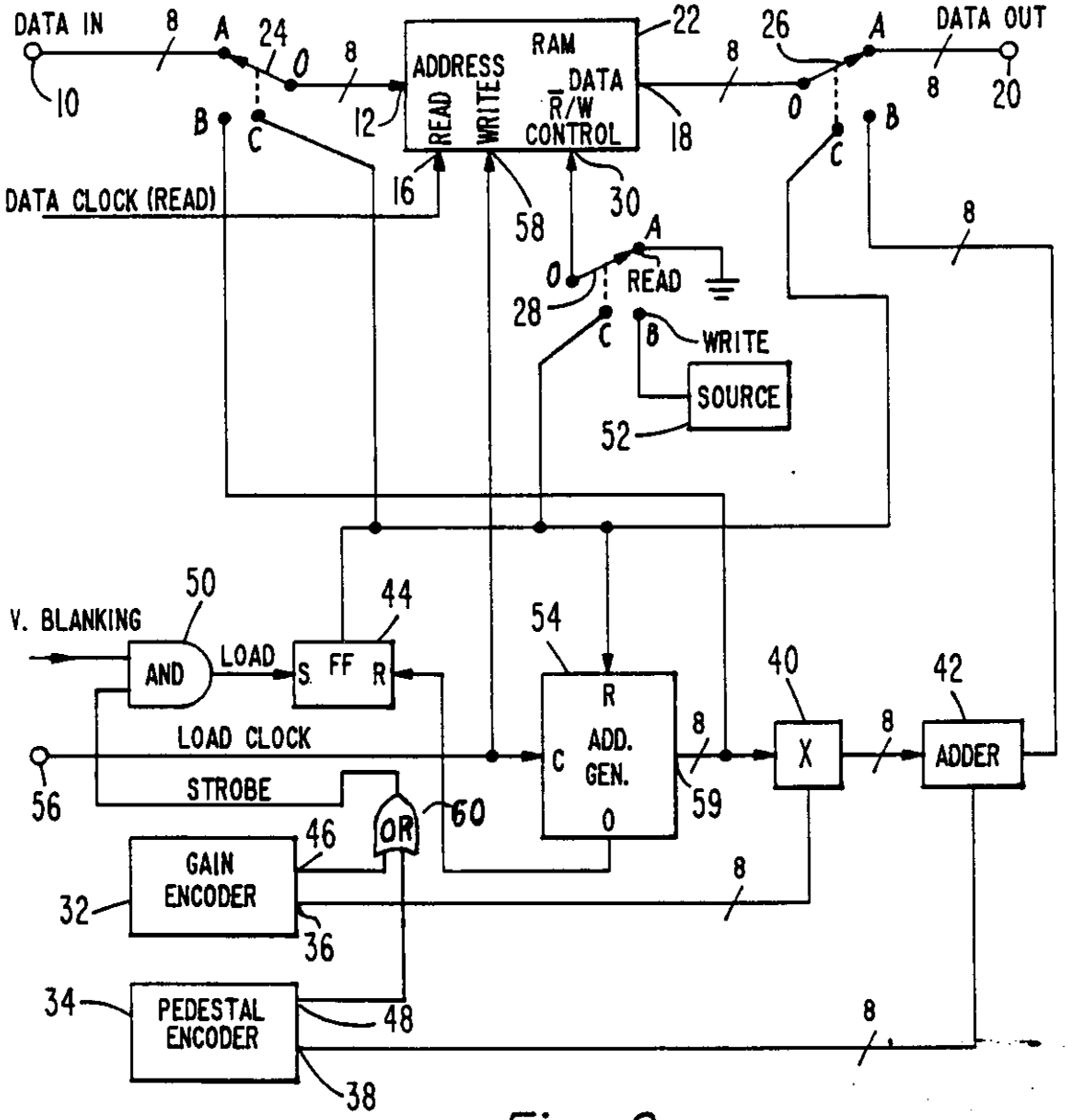

Fig. 2

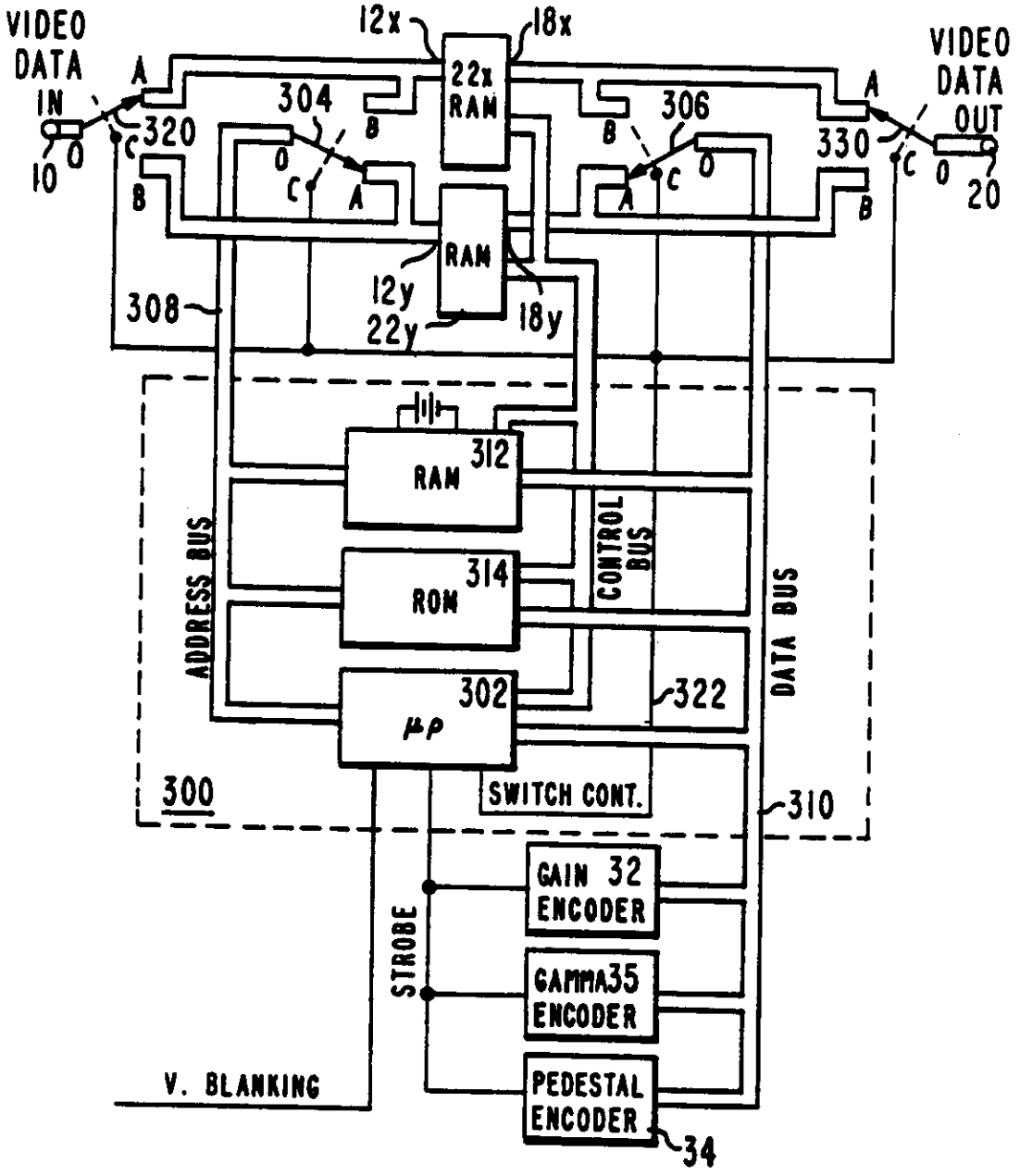
VIDEO DATA IN
10
320
304
306
330
VIDEO DATA OUT
20
12x
18x
22x RAM
RAM
12y
22y
18y
308
312
RAM
314
ROM
302
μP
322
ADDRESS BUS
CONTROL BUS
DATA BUS
300
SWITCH CONT.
310
GAIN 32 ENCODER
GAMMA35 ENCODER
PEDESTAL ENCODER
34
STROBE
V. BLANKING

Fig. 3

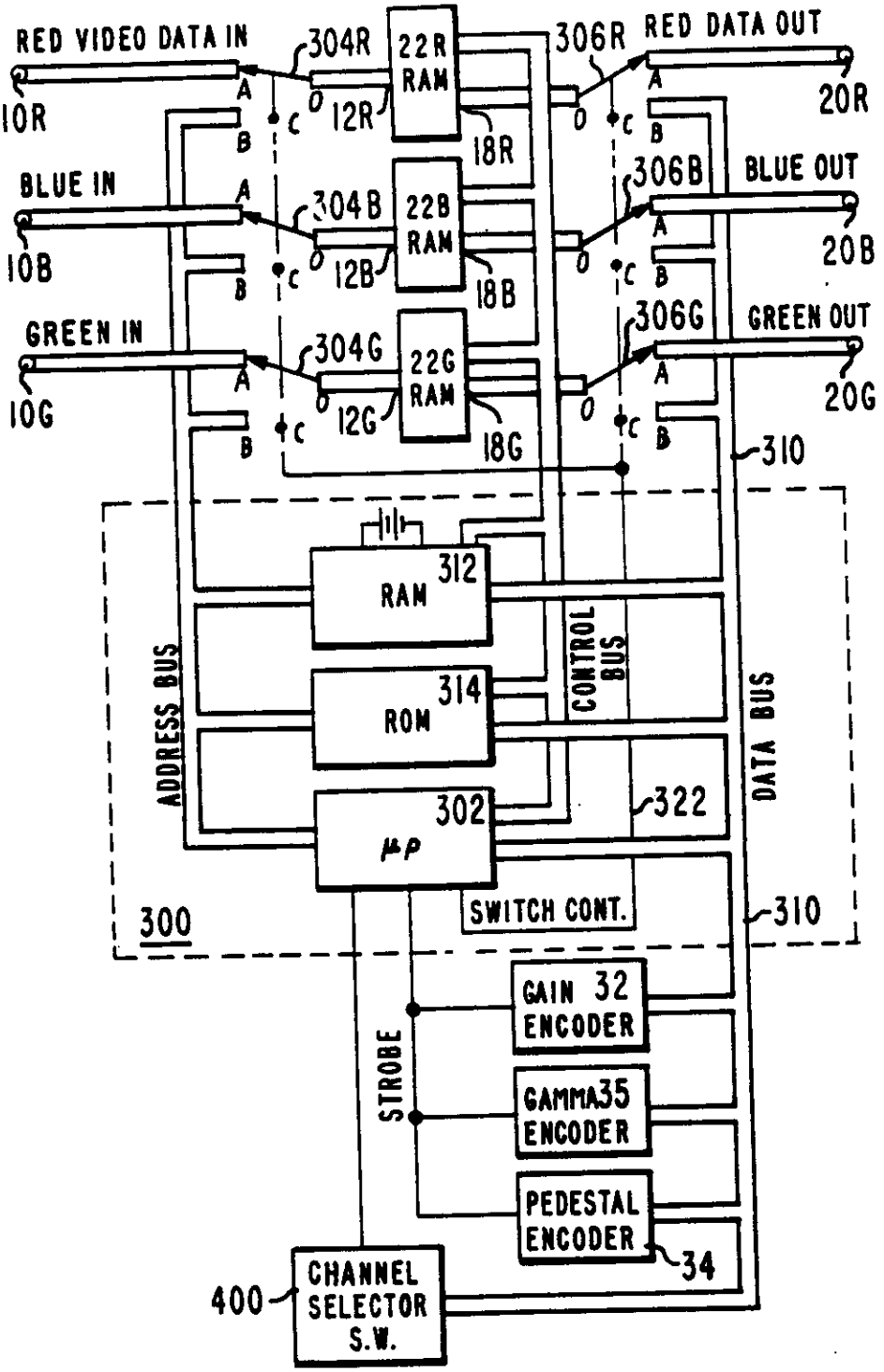
RED VIDEO DATA IN
10R
304R
22R RAM
12R
18R
306R
RED DATA OUT
20R
BLUE IN
10B
304B
22B RAM
12B
18B
306B
BLUE OUT
20B
GREEN IN
10G
304G
22G RAM
12G
18G
306G
GREEN OUT
20G
310
RAM
312
ROM
314
μP
302
322
ADDRESS BUS
CONTROL BUS
DATA BUS
SWITCH CONT.
300
310
GAIN 32 ENCODER
GAMMA35 ENCODER
PEDESTAL ENCODER
34
STROBE
400
CHANNEL SELECTOR S.W.

Fig. 4

CONTROLLED RAM SIGNAL PROCESSOR

The present invention relates to a high-speed digital signal processor and more particularly to the type of processor utilizing a look-up table to generate the output signal from an input signal such as a video signal.

In the prior art, it is known to use a read-only memory (ROM) for processing digital signals at high speed. (A ROM has data prestored in its locations by, for example, IC mask layout, or electrically blowing internal fuses.) As illustrated in FIGURE 1, digital signals, such as a video signal, are applied in parallel to an 8-bit input terminal 10, and from there to an 8-bit address input 12 of a ROM 14. The digital video signals may come, for example, from an A/D converter (not shown) operated at a clock rate. The input of the converter would have an analog video signal applied to it so that the input video signal is sampled and then 8-bit quantized (256 grey levels) at the clock rate. The clock which drives the ADC (not shown) is also applied to a read input 16 of ROM 14. For each possible signal value applied to the ROM address 12, there is a corresponding ROM memory location which contains data which may be read from an 8-bit ROM data output 18 and from there to an 8-bit output terminal 20. Typically, line 20 will be 8-bits wide for television applications, but may have other values.

The processing performed on the input signal depends on the data stored in the ROM 14. For example, if the datum stored in each ROM location is a value representative of one-half the address of that location, the output will represent one-half of the input, and ROM 14 functions as a 2:1 attenuator. Other amplitude functions are possible. For example, in order to provide limiting, the data stored in some ROM locations are values representing one-half the address of those locations. However, ROM locations for addresses above a particular value all contain data representing one-half of this particular value. This will give a linear gain of one-half up to the limiting value and no increase after that value.

In a similar manner, pedestal functions may be generated by storing in each ROM location data representing the address of those locations summed with a fixed offset value. Gamma correction can be accomplished by setting the values stored in each ROM location in accordance with a predetermined exponential gamma function such as a square-root function.

The described prior art system has the disadvantage that the transfer function is fixed in the ROM memory. For example, if three identical such ROMs were used, each one controlling the gain, pedestal and gamma of one of three color representative signals derived from a vidicon, analog controls would have to precede the ADC to standarize the three signal levels entering the ROMs. In the absence of such standardization, the ROMs could not be used because the transfer functions could not be varied to meet varying conditions. It would be possible, of course, to change the ROMs as described in U.S. Patent No. 4,316,219, issued February 16, 1982, for Terence Smith and Frank Marlowe and entitled "SYNCHRONIZING CIRCUIT ADAPTABLE FOR VARIOUS TV STANDARDS." While this allows changing ROMs when a different use is intended, it does not solve the problem of variations encountered during use.

It is therefore desirable to have a signal processor that can change its transfer function during use.

According to the present invention, a digital look-up table signal processing system is provided having at least one signal processing channel including at least one RAM having data terminals for providing data representative of look-up contents in a location of the RAM selected by a signal to be processed applied as an address signal input. The contents of the RAM are in accordance with a composite transfer function. From control signals determinative of components of the composite transfer function appropriate new contents of said locations are obtained according to a predetermined algorithm and the RAM is loaded with these new contents. It will be appreciated that a RAM is a memory which may have data read from and written into addressed locations.

In the drawings:

FIGURE 1 shows a typical prior art signal processor using a ROM as already described;

FIGURE 2 shows a RAM hardwired processor in accordance with a first embodiment of the invention;

FIGURE 3 shows a microprocessor controlled second embodiment; and

FIGURE 4 shows a plural channel embodiment.

FIGURE 2 shows a hardwired embodiment of the invention for use in one channel of a television camera. The ROM 14 of FIGURE 1 has been replaced by a RAM 22 to allow control of the transfer function between data input 10 and data output 20 during use. During normal operation, an 8-bit digital video signal from a camera tube and A/D converter (not shown), for example, is applied to data input 10 and from there to a pole A of an 8-bit switch 24 (8 poles, one for each data bit). A terminal O of switch 24 is coupled to address input 12 of RAM 22. A data clock signal is applied to a read clock input 16 of RAM 22. When switch 24 is in the A position, the input data 10 is applied to the address input 12 of RAM 22. A read/write control input 30 of RAM 22 is coupled to a terminal O of a switch 28. A pole A of switch 28 is coupled to ground. When switch 28 is in position A, the read/write control input 30 is grounded placing RAM 22 in a read mode. For each value of input data applied as an address to RAM 22, there is a corresponding memory location which contains data in accordance with a previously stored transfer function. The data stored in the memory location corresponding to the value of the video signal applied to the address terminal 10 appears at a data terminal 18 of RAM 22 at each clock pulse. The data terminal 18 of RAM 22 is coupled to a terminal O of an 8-bit switch 26. A pole A of switch 26 is coupled to the data output 20. When switch 26 is in the A position, the data terminal 18 of RAM 22 is coupled to the data output 20.

Switches 24,26, and 28 all have control inputs C. When a voltage corresponding to logic 'o' (ground for TTL logic) is applied to the control input, the switch assumes the A position. When a voltage corresponding to a logic '1' (+5 volts for TTL logic) is applied to the control input,

the switch assumes the B position. Although shown as mechanical switches, it should be appreciated that switches 24,26 and 28 are electronic switches in the preferred embodiment.

An output of a flip-flop 44 is coupled to the control terminals of switches 24,26, and 28. When the flip-flop 44 is reset, a logic 'o' is applied to the switches 24,26, and 28. In this case, all the switches assume the A position, and the apparatus operates as described above.

So long as the contents of RAM 22 are not changed, it operates precisely as does ROM 14 of FIGURE 1, providing an amplitude change according to the programmed function.

Assuming that a pedestal or a gain function of the camera tube of a particular channel changes, it may be desirable to alter the programming, i.e., the transfer function of RAM 22. These changes will ordinarily become apparent while the camera is in use. The user does not usually have facilities for analyzing the desired transfer function and reprogramming the RAM. Consequently, the camera as sold to the user must provide some means for adjustment of the transfer function. Ideally, the means provided will have user controls which perform in the same manner as the analog pedestal or gain functions with which the user is familiar.

According to the invention, the changes are initiated by entering new gain and pedestal values on gain and pedestal digital shaft encoders 32 and 34, respectively. The new gain or pedestal values are present at 8-bit outputs 36 and 38, respectively, and are applied to 8-bit inputs of an 8-bit multiplier 40 and an 8-bit adder 42, respectively. Encoders 32 and 34 also produce, at outputs 46 and 48, signals indicating that the encoders have new values available at the 8-bit outputs 36 and 38, respectively. The new-value outputs 46 and 48 are coupled to first and second inputs, respectively, of an OR-gate 60. The output of the OR-gate 60 is a strobe signal which is applied to one input of an AND gate 50. The other input of

gate 50 receives a vertical blanking signal from synchronization circuits (not shown) present in the camera. The output of gate 50 provides a load command signal, which occurs only during the vertical blanking interval to avoid possible disturbances in the displayed picture due to transfer function changes during active video. If desired, the load signal can be made to occur during several horizontal blanking intervals.

The load signal from gate 50 is applied to a set input S of a flip-flop 44, Flip-flop 44 provides an output signal that controls switches 24,26, and 28. As described above, when flip-flop 44 is 'set', the switches 24,26 and 28 all assume position B. A source 52 applies a voltage to pole B of switch 28. When switch 28 is in position B, the read/write control input 30 of RAM 22 is at a voltage supplied by source 52 placing RAM 22 in the write mode. Flip-flop 44 is also coupled to a reset input R of an address generator 54. When flip-flop 44 is 'set', address generator 54 is reset to zero. A load clock pulse signal received at an input 56 from a load clock generator (not shown) is applied to a write clock input 58 of RAM 22 and to a clock input C of address generator 54. Output 59 of address generator 54 is coupled to pole B of switch 24 and to a second input of multiplier 40.

Address generator 54 sequentially provides, at the load clock rate, binary address signals representing the decimal numbers 0 to 255. When switch 24 is in position B, these address signals are applied to address input 12 of RAM 22. The load clock generator rate is selected to allow generator 54 to generate 255 addresses during the vertical blanking interval.

The address signals applied to multiplier 40 are multiplied by the gain determined by gain encoder 32. The resulting product output signal is applied to adder 42. For example, if the gain is one, then the addresses from generator 54 are applied unchanged to adder 42 (i.e., multipled by 1); if the gain is one-half, then signals representing one-half the value of the address are so

applied.

An adder 42 adds a pedestal (D.C. offset) as determined by pedestal encoder 34 to the product signal. The resulting sum signal is provided to pole B of switch 26. When switch 26 is in position B, the sum signal from adder 42 is applied to data terminal 18, which functions as a data input.

An overflow output O of address generator 54 is coupled to a reset input R of flip-flop 44. When generator 54 provides a signal at output 59 corresponding to decimal 255, overflow output 0 of generator 54 provides a high output signal to reset input R of flip-flop 44 that indicates that the writing into RAM 22 has been completed. Flip-flop 44 is reset, and switches 24,26, and 28 assume position A, as illustrated in FIGURE 2. Also, read/write control input 30 of RAM 22 is grounded, placing RAM 22 in the read mode. Therefore, signals coming in at input 10 can now be applied to RAM 22 through switch 24 and processed therein in accordance with the new gain and pedestal transfer functions and an output signal provided to output 20 through switch 26.

FIGURE 3 shows a microprocessor-controlled second embodiment of the invention where corresponding elements have been given corresponding reference numerals. As shown therein, RAM 22 of FIGURE 2 has been replaced by two RAMs 22x and 22y. This enables one RAM to process the video signal, while the other RAM can have its transfer function changed during the active video portion of the scanning raster without causing disturbances in the viewed scene. For example, for switches in the positions illustrated in FIGURE 3, a switch 320 routes the video data at terminal 10 to an address input 12x of a RAM 22x, and a switch 330 connects a data terminal 18x to video data output 20. Thus, RAM 22x processes the video signal in accordance with the transfer function therein.

A block 300 is controlled by a microprocessor 302. An address buss 308 of microprocessor 302 is connected to a terminal O of a switch 304, and a data buss 310 of the

microprocessor 302 is connected to a terminal O of switch 306. Block 300 carries signals over the 8-bit data buss 310 which may be generated by any signal source connected to it. As illustrated, signal sources are a gain encoder 32, a gamma encoder 35, and a pedestal encoder 34. Other sources such as thumb-wheel switches, or potentiometers with analog-to-digital converters coupled to their respective outputs, could be used.

A ROM 314 of block 300 includes a preprogrammed fixed equation representing various factors affecting the transfer function. For example, if the functions of gain, pedestal and gamma are to be provided, it is important to know whether the pedestal is to be applied before or after the gamma correction. If the function of the block is to correct for errors generated by the camera tube, the pedestal addition should precede the gamma corrections. On the other hand, if the pedestal addition is to compensate for later-occuring clamp offsets, the gamma correction should precede the pedestal addition. ROM 314 also contains a set of instructions for carrying out the calculation.

Block 300 also includes a nonvolatile memory which may be, for example, a RAM 312 with battery back-up operation. RAM 312 stores the present value of the various parameters being processed. In a particular example, the nonvolatile memory may include the number 0.5 representing the present value of the gain, a value of pedestal which may, for example, presently be zero, a value of gamma, which may be 0.5. At turn-on, microprocessor 302 calculates the transfer function value for the first address value of RAMs 22x and 22y. The microprocessor 302 utilizes the three values stored in nonvolatile memory 312, in an appropriate equation stored in ROM 314 (in accordance, for example, with whether gamma correction precedes or succeeds pedestal addition). Having made the calculation, the result is stored in RAM 22y assuming switches 304 and 306 are in the position A, as shown in FIGURE 3. Microprocessor 302 then proceeds to the second address, again performs the calculation and stores the result in RAM 22y. Microprocessor

302 continues to step through the addresses and for each step performs calculations giving the desired transfer function.

At the end of the calculation interval, switches 304, 306, 320, and 330 are switched during the next vertical interval by microprocessor 302 acting through a switch control line 322 to be in positions opposite that shown in FIGURE 3. Thus, the video data at input 10 is applied by switch 320 to address input 12y of RAM 22y and switch 330 connects data terminal 18y of RAM 22y to output terminal 20. Hence, RAM 22y now processes the video signal in accordance with the new transfer function stored therein. Switches 304 and 306 connect address and data busses 308 and 310, respectively, to address input 12x and data terminal 18x, respectively, of RAM 22x. Thus, when it is next desired to change gain, gamma, or pedestal functions, the new values are stored in RAM 22x. During the next vertical interval, switches 320, 304, 306 and 330 are switched into the positions shown in FIGURE 3, and hence RAM 22x once again processes the video signal.

In systems where interruptions in the video signal are tolerable, such as pre-air time set-up adjustments, it is possible to use only one of the RAMs 22x and 22y. In such systems, the video output signal would be switched off while loading of the RAM occurs.

FIGURE 4 shows a plural channel third embodiment of the invention, wherein corresponding reference numerals are used with corresponding elements and the letters R, G, B are added to the numerals to indicate elements in the red, green and blue channels. As shown in FIGURE 4, a channel selector encoder 400 determines which channel is having the transfer coefficient of its particular RAM 22R, 22G, or 22B changed. Then microprocessor 302 addresses only that particular RAM to provide the change in transfer function. If it is desired that all channels have the same transfer function, all RAMs would be addressed for loading at the same time. Further, two RAMS per channel can be used as in the single channel embodiment of FIGURE 3. Still further,

the new coefficients can be loaded into RAM 312 as they are being calculated. After the calculation is complete, during the next occurring vertical interval, the new coefficients can be rapidly transferred from RAM 312 to at least one of RAMS 22R, 22B, and 22G. This makes the video signal discontinuity short, and it occurs only during the vertical interval. To reduce even this short discontinuity, a blanking signal can be connected to at least one of outputs 20G, 20B and 20R during the occurrence of the discontinuity. For some applications, this procedure eliminates the need for two RAMs per channel.

It will be appreciated that many other embodiments are possible within the scope of the invention. For example, encoders 32, 34 and 35 can contain memory, RAM 312 can then be a volatile type.

Further, if the calculation for the new look-up value is unduly complicated, and not many calculations are required, then these calculations can be done beforehand and stored in ROM 314. At the appropriate time, the look-up data can be transferred to RAMs 22x or 22y. Still further, partial calculations may be done beforehand with final calculations done just before said transfer.

As used in this description and claims, "RAM" means a random access read/write memory. Further, "high speed" means the RAM can operate at the signal data rate.

CLAIMS:

1. A digital look-up table signal processing system comprising:

a first signal processing channel including at least a first RAM having data terminals for providing data representative of look-up contents in a location of said RAM selected by an address signal input, said contents being in accordance with a composite transfer function;

means for applying a signal to be processed to said address signal input;

means for providing control signals for determining components of said composite transfer function;

means for obtaining from said control signals appropriate new contents for said locations according to a predetermined algorithm; and

means for loading said RAM with said new contents.

2. A system as claimed in claim 1, wherein said signal processing channel further comprises a second RAM and means for alternatively switching the signal to be processed to one or the other of said first and second RAMs as address signal input thereto said loading means loading only that RAM to which that signal is not so switched.

3. A system as claimed in claims 1 or 2, further comprising second and third signal processing channels;

wherein all of said RAMs of said signal processing channels are loaded by said loading means.

4. A system as claimed in claim 3 wherein said channels are for processing signals representing red, green and blue color component signals of a television signal.

5. A system as claimed in any preceding claim wherein said means for providing said control signals comprise a plurality of digital shaft encoders.

6. A system as claimed in any preceding claim, wherein said means for providing said control signals comprise means for controlling at least one of gain, pedestal, and gamma functions.

7. A system as claimed in any preceding claim, wherein said obtaining means comprises a means for calculating said new contents.

8. A system as claimed in Claim 7, wherein said calculating means comprises circuitry coupled together in accordance with said algorithm.

9. A system as claimed in Claim 7, wherein said calculating means comprises a ROM means for storing said algorithm and a microprocessor coupled to said ROM means.

10. A system as claimed in any preceding claim, wherein said loading means comprises an address generator having an input means for receiving a load clock and an output coupled to said RAM.

11. A system as claimed in any of claims 1-9, wherein said loading means comprises a microprocessor coupled to said RAM.

12. A system as claimed in Claims 10 or 11, wherein said loading means comprises means for ensuring loading of said RAM only during a blanking interval of said signal to be processed.

13. A system as claimed in any preceding claim, wherein said obtaining means comprises means for storing at least a portion of said new contents.

14. A system according to any preceding claim wherein said system is in a television camera.

15. A digital signal processing system substantially as hereinbefore described with reference to Fig. 2, Fig. 3 or Fig. 4 of the accompanying drawings.

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5th Year	
6th Year	
7th Year	
8th Year	
9th Year	
10th Year	
11th Year	
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14th Year	
15th Year	
16th Year	
17th Year	
18th Year	
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Patent ceased or expired:	