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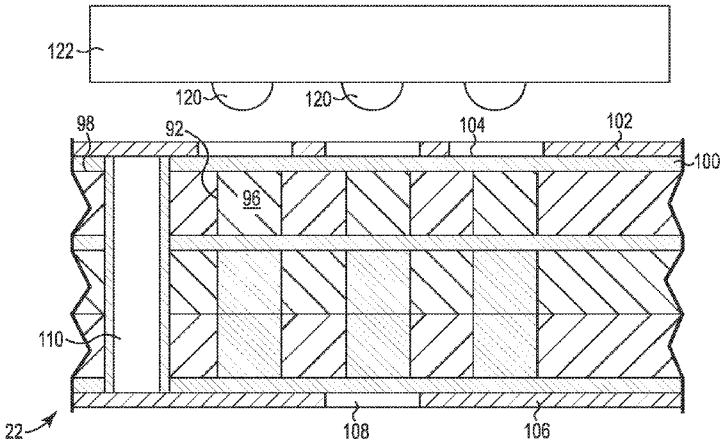


Fig. 7

(57) Abstract: A high density region for a low density circuit. At least a first liquid dielectric layer is deposited on the first surface of a first circuitry layer. The dielectric layer is imaged to create plurality of first recesses. Surfaces of the first recesses are plated electro-lessly with a conductive material to form first conductive structures electrically coupled to, and extending generally perpendicular to, the first circuitry layer. A plating resist is applied. A conductive material is electro-plated to the first conductive structure to substantially fill the first recesses, and the plating resist is removed.

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HYBRID PRINTED CIRCUIT ASSEMBLY WITH LOW DENSITY MAIN CORE AND EMBEDDED HIGH DENSITY CIRCUIT REGIONS

Cross-Reference to Related Applications

[0001] This application claims the benefit of United States Provisional Application No. 61/669,884, filed July 10, 2012, the disclosure of which is hereby incorporated by reference.

Technical Field

[0002] The present disclosure relates to a high density circuit embedded or merged with a lower density circuit, such as a printed circuit board ("PCB"). The present method merges processes used in the printed circuit and semiconductor processing.

Background of the Invention

[0003] Traditional printed circuits are often constructed in what is commonly called rigid or flexible formats. The rigid versions are used in nearly every electronic system, where the printed circuit board (PCB) is essentially a laminate of materials and circuits that when built is relatively stiff or rigid and cannot be bent significantly without damage.

[0004] Flexible circuits have become very popular in many applications where the ability to bend the circuit to connect one member of a system to another has some benefit. These flexible circuits are made in a very similar fashion as rigid PCB's, where layers of circuitry and dielectric materials are laminated. The main difference is the material set used for construction. Typical flexible circuits start with a polymer film that is clad, laminated, or deposited with copper. A photolithography image with the desired circuitry geometry is printed onto the copper, and the polymer film is etched to remove the unwanted copper. Flexible circuits are very commonly used in many electronic systems such as notebook computers, medical devices, displays, handheld devices, autos, aircraft and many others.

[0005] Flexible circuits are processed similar to that of rigid PCB's with a series of imaging, masking, drilling, via creation, plating, and trimming steps. The resulting circuit can be bent, without damaging the copper circuitry. Flexible circuits are solderable, and can have devices attached to provide some desired function. The materials used to make flexible circuits can be used in high frequency applications

where the material set and design features can often provide better electrical performance than a comparable rigid circuit.

[0006] Flexible circuits are connected to electrical system in a variety of ways. In most cases, a portion of the circuitry is exposed to create a connection point. Once exposed, the circuitry can be connected to another circuit or component by soldering, conductive adhesive, thermo-sonic welding, pressure or a mechanical connector. In general, the terminals are located on an end of the flexible circuit, where edge traces are exposed or in some cases an area array of terminals are exposed. Often there is some sort of mechanical enhancement at or near the connection to prevent the joints from being disconnected during use or flexure.

[0007] In general, flexible circuits are expensive compared to some rigid PCB products. Flexible circuits also have some limitations regarding layer count or feature registration, and are therefore generally only used for small or elongated applications.

[0008] Rigid PCBs and package substrates experience challenges as the feature sizes and line spacing are reduced to achieve further miniaturization and increased circuit density. The use of laser ablation has become increasingly used to create the via structures for fine line or fine pitch structures. The use of lasers allows localized structure creation, where the processed circuits are plated together to create via connections from one layer to another. As density increases, however, laser processed via structures can experience significant taper, carbon contamination, layer-to-layer shorting during the plating process due to registration issues, and high resistance interconnections that may be prone to result in reliability issues. The challenge of making fine line PCBs often relates to the difficulty in creating very small or blind and buried vias.

[0009] The process used by current technology is based upon a dry film process, where a substrate of some sort has a copper layer as the base circuit layer onto which a dry film is applied. The dry film is then patterned with a laser to create the circuit patterns. The next copper layer is added and etched as appropriate, with the laser used to drill through the film to expose the previous copper layer so a via can be plated to join the circuit layers. This process is typically used for semiconductor package substrates and larger format circuit boards, such as used in a cell phone. For larger format circuit boards, the dry film technology is used to build fine line

circuits on top of base circuit board made with conventional low density lamination techniques.

[0010] In both cases, the package substrate and the larger format circuit board build up are very expensive compared to traditional low density laminate technology, and suffer from several limitations inherent to the process. For example, in the case where a low density laminate base is used as the starting point for subsequent high density layers are built up, the cost increases dramatically since the entire surface of the lower density base board must be processed with the build up process across the entire area, not just in the areas where the high density is required.

[0011] Another limitation is the reliability of the via structures joining one circuit layer to another, which tend to be a barrel plated structures with the side walls of the via plated and in many cases must be filled with a via fill material to eliminate an air pocket which may separate during solder reflow temperatures. The vias require drilling through the dry film to expose the previous circuit layer in order to create the via that connects the circuit layers. The dry film is applied as a solid contiguous sheet where the material on that particular layer is restricted to that particular material across the entire layer in the build up less the areas ablated to create the via target for joining the previous and subsequent circuit layers. That is, the dry layer film is homogeneous across the entire layer.

Brief Summary of the Invention

[0012] The present disclosure relates to a high density localized circuit region embedded or merged with a lower density circuit, such as a PCB, flexible circuit, or the like. The present method merges processes used in the printed circuit and semiconductor packaging industries that will enable next generation electrical performance. By combining methods used in the PCB and flexible circuit fabrication and semiconductor packaging industries, the present disclosure enables fine line high density circuit structures with attractive cost of manufacture.

[0013] The present disclosure permits bulk conductive material to be added to create a very small low resistance vias to increase density and reduce line and feature pitch of the high density circuit. The printed circuit can be produced to replicate a traditional circuit, or it can be an interconnect to one or more members of a system embedded or incorporated. In basic terms, the structure leverages methods used in the semiconductor packaging industry such as pillar termination to act as the via connecting layers within the circuit stack. In addition, the high density circuit can be

treated as a system of its own by incorporating printed transistors or other passive and active function.

[0014] As noted above, printed circuit fabrication methods have advanced in recent years due to the adoption of high performance smart phones and tablet computers. These small form factor circuit boards are often made with what is called a High Density Interconnect ("HDI") or Build Up process, where the main substrate has the lower density regions and the higher density regions are built up onto the lower density core. This process employs a dry film with laser drilled vias within the build-up areas to create the layer to layer interconnect.

[0015] The present disclosure also provides a high density circuit structure embedded or merged with a lower density main PCB produced with a low cost conventional fabrication method. The present fabrication process includes depositing a liquid dielectric material onto a high density substrate, patterning the dielectric material to create desired features and via locations, processing the dielectric material to create a surface that will accept electro-less copper deposition, directly metalizing, etching to create circuit patterns, copper flash or electro-deposit plating to build up thicker copper structures etc., with steps repeated to create multiple layers.

[0016] The merger of the high density circuit structure to the lower density circuit is typically accomplished by targeting copper terminal points in the lower density circuit that are plated together with corresponding locations within the high density circuit. The final assembly is optionally coated with final mask that essentially provides the appearance of a contiguous construction.

[0017] In one embodiment, a high density coupon which appears similar in nature to a semiconductor package substrate is mated with corresponding terminal locations within the low density circuit and plated or thermal compression bonded together. The high density circuit can also be formed in situ directly on the low density circuit.

[0018] The present disclosure includes electro-less plating surfaces of recesses in dielectric layers to create conductive structures, such as vias. The plated recesses are then filled with a conductive material using electroplating techniques. The resulting structure is a very small low resistance vias that permits increased density and reduced line and feature pitch

[0019] The present high performance electrical circuit can be treated as a system of its own by incorporating electrical devices or other passive and active function,

such as for example, ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. In some embodiments, the electrical devices can be formed using printing technology, adding intelligence to the circuit assembly.

[0020] The liquid dielectric can be processed to create vias and associated circuit geometry having a variety of shapes and sizes, depending on the terminal structure on the circuit members. The contact members and vias can be positioned at a variety of locations, heights, or spacing to match the parameters of existing connections making it easy to replace an existing circuit without changing hardware or the low density circuit. The present disclosure permits the creation of blind or buried conductive structures on very tight pitch of about 25 microns or below without the use of laser ablation.

[0021] Traditional PCB and flex circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. The present disclosure employs a mix of additive and subtractive technologies to permit a wide variety of materials to be applied on a single layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0022] The present disclosure is directed to a high density region for a low density circuit. At least a first liquid dielectric layer is deposited on the first surface of a first circuitry layer imaged to create a plurality of first recesses. Surfaces of the first recesses are plated electro-lessly with a conductive material to create a first conductive structure electrically coupled to, and extending generally perpendicular to, the first circuitry layer. A conductive material is electro-plated to the first conductive structure to substantially fill the first recesses. At least a second liquid dielectric layer is deposited on the first dielectric layer to include a plurality of second recesses imaged to generally align with a plurality of the first conductive structures. Surfaces of the second recesses are plated electro-lessly with a conductive material create second conductive structures electrically coupled to, and extending generally

perpendicular to, the first conductive structures. A conductive material is electro-plated to the second conductive structures to substantially fill the second recesses.

[0023] In one embodiment, an IC device is electrically coupled to the plating in a plurality of the second recesses.

[0024] The high density region can include a second circuitry layer located on the second dielectric layer and electrically coupled with a plurality of the second conductive structures. A third dielectric layer is optionally deposited on the second dielectric layer imaged to include a plurality of third recesses generally aligned with a plurality of the second conductive structures.

[0025] The high density region can include a conductive material plated on surfaces of a plurality of the third recesses to create a third conductive structure electrically coupled to, and extending parallel to the second conductive structures. A conductive material is electro-plated to the third conductive structures to substantially fill the third recesses. An IC device including a plurality of contact pads is electrically coupled to a plurality of the third conductive structures, wherein the IC device is electrically coupled by one of a flip chip attachment directly to a plurality of third conductive structures, solder balls, or wire bonding.

[0026] The high density circuit can be constructed on the low density circuit or as a separate structure that is later merged with the low density circuit. In one embodiment, the first circuitry layer is formed on the low density circuit and the high density circuit is formed on the first circuitry layer.

Brief Description of the Several Views of the Drawing

[0027] Figures 1A and 1B are top and side views of a plurality of high density circuit structures combined with a low density PCB in accordance with an embodiment of the present disclosure.

[0028] Figure 1C is a side view of the PCB merged with the high density circuit structures in accordance with an embodiment of the present disclosure.

[0029] Figure 2A is a cross-sectional view of a method of making a high density circuit structure in accordance with an embodiment of the present disclosure.

[0030] Figure 2B is a cross-sectional view of an alternate method of making a high density circuit structure in accordance with an embodiment of the present disclosure.

[0031] Figure 3 illustrates an optional additional layer on the high density electrical circuit of Figure 1 in accordance with an embodiment of the present disclosure.

[0032] Figure 4 illustrates application to a second circuitry layer to the high density electrical circuit of Figure 1 in accordance with an embodiment of the present disclosure.

[0033] Figure 5 illustrates an optional dielectric layer on the high density electrical circuit of Figure 1 in accordance with an embodiment of the present disclosure.

[0034] Figure 6 illustrates an optional etching step on the high density electrical circuit of Figure 1 in accordance with an embodiment of the present disclosure.

[0035] Figure 7 illustrates an electrical interconnect interfaced with a BGA device in accordance with an embodiment of the present disclosure.

[0036] Figure 8 illustrates an electrical interconnect for a flexible circuit in accordance with an embodiment of the present disclosure.

[0037] Figure 9 illustrates an electrical interconnect for an IC package in accordance with an embodiment of the present disclosure.

[0038] Figure 10 illustrates an alternate electrical circuit for an IC package in accordance with an embodiment of the present disclosure.

[0039] Figure 11 is a side sectional view of an electrical circuit in accordance with an embodiment of the present disclosure.

[0040] Figure 12 is a side sectional view of an alternate electrical circuit with printed compliant material in accordance with an embodiment of the present disclosure.

[0041] Figure 13 illustrates an electrical circuit with optical features in accordance with an embodiment of the present disclosure.

[0042] Figure 14 illustrates an alternate high density electrical circuit with optical features in accordance with an embodiment of the present disclosure.

[0043] Figure 15 illustrates an alternate high density circuit structure with printed vias in accordance with an embodiment of the present disclosure.

[0044] Figure 16 illustrates an alternate high density circuit structure with printed electrical devices in accordance with an embodiment of the present disclosure.

[0045] Figure 17 illustrates an alternate high density electrical circuit with printed compliant electrical pads to plug into another connector in accordance with an embodiment of the present disclosure.

[0046] Figure 18 is a top view of a high density electrical circuit in accordance with an embodiment of the present disclosure.

[0047] Figure 19 is a side view of an alternate high density circuit with RF wave guides in accordance with an embodiment of the present disclosure.

[0048] Figure 20 is a side view of various methods of coupling a high density circuit with a low density circuit in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0049] A high density circuit structure according to the present disclosure may permit fine contact-to-contact spacing (pitch) on the order of less than 1.0 mm pitch, and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. Such fine pitch high density circuit structures are especially useful for communications, wireless, and memory devices.

[0050] The present high density circuit structure can be configured as a low cost, high signal performance electrical interconnect assembly, which has a low profile that is particularly useful for desktop and mobile PC applications. IC devices can be installed and uninstalled without the need to reflow solder. The solder-free electrical connection of the IC devices is environmentally friendly. In another embodiment, the high density circuit structure can also be a portion of a socket or semiconductor package.

[0051] Figures 1A and 1B schematically illustrate the merger of a lower density circuit 20 with one or more high density circuits 22A, 22B, 22C, 22D ("22") into the contiguous assembly of Figure 1C. The lower density circuit 20 may be a printed circuit board, a flexible circuit, or the like. The high density circuit 22 can be a printed circuit board, an IC socket, a semiconductor package, or the like.

[0052] Dielectric material 24 is optionally applied to the surface 26 of the low density circuit 20 so the location of the high density circuits 22 is at least partially defined and isolated. The dielectric material 24 may be a film or a liquid dielectric. The dielectric material 24 is imaged to expose the circuit locations 28 for the high density circuits 22, improving alignment of vias on the lower density main core 20 with the high density circuits 22.

[0053] As will be discussed in more detail below, the dielectric 24 is optionally processed to enable electro-less or electrolytic copper plating to adhere to the surface of the dielectric and grow a thick trace or pillar or via structure within the imaged region with undesired areas remaining un-plated or post plate etched to remove unwanted copper. Once the surfaces are plated, a higher deposition rate electroplate copper can be applied to build up the thickness or area of copper as desired.

[0054] If the circuit assembly 30 is a flexible circuit, the base layer can be a material such as polyimide or liquid crystal polymer. If the circuit assembly 30 is a rigid circuit board, the base can be FR4 or one of many high speed laminates or substrates. If the circuit assembly 30 is a semiconductor package, the base can be a material such as FR4, BT resin of any one of a variety of laminate or substrate materials. If the circuit assembly 30 is an electrical connector or socket, the base can be molded LCP, machined plastic, or a variety of films or substrate materials.

[0055] The high density circuits 22 (also referred to as "coupons") can be made using conventional build up technology described above or using the process described below. The high density circuits 22 are then merged with the low density circuit 20. In another embodiment, the high density circuits 22 can be fabricated in-situ directly on the low density circuit 20 using the processes described herein. The present method permits the high density circuits 22 to be formed directly in the circuit locations 28, without having to extend the processing across the entire low density circuit 20.

[0056] Figure 2A is a side cross-sectional view of a method of making the high density electrical circuits 22 in accordance with an embodiment of the present disclosure. The first step is to start with base material of some sort, such as a copper foil 32A or a core 34 of some sort to act as a support member. If the starting base is copper foil 32A, then the foil can act as the first layer circuitry or escape layer which would be the layer to be merged with the circuit locations 28 on the low density circuit 20. In the case where the high density circuit 22 is a semiconductor package, the foil 32A can be the termination points for BGA attachment to the low density circuit 20. The base 34 can also be a sacrificial member that is removed at some point later in the process to reveal the individual coupons 22.

[0057] In the illustrated embodiment, copper foil circuitry layer 32A is located on reinforcing layer 34. The layer 34 can be a traditional PCB or laminated to a stiffening layer or core, such as glass-reinforced epoxy laminate sheets (e.g., FR4). The circuitry layer 32A can be preformed or can be formed using a fine line imaging step is conducted to etch copper foil as done with many PCB processes.

[0058] Liquid dielectric material 36 is applied to surface 38 and flows between the regions of the circuitry 32A. A dry dielectric film, by contrast, does not flow into the recessed regions. The dielectric layer 36 can be tack cured to partially link the polymer and allow for handling, while retaining the ability to image the material in a

photolithography process. Alternatively, the dielectric layer 36 can be processed with a laser direct imaging process known as LDI.

[0059] The dielectric material 36 is typically imaged to create recesses 37 that expose the desired locations 40 on circuitry layer 32A with theoretical via locations 37 created as part of the image directly in proximity to the circuitry layer 32A. One benefit of imaging the dielectric layer 36 is that the via structures do not need to be round as with traditional drilled vias. Any shape that can be imaged and will result in a grown full metal via 54 of the desired shape.

[0060] The dielectric surface 46 can be planarized to create a very consistent dielectric thickness and planarity, as well as assist with preparing select surfaces for electro-less copper plating adhesion. Planarization also permits as many layers to be added to the circuit 22 as needed.

[0061] The dielectric layer 36 is preferably processed to promote electro-less copper plating using one or more of plasma treatment, permanganate, carbon treatment, impregnating copper nano-particles to activate the desired surfaces to promote electroplating. In the illustrated embodiment, the dielectric material 36 is processed to promote plating adhesion to the side walls 44 of the recesses 37. Electro-less copper plating is applied to the side walls 44 of the recesses 37 to create conductive structures 50, resulting in a three-dimensional landscape. Additional discussion of the use of electro-less plating of the dielectric structure is disclosed in PCT/US2012/53848, filed September 6, 2012, entitled DIRECT METALIZATION OF ELECTRICAL CIRCUIT STRUCTURES, the entire of disclosure of which is hereby incorporated by reference.

[0062] A plating resist is applied, imaged and developed to expose the via location 37 and previous circuit layer 32A. In the illustrated embodiment, the conductive structure 50 is an annular-shaped via electrically coupled to the circuitry layer 32A with a center opening or recess 52. Once the surfaces 44 of the dielectric material 36 are plated, a higher deposition rate electroplate copper can be used to fill the recess 52 with conductive material 54 to form a conductive pillar 56. The plating resist is stripped and the copper deposition 50, 54 is optionally planarized. The resulting conductive pillars 56 include a shell 50 of electro-less conductive material and a core 54 of electro-plated conductive material.

[0063] A present process creates the ability to stack full metal vias 54 in subsequent deposition steps to create a high aspect ratio via without the need to drill through the

entire stack 22 in one operation. Another benefit is the ability to provide a mounting point for a packaged semiconductor device where a copper pillars 54 are created as an alternative to conventional via in pad construction which can be plagued with reliability issues and high costs to manufacture.

[0064] In another embodiment, the present process enhances the electroplating process is to deposit electro-less copper or copper flash to provide a bus structure for bulk copper electro plating. The copper bus structure is subsequently removed with a differential etch process that leaves bulk copper 54 intact. An alternate step can be employed to add multiple layers of resist 36 and continue the copper growth procedure if desired, with the resulting structures encapsulated by the next dielectric application.

[0065] The shape of the conductive structures 50, 54 is dictated by the shape of the recesses 37. A square recess 37 results in a square-shaped conductive structure 54. The plating process can be controlled to a certain degree, but in some cases with fine pitch geometries and high speed circuits, upper surfaces 46 of the dielectric 36 and the conductive structure 54 may vary in topography or height relative to the field, and the dielectric material 36 may vary in thickness slightly especially if liquid material is used. Consequently, it is preferred to planarize to surfaces 46 of the conductive structures 54 and the exposed surface 46 of the dielectric 36 between steps to control thickness and flatness of the electrical circuit 22.

[0066] In the illustrated embodiment, additional foil layer 32B is applied and processed to create a circuit structure using any of the techniques discussed herein. The conductive material 54 electrically couples the circuit layer 32A to the circuit layer 32B.

[0067] The present method permits the material between layers and within each layer to be varied. One aspect of the present process that differs from the traditional dry film build up process is the nature of the dielectric deposition in liquid form. The dielectric layer 36 can be applied by screen printing, stencil printing, jetting, flooding, spraying etc. The liquid material 36 flows and fills any recessed regions within a previous circuit landscape 32A. During the development process, desired regions remain and the regions that are not desired are washed away with fine resolution of the transition regions within the landscape. Multiple depositions steps can be tack cured and imaged such that thicker sections of dielectric 36 can be developed and washed away in one or multiple strip operations. As a result, internal cavities or

mass regions can be excavated and subsequently filled at the next dielectric layer with materials that have physical properties differing from the base dielectric 36. In other words, the excavated regions can be filled or treated with materials that have a different dielectric constant, vary in conductive or mechanical or thermal properties to achieve a desired performance function not possible with a contiguous dry film technique. In basic terms, the present process not only provides the ability to alter the material set and associated properties in a given layer, but the material set can be altered at any given point within a given deposition or layer.

[0068] The present process can also be used in combination with existing dry film techniques. For example, one or more of the layers can be a preformed dielectric film to leave air dielectric gaps between traces. Recesses 37 in the dielectric layer 36 that expose circuitry 32A can be formed by printing, embossing, imprinting, laser cutting, chemical etching with a printed mask, or a variety of other techniques.

[0069] Figure 2B illustrates an alternate high density electrical circuit 22 in accordance with an embodiment of the present disclosure. The process is the same as discussed in connection with Figure 2A, except that the sidewalls 44 of the dielectric material 36 are not processed to receive electro-less plating. Rather, a bulk conductive material 42 is applied directly to exposed portions 40 of the circuit layer 32A. The surface 46 is preferably planarized and the circuit layer 32B is applied using any of the techniques disclosed herein.

[0070] Figure 3 illustrates higher aspect ratio conductive pillar 60 formed on the high density electrical circuit 22 without the foil layer 32B. The process discussed above is repeated by applying another layer 62 of dielectric 36 that is imaged to created recesses 64 that expose the upper surface 66 of the copper pillar 42. The upper surfaces 66 of the copper pillars 42 are then plated as discussed above to create conductive extension 68 of the copper pillar 42.

[0071] In one embodiment, the conductive extensions 68 are planarized to permit die attach point 70 to facilitate flip chip attach of the die 72 to the conductive extensions 68 directly. In another embodiment, exposed surfaces 74 of the plating can be enlarged to facilitate soldering of the die 72 to the conductive extensions 68.

[0072] Figure 4 illustrates circuitry layer 80 is applied to the top surface 78 of the electrical circuit 22 and coupled to the conductive extensions 68. The circuitry layer 80 creates the base for additional routing layers and to facilitate vertical connection

to subsequent layers in the stack in accordance with an alternate embodiment of the present disclosure.

[0073] Figure 5 illustrates dielectric layer 90 added to the subsequent circuitry layer 80 in accordance with an alternate embodiment of the present disclosure. The dielectric layer 90 is imaged to create recesses 92 that expose portions 94 of the circuitry layer 80 that corresponds with the via extensions 68. The dielectric layer 90 protects the portions of the circuitry layers 80 that are not to be etched and provides access to the foil intimate to the conductive structures 42 and 68. In one embodiment, the extension 68 is optionally conductive structure 50 with a core 54 of conductive or non-conductive material.

[0074] Figure 6 illustrates a subsequent etch process that removes the copper foil 94 (see Figure 5) located in the recesses 92 to allow access for the next plating step to join the layers together in accordance with an alternate embodiment of the present disclosure.

[0075] Depending on the dielectric material 90 and desired final construction, the resist layer 90 can be stripped to provide a level to be planarized as the base of further processing or the resist layer 90 can be left in place provided it is of the proper material type. The exposed regions that provided access for etch and plating can be filled with similar material to seal the layer which can be planarized for further processing if desired.

[0076] Figure 7 illustrates one possible variation of the electrical circuit 22. Recesses 92 are filled with a dielectric material 96 and the surface 98 is planarized to receive circuitry plane 100. Dielectric layer 102 is deposited on the circuitry plane 100 to expose selective regions 104. The selective regions 104 are configured to correspond to solder balls 120 on BGA device 122. In the illustrated embodiment, bottom dielectric layer 106 is optionally deposited on circuitry layer 52 in a manner to expose selective regions 108.

[0077] In one embodiment, the electrical circuit 22 is further processed with conventional circuit fabrication processes to create larger diameter through vias or through holes plated 110 as needed, solder mask applied and imaged to expose device termination locations 104, 108, laser direct imaging, legend application etc. In another embodiment, the via 110 is formed using electro-less plating of each layer of the stack, as illustrated in Figure 6.

[0078] Figure 8 illustrate an alternate embodiment in which the electrical circuit 22 is used in a flexible circuit applications. The electrical circuit 22 is laminated with ground planes and cover layers 112, 114. In some applications the insulating layers 112, 114 are applied by jet printing of polyimide or liquid crystal polymers (LCP) inks as a final layer or as a combination of laminated film and jetted material.

[0079] Figure 9 illustrates an electrical circuit 22 for semiconductor packaging applications in accordance with an embodiment of the present disclosure. The stack 152 can be final processed with a variety of options to facilitate electrical connections to IC devices 162, 166, 172 and to system level attachment to low density circuit 20.

[0080] In one embodiment, the plating 160 is planarized to facilitate flip chip attach to the structure directly (see e.g., Figure 2) or to receive BGA device 162. In other embodiment, plating 164 is extended to facilitate direct soldering of IC device die 166 with paste. In yet another embodiment, plating 168 is wire bonded 170 to the IC device 172.

[0081] The low density main core 20 can be processed to accept a traditional ball grid array attachment 182 for an area array configuration or plated with solder/tin etc. for a no lead peripheral termination. The low density main core 20 can also be fashioned to have plating or post extensions 184 to facilitate direct solder attach with paste and provide a natural standoff from the low density circuit 20.

[0082] Figure 10 illustrates an electrical circuit 22 for a semiconductor packages 202 with dielectric materials 204 surrounding the conductive structures 206 in accordance with an embodiment of the present disclosure. Internal circuits and terminations may also be added by imaging or drilling the core material with a larger opening than needed and filling those openings with dielectric and imaging the desired geometry to facilitate conductive structure formation.

[0083] Figure 11 illustrates an alternate electrical circuit 230 with an insulating layer 232 applied to the circuit geometry 234. The nature of the liquid dielectric application process allows for selective application of dielectric layer 232 to leave selected portions 236 of the circuit geometry 234 expose if desired. The resulting high density electrical circuit 230 can potentially be considered entirely “green” with limited or no chemistry used to produce beyond the direct write materials.

[0084] The dielectric layers of the present disclosure may be constructed of any of a number of dielectric materials that are currently used to make sockets, semiconductor packaging, and printed circuit boards. Examples may include UV

stabilized tetrafunctional epoxy resin systems referred to as Flame Retardant 4 (FR-4); bismaleimide-triazine thermoset epoxy resins referred to as BT-Epoxy or BT Resin; and liquid crystal polymers (LCPs), which are polyester polymers that are extremely unreactive, inert and resistant to fire. Other suitable plastics include phenolics, polyesters, and Ryton® available from Phillips Petroleum Company.

[0085] In one embodiment, one or more of the dielectric materials are designed to provide electrostatic dissipation or to reduce cross-talk between the traces of the circuit geometry. An efficient way to prevent electrostatic discharge ("ESD") is to construct one of the layers from materials that are not too conductive but that will slowly conduct static charges away. These materials preferably have resistivity values in the range of 10^5 to 10^{11} Ohm-meters.

[0086] Figure 12 illustrates an alternate high density electrical circuit 250 in accordance with an embodiment of the present disclosure. Dielectric layer 252 includes openings 254 into which compliant material 256 is deposited or printed before formation of circuit geometry 258. The compliant material 256 improves reliability during flexure of the electrical circuit 250.

[0087] Figure 13 illustrates an alternate high performance electrical circuit 260 in accordance with an embodiment of the present disclosure. Optical fibers 262 are located between layers 264, 266 of dielectric material. In one embodiment, optical fibers 262 are positioned over compliant layer 268, and dielectric layer 270 is formed over and around the optical fibers 262. A compliant layer 272 is preferably provided above the optical fiber 262 as well. The compliant layers 268, 272 support the optical fibers 262 during flexure. In another embodiment, the dielectric layer 270 is imaged with recesses into which the optical fibers 262 are deposited.

[0088] In another embodiment, optical quality materials 274 are printed during assembly of the high density electrical circuit 260. The optical quality material 274 and/or the optical fibers 262 comprise optical circuit geometries. The printing process allows for deposition of coatings in-situ that enhances the optical transmission or reduces loss. The precision of the printing process reduces misalignment issues when the optical materials 274 are optically coupled with another optical structure.

[0089] Figure 14 illustrates another embodiment of a present high density electrical circuit 280 in accordance with an embodiment of the present disclosure. Embedded coaxial RF circuits 282 or printed micro strip RF circuits 284 are located within the

dielectric layers 286. These RF circuits 282, 284 are preferably created by printing dielectrics and metallization geometry.

[0090] As illustrated in Figure 15, use of the present process allows the creation of a high density electrical circuit 290 with inter-circuit, 3D lattice structures 292 having intricate routing schemes. Conductive pillars 294 can be plated with each layer, without drilling.

[0091] The nature of the present process permit controlled application of dielectric layers 296 creates recesses 298 that control the location, cross section, material content, and aspect ratio of the conductive traces 292 and the conductive pillars 294. Maintaining the conductive traces 292 and conductive pillars 294 with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications.

[0092] Using the imaged recesses 298 to control the aspect ratio of the conductive traces 292 and the conductive pillars 294 results in a more rectangular or square cross-section, with the corresponding improvement in signal integrity. The recesses 298 are preferably processed to receive electro-less plating, followed by electroplating to build up the conductive traces 292.

[0093] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces are transferred to the recesses 298. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses 298. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses 298 not occupied by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses 298.

[0094] In another embodiment, a thin conductive foil is pressed into the recesses 298, and the edges of the recesses 298 acts to cut or shear the conductive foil. The process locates a portion of the conductive foil in the recesses 298, but leaves the negative pattern of the conductive foil not wanted outside and above the recesses 298 for easy removal. Again, the foil in the recesses 298 is preferably post plated to

add material to increase the thickness of the conductive traces 292 in the circuit geometry and to fill any voids left between the conductive foil and the recesses 298.

[0095] Figure 16 illustrates a high density electrical circuit 300 with printed electrical devices 302. The electrical devices 302 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like. In the illustrated embodiment, electrical devices 302 include printed LED indicator 304 and display electronics 306. Geometries can also be printed to provide capacitive coupling 308. Compliant material can be added between circuit geometry, such as discussed above, so the present electrical circuit can be plugged into a receptacle or socket, supplementing or replacing the need for compliance within the connector.

[0096] The electrical devices 302 are preferably printed during construction of the circuit assembly 300. The electrical devices 302 can be ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. For example, the electrical devices 302 can be formed using printing technology, adding intelligence to the high performance electrical circuit 300. Features that are typically located on other circuit members can be incorporated into the circuit 300 in accordance with an embodiment of the present disclosure.

[0097] The availability of printable silicon inks provides the ability to print electrical devices 302, such as disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. In particular, U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated by reference, teach using ink-jet printing to make various electrical devices, such as, resistors, capacitors, diodes, inductors (or elements which may be used in radio

applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistor (including, light emitting, light sensing or solar cell elements, field effect transistor, top gate structures), and the like.

[0098] The electrical devices 302 can also be created by aerosol printing, such as disclosed in U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference.

[0099] Printing processes are preferably used to fabricate various functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[00100] Ink jet printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semi conductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[00101] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or Teflon.

[00102] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[00103] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from DuPont located in Wilmington, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[00104] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[00105] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic /organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[00106] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108

(December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181, which is incorporated herein by reference.

[00107] A protective layer can optionally be printed onto the electrical devices. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[00108] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present disclosure.

[00109] The ink-jet print head preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[00110] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[00111] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electro pneumatic, electrostatic, rapid ink heating, magneto hydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[00112] While ink jet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: pre-metered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll

coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; and other similar techniques.

[00113] Figure 17 illustrates an alternate high density electrical circuit 320 with compliant material 322 added between circuit geometries 324, 326 to facilitate insertion of circuit geometries 328, 330 into a receptacle or socket. The compliant material 322 can supplement or replace the compliance in the receptacle or socket. In one embodiment, the compliance is provided by a combination of the compliant material 322 and the exposed circuit geometries 328, 330.

[00114] Figure 18 illustrates the unique nature of the present high density circuit construction, where the various circuits and via locations are surrounded by the deposited dielectric within a single layer, rather than layer by layer differential in dielectric or laminate material as seen with conventional methods. In this example, lower level circuit structures 352, 356 are visible through an optically transparent metalized dielectric. Metalized dielectric 350 and printed dielectric 358 can exist in the same layers. Optically imaged via structures 354 span multiple layers.

[00115] Figure 19 illustrates a high density circuit 400 with optical waveguides in accordance with an embodiment of the present disclosure. Metalized channels 402, 404 can function as RF waveguides, embedded antennae, embedded microstrip, and the like. The channels 402, 404 can be metalized using the electro-less plating discussed herein. In one embodiment, the channels 402, 404 in the dielectric 406 are filled with optical transmission material. The channels 402, 404 can optionally be sealed or encapsulated by subsequent dielectric layers.

[00116] In another embodiment, the channel 404 includes optional directional mirror 408 to direct the light with low loss in the X and Y planes in ways that are not possible to bend glass fiber. In the illustrated embodiment, the mirror 408 creates an Z-axis optical via 410.

[00117] In yet another embodiment, metal circuits 412, 414 are created at the top and bottom of the channel 402, and/or on the side walls 416 of the channel 402. The channel 402 is preferably filled with the appropriate optical material 418. The combined or hybrid channel 402 can act as an optical waveguide through the optical material, with an RF signal passing through the optical material of a given dielectric constant guided by the Metalized surfaces 412, 414. The photonic source can be

external to the high density circuit 400 or embedded within the circuit 400 and activated by the appropriate metal circuitry. Figure 20 illustrates an embodiment for merging a high density circuit 22 with a low density circuit 20 in accordance with an embodiment of the present disclosure. Assuming the high density circuit is created as a discrete structure separate from the low density circuit 20, various methods can be used to merge the two circuit structures 20, 22. For example, Figure 20 illustrates various termination points that can be formed on the high density coupon 22 and/or the low density board 20.

[00118] In the left hand side of Figure 20, copper pillar 430 is plated up to correspond to a through hole 432 in the mating circuit such that the post 430 resides inside the hole 432. The hole 432 is slightly larger than the post 430 for alignment purposes and the two 430, 432 are plated together. The center left version shows a post 434 with a tapered top 436 that is essentially a friction or slight deformation fit to mechanically join with the recess 438. The center right shows a through hole 440 and a corresponding pad or trace 442 that align with the hole 440. The two features 440, 442 are preferably plated together. The right hand shows a stud bump or plated bump 444 that is configured to pierce the circuit layer 446. Each of these types of interfaces can be on the high density coupon 22, or on the low density circuit 20 or a mixture of both locations as well as a mixture of types within the same construction. In practice, the interconnect points are typically buried by the final solder mask and reinforced mechanically, or they may reside directly under the high density coupon 22 in some cases.

[00119] An alternate method is to mimic the traditional build up process, a portion of the final copper layer on the low density base board 20 is designed and structured to act as the first circuit layer 32A for the high density circuit 22 (see Figure 2A). The high density circuit 22 is then constructed directly on the low density circuit 20 at that location as described herein. Once the high density circuit 22 is processed and terminate in a manner desired to facilitate subsequent component mounting to the high density circuit 22, a final solder mask is applied to fully encapsulate the high density regions 22 and leave desired high density terminals flush with the final solder mask. The resulting hybrid structure 30 appears to resemble a board that was built entirely with the low density process, but actually contains the high density regions deposited and grown in place with underlying circuit structures encapsulated and reinforced with the final solder mask layer.

[00120] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the disclosure. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the disclosure, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the present disclosure.

[00121] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[00122] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the present disclosure is not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[00123] Other embodiments of the disclosure are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the disclosure, but as merely providing illustrations of some of the presently preferred embodiments of this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the disclosure. Thus, it is intended

that the scope of the present disclosure herein disclosed should not be limited by the particular disclosed embodiments described above.

[00124] Thus the scope of this disclosure should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present disclosure fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present disclosure is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean “one and only one” unless explicitly so stated, but rather “one or more.” All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present disclosure, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A high density region for a low density circuit comprising:

at least a first liquid dielectric layer deposited on the first surface of a first circuitry layer imaged to create a plurality of first recesses;

surfaces of the first recesses plated electro-lessly with a conductive material comprising a first conductive structure electrically coupled to, and extending generally perpendicular to, the first circuitry layer;

a conductive material electro-plated to the first conductive structure to substantially fill the first recesses;

at least a second liquid dielectric layer deposited on the first dielectric layer to include a plurality of second recesses imaged to generally align with a plurality of the first conductive structures;

surfaces of the second recesses plated electro-lessly with a conductive material comprising second conductive structures electrically coupled to, and extending generally perpendicular to, the first conductive structures; and

a conductive material electro-plated to the second conductive structures to substantially fill the second recesses.

2. The high density region for a low density circuit of claim 1 comprising an IC device electrically coupled to the plating in a plurality of the second recesses.

3. The high density region for a low density circuit of claim 1 comprising:

a second circuitry layer located on the second dielectric layer and electrically coupled with a plurality of the second conductive structures; and

at least a third dielectric layer deposited on the second dielectric layer imaged to include a plurality of third recesses generally aligned with a plurality of the second conductive structures.

4. The high density region for a low density circuit of claim 3 wherein portions of the second circuitry layer located in the third recesses is etched away to expose a plurality of the second conductive structures.

5. The high density region for a low density circuit of claim 3 comprising:

a conductive material plated on surfaces of a plurality of the third recesses comprising a third conductive structure electrically coupled to, and extending parallel to the second conductive structures;

a conductive material electro-plated to the third conductive structures to substantially fill the third recesses; and

an IC device including a plurality of contact pads electrically coupled to a plurality of the third conductive structures, wherein the IC device is electrically coupled by one of a flip chip attachment directly to a plurality of third conductive structures, solder balls, or wire bonding.

6. The high density region for a low density circuit of claim 3 comprising:

a third circuitry layer located on the third dielectric layer; and

a covering layer extending across the third circuitry layer, the covering layer comprising a plurality of openings exposing contact pads on the third circuitry layer configured to electrically couple with an IC device.

7. The high density region for a low density circuit of claim 1 wherein the high density circuit is constructed on the low density circuit. .

8. The high density region for a low density circuit of claim 1 wherein the first circuitry layer is formed on the low density circuit and the high density circuit is formed on the first circuitry layer. .

9. The high density region of a low density circuit of claim 1 wherein the high density printed circuit board comprises a discrete structure configured to electrically couple with the low density circuit.

10. A method of making a high density circuit for a low density circuit comprising the steps of:

depositing at least a first liquid dielectric layer on the first surface of a first circuitry layer to include a plurality of first recesses;

processing selected surfaces of the first recesses to accept electro-less conductive plating deposition;

depositing conductive plating electro-lessly on the selected surfaces of the first recesses comprising a plurality of first conductive structures electrically coupled to, and extending generally perpendicular to, the first circuitry layer;

applying a plating resist to the high density circuit;

substantially filling the first recesses with a conductive material using electro-deposit plating; and

removing the plating resist.

11. The method of claim 10 comprising the steps of:

depositing at least a second liquid dielectric layer on the first dielectric layer to include a plurality of second recesses generally aligned with a plurality of the first conductive structures;

processing selected surfaces of the second recesses to accept electro-less conductive plating deposition;

depositing a conductive material electro-lessly on the selected surfaces of the second recesses comprising a plurality of second conductive structures electrically coupled to, and extending generally perpendicular to, the first conductive structures;

applying a plating resist to the high density circuit;

substantially filling the second recesses with a conductive material using electro-deposit plating; and

removing the plating resist.

12. The method of claim 11 comprising planarizing the first dielectric layer and the first conductive structures before depositing the second dielectric layer.

13. The method of claim 11 comprising electrically coupling contact pads on an IC device to a plurality of the second conductive structures.

14. The method of claim 11 comprising the steps of:

locating a second circuitry layer on the second dielectric layer to electrically couple the second circuitry layer with a plurality of the second conductive structures; and

depositing a third dielectric layer on the second dielectric layer to include a plurality of third recesses generally aligned with a plurality of the second conductive structures.

15. The method of claim 14 comprising etching away portions of the second circuitry layer located in the third recesses to expose a plurality of the second conductive structures.

16. The method of claim 15 comprising the steps of:

plating a conductive material on surfaces of a plurality of the third recesses comprising a plurality of third conductive structure electrically coupled to, and extending parallel to the second conductive structures; and

electrically coupling contact pads on an IC device to a plurality of the third conductive structures, wherein the step of electrically coupling comprises one of a flip chip attachment directly to a plurality of third conductive structures, solder balls, or wire bonding.

17. The method of claim 10 comprising constructing the high density circuit directly on the low density circuit or as a discrete structure.

18. The method of claim 10 comprising the steps of:

forming the first circuitry layer on the low density circuit; and

constructing the high density circuit directly on the low density circuit.

19. The method of claim 10 comprising depositing a dielectric material in one or more of the recesses to surround one or more of the conductive structures.

20. The method of claim 10 comprising printing at least one electrical device on one of the dielectric layers and electrically coupling the electrical device to at least a portion of the circuitry layers.

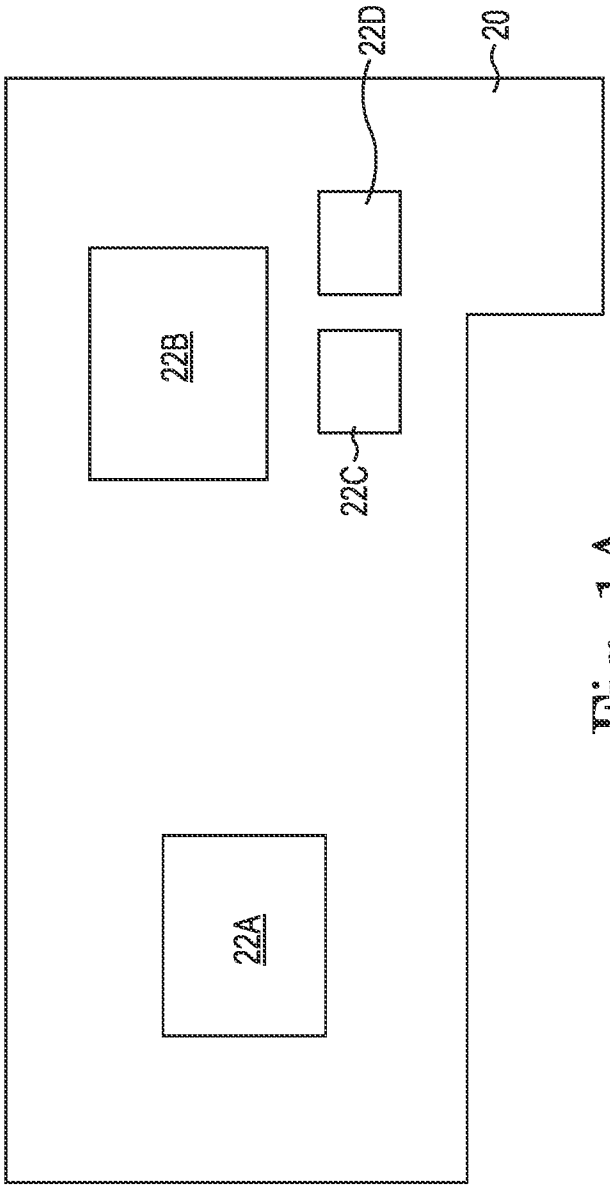


Fig. 1A

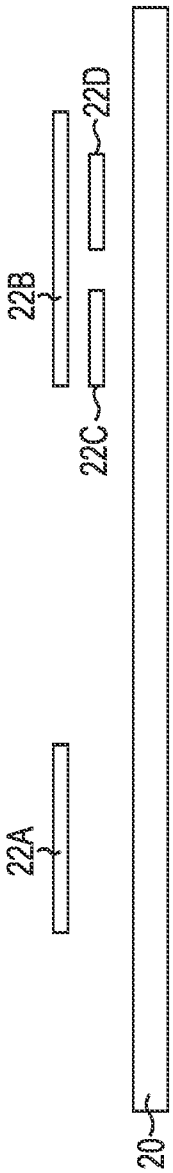


Fig. 1B

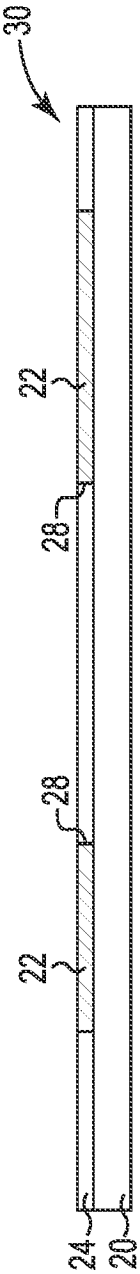


Fig. 1C

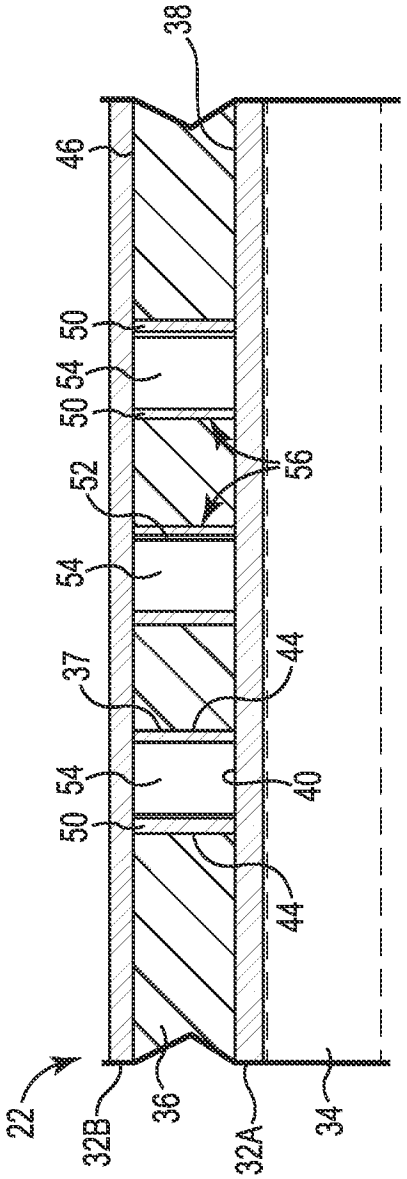

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Fig. 2A

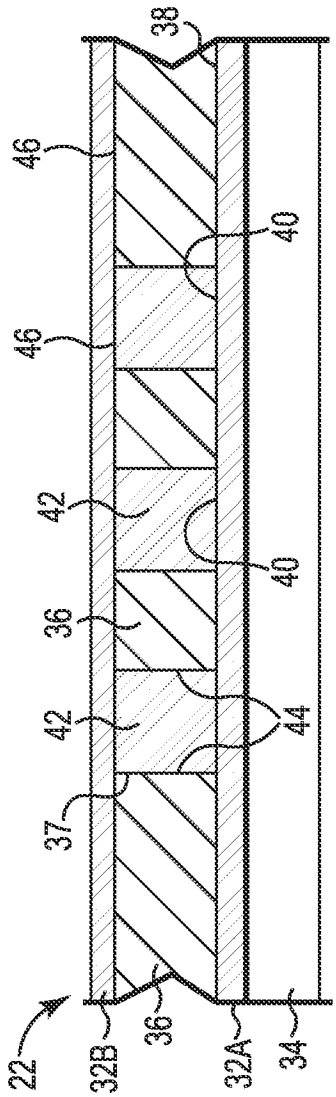

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Fig. 2B

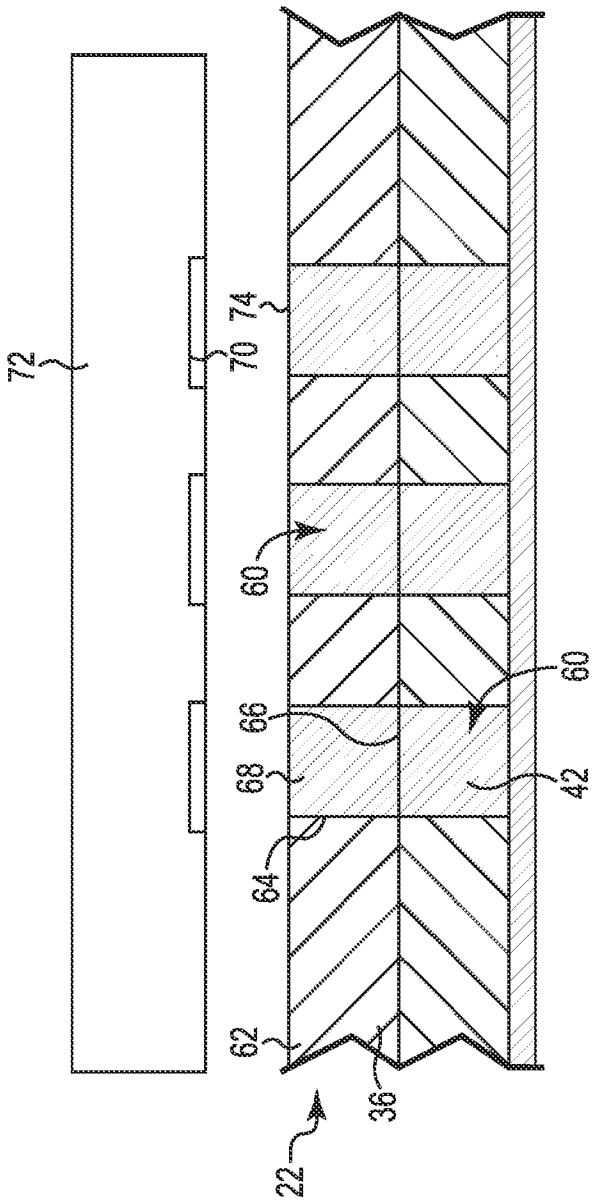


Fig. 3

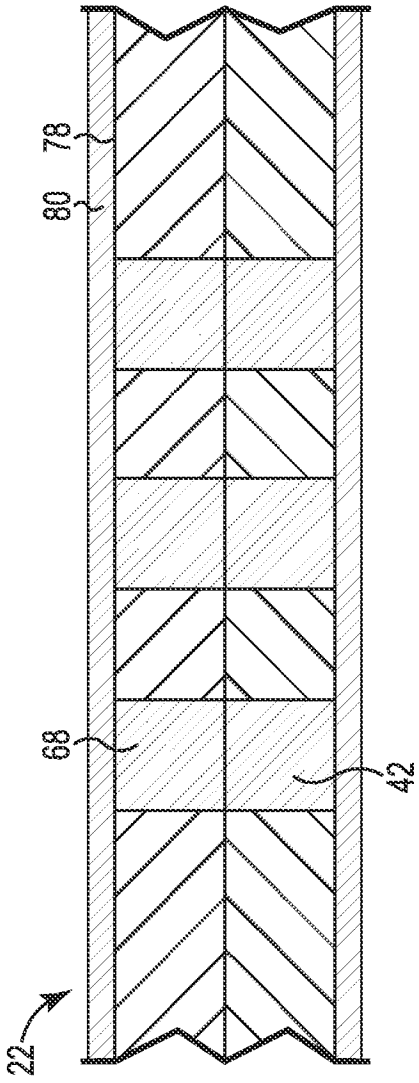


Fig. 4

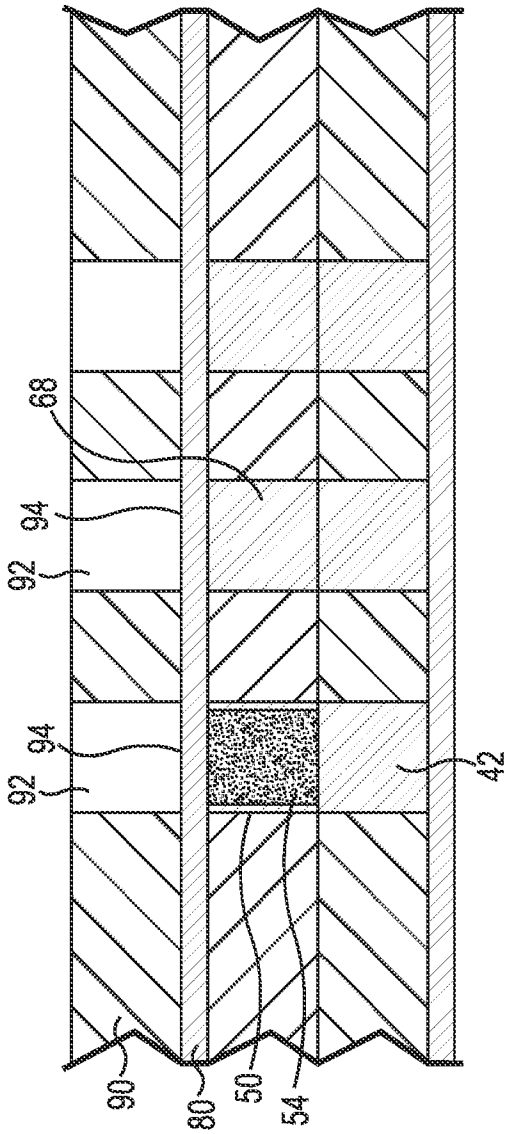


Fig. 5

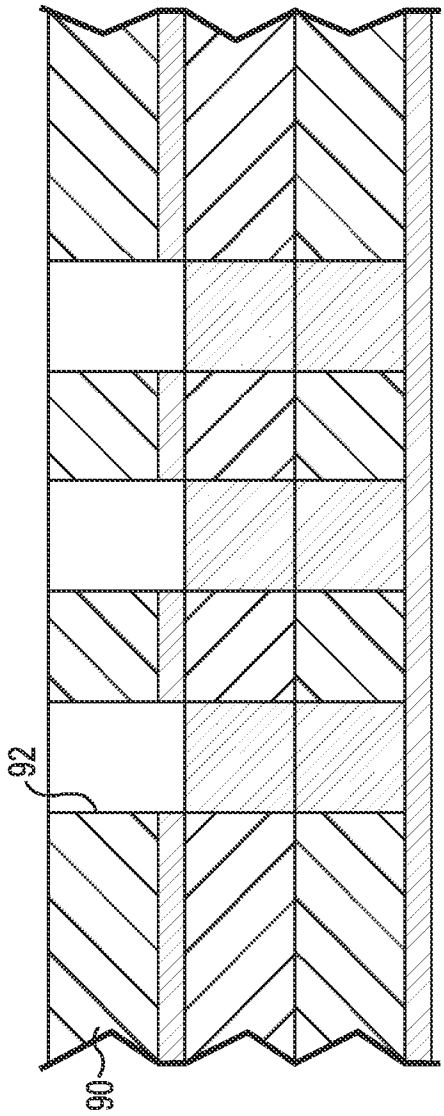


Fig. 6

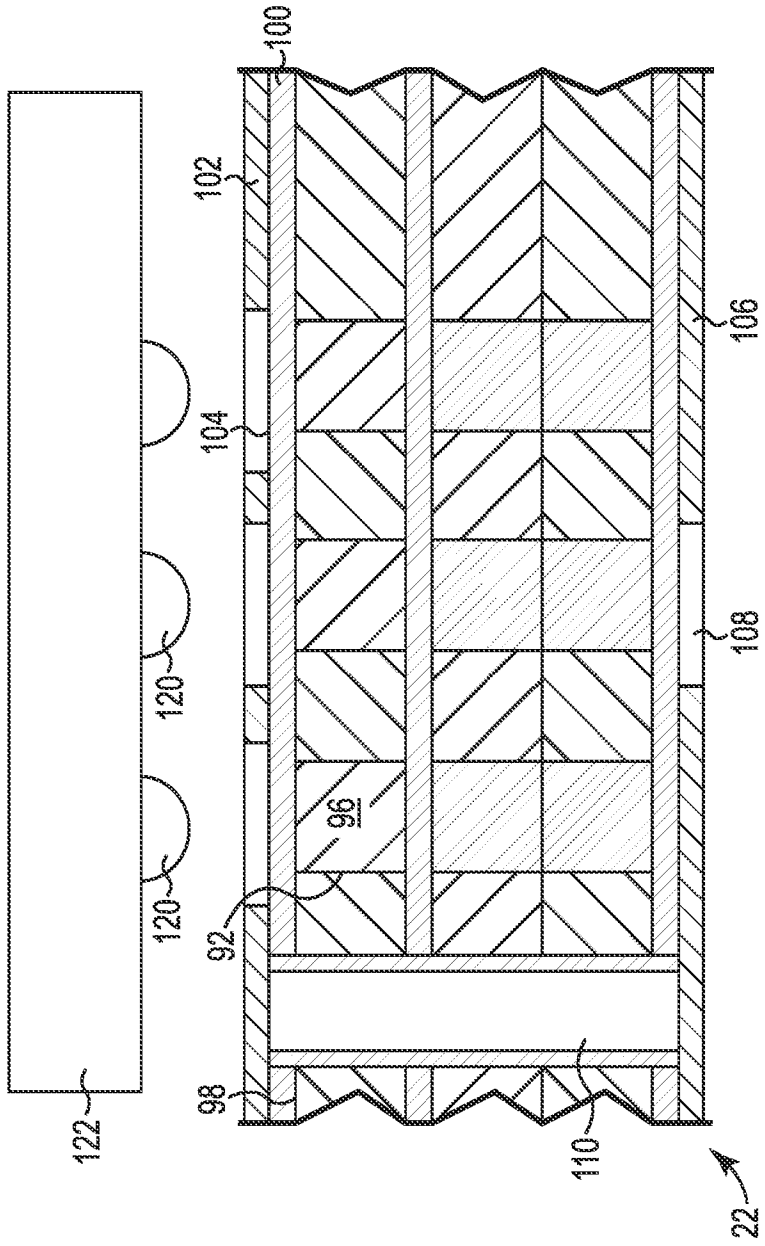


Fig. 7

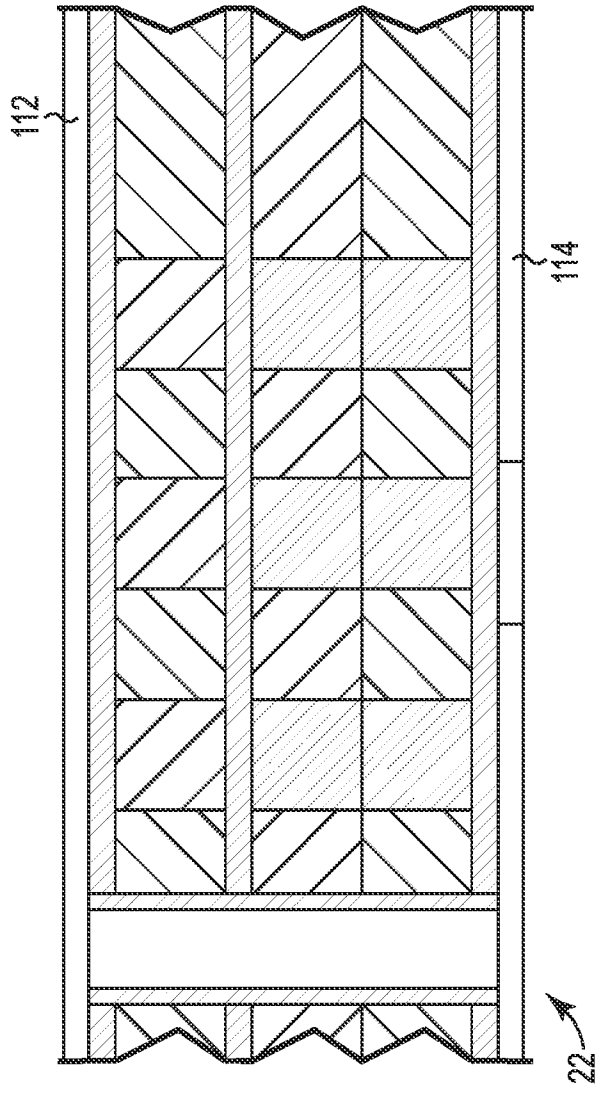


Fig. 8

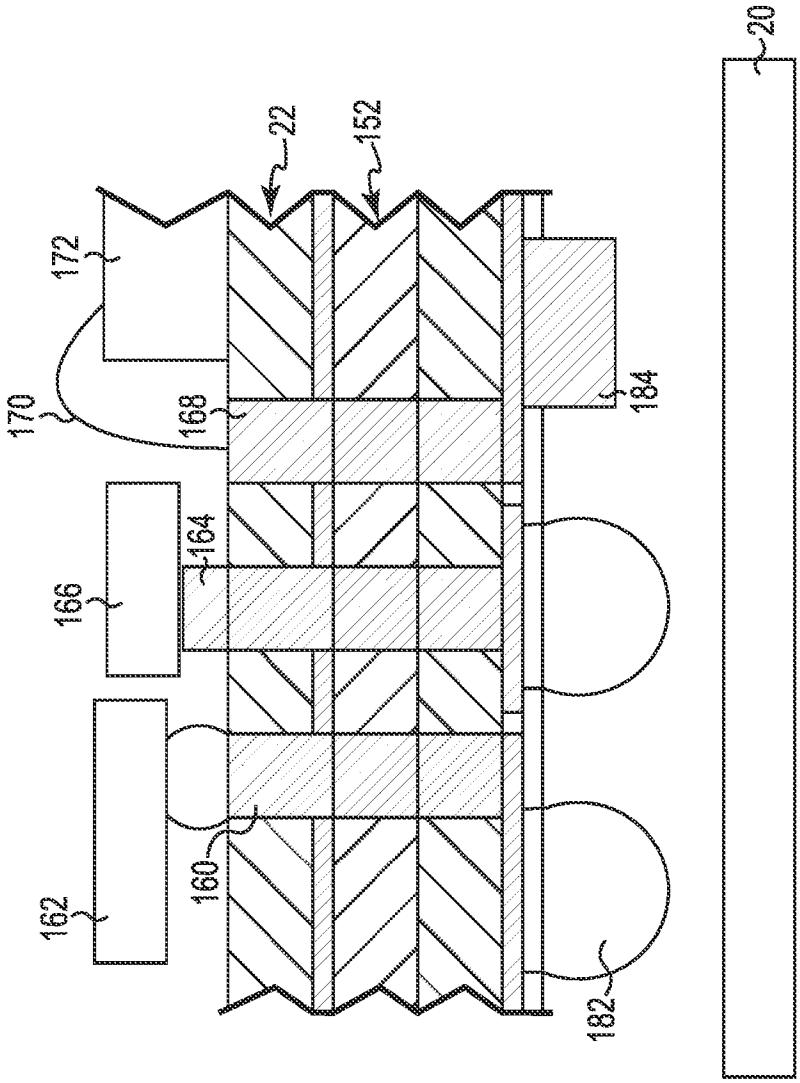


Fig. 9

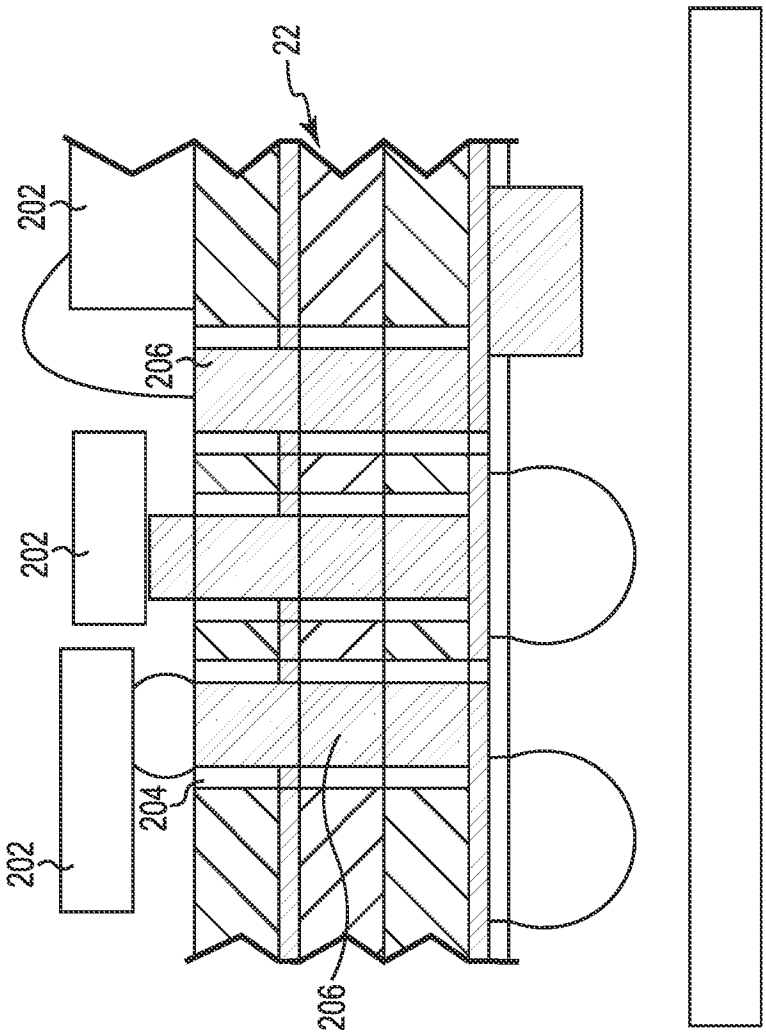


Fig. 10

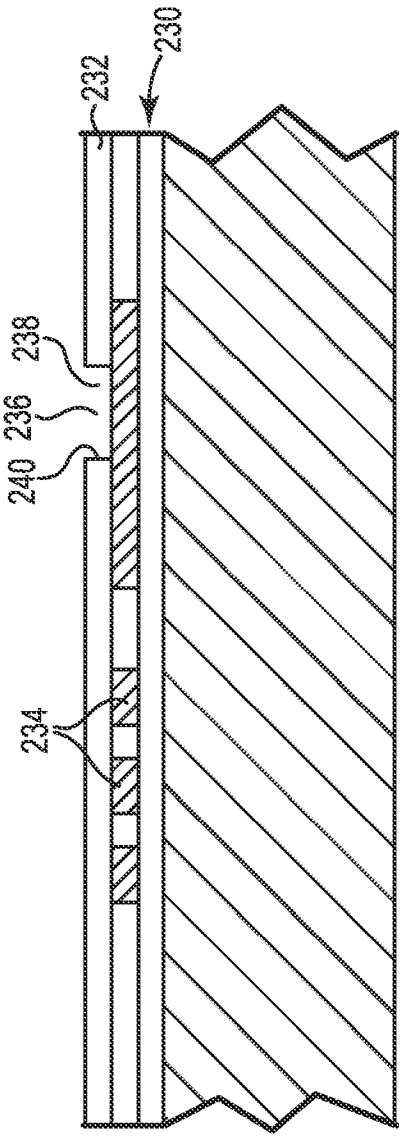


Fig. 11

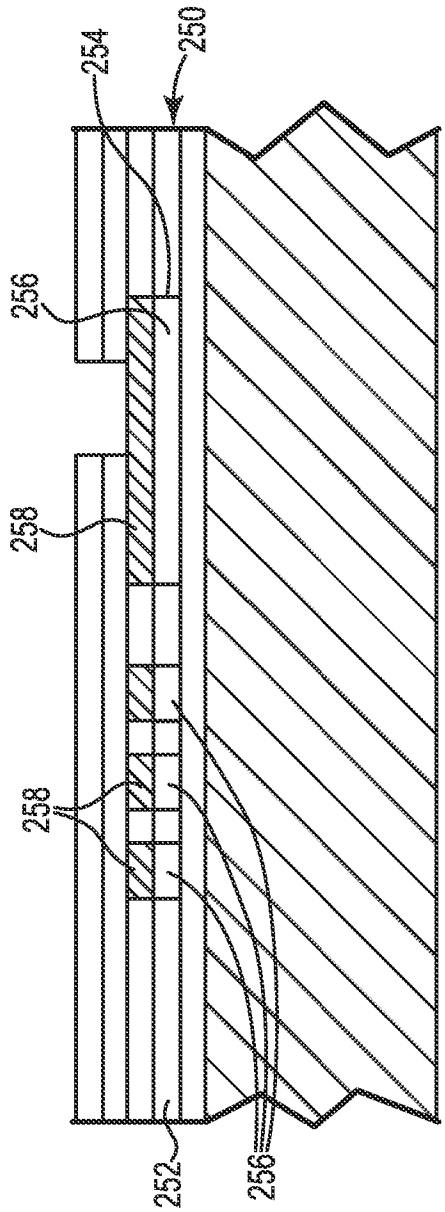


Fig. 12

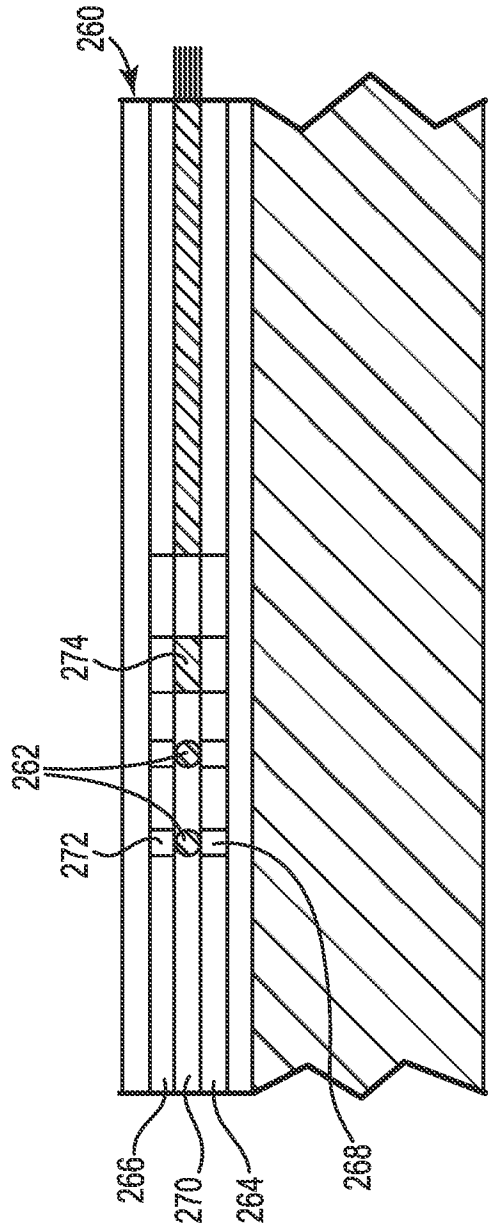


Fig. 13

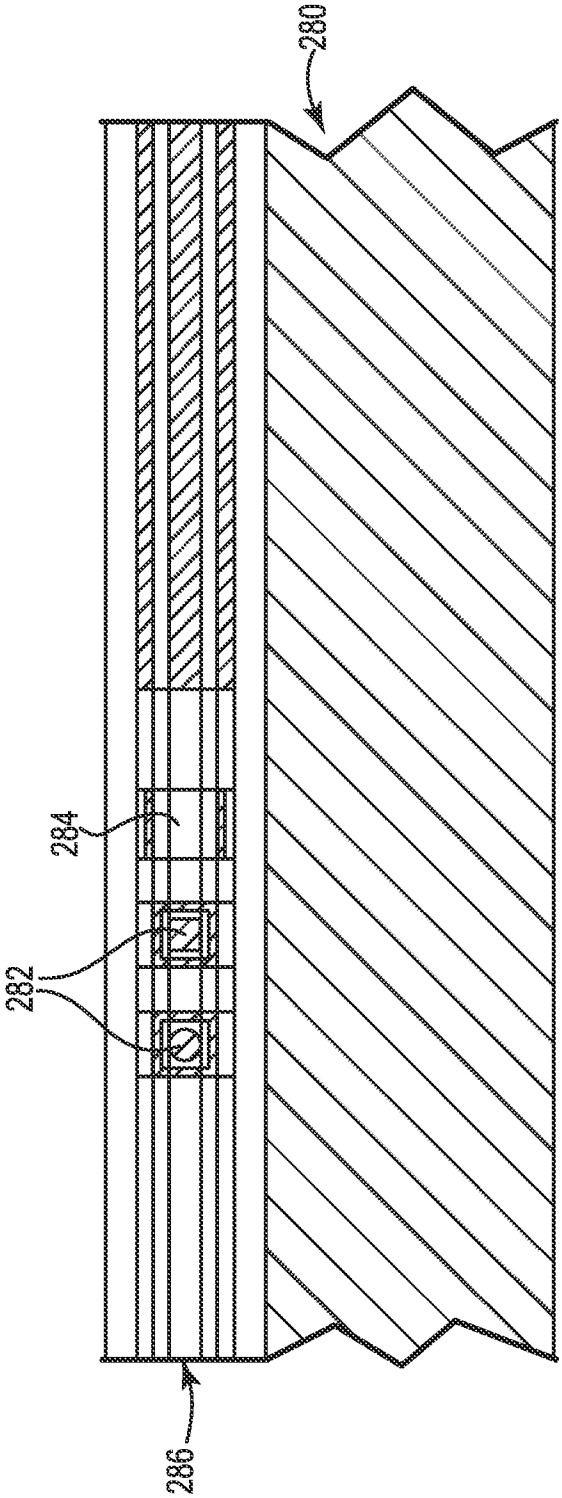


Fig. 14

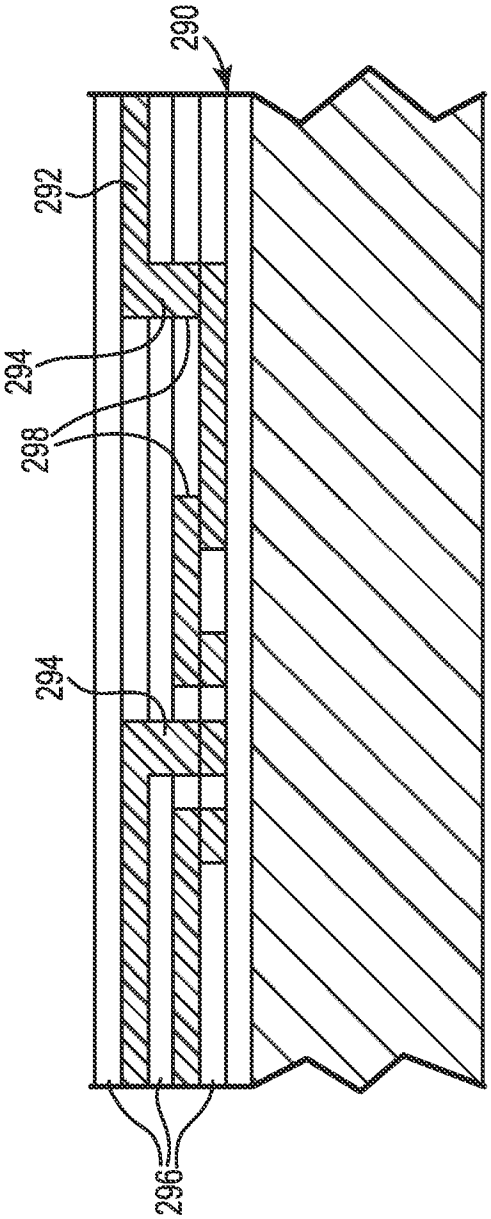


Fig. 15

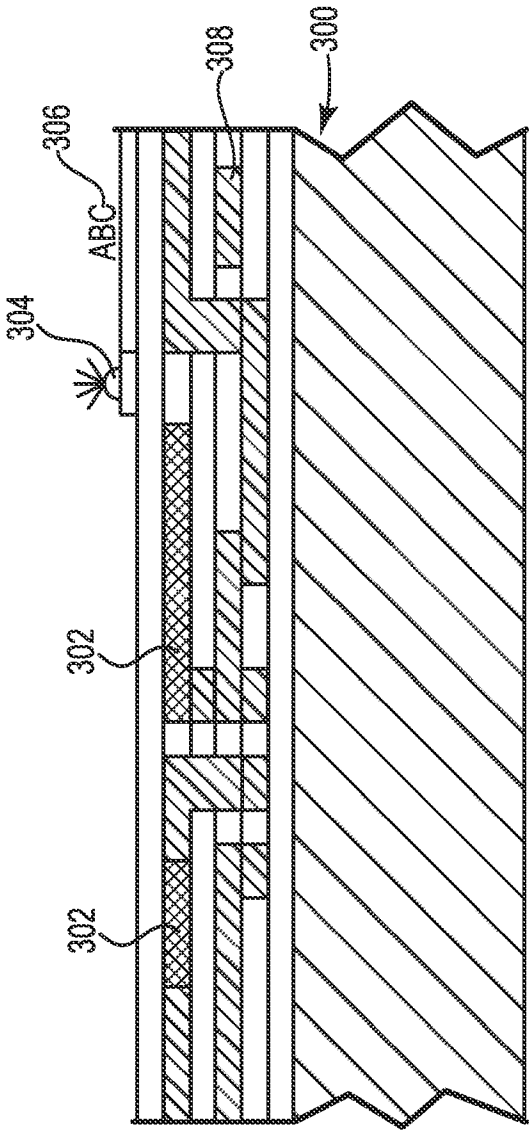


Fig. 16

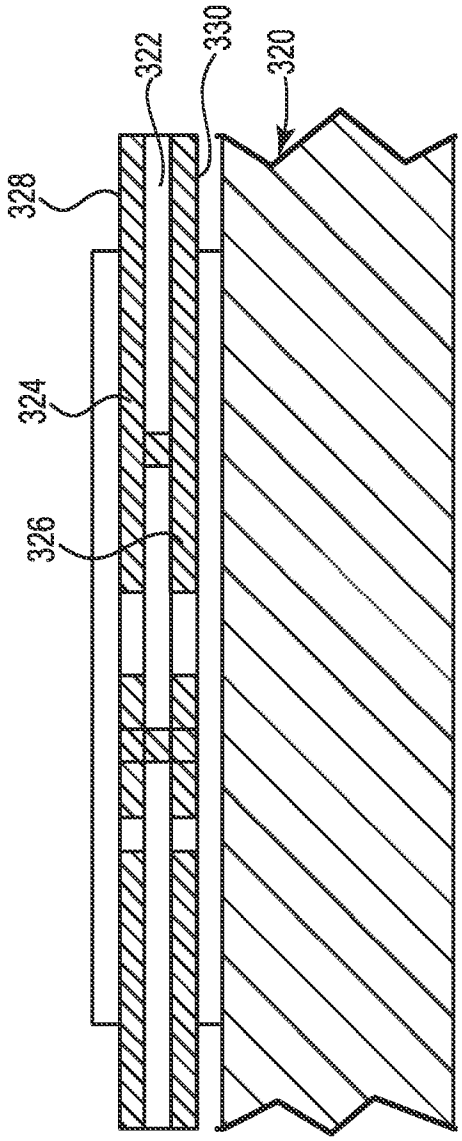


Fig. 17

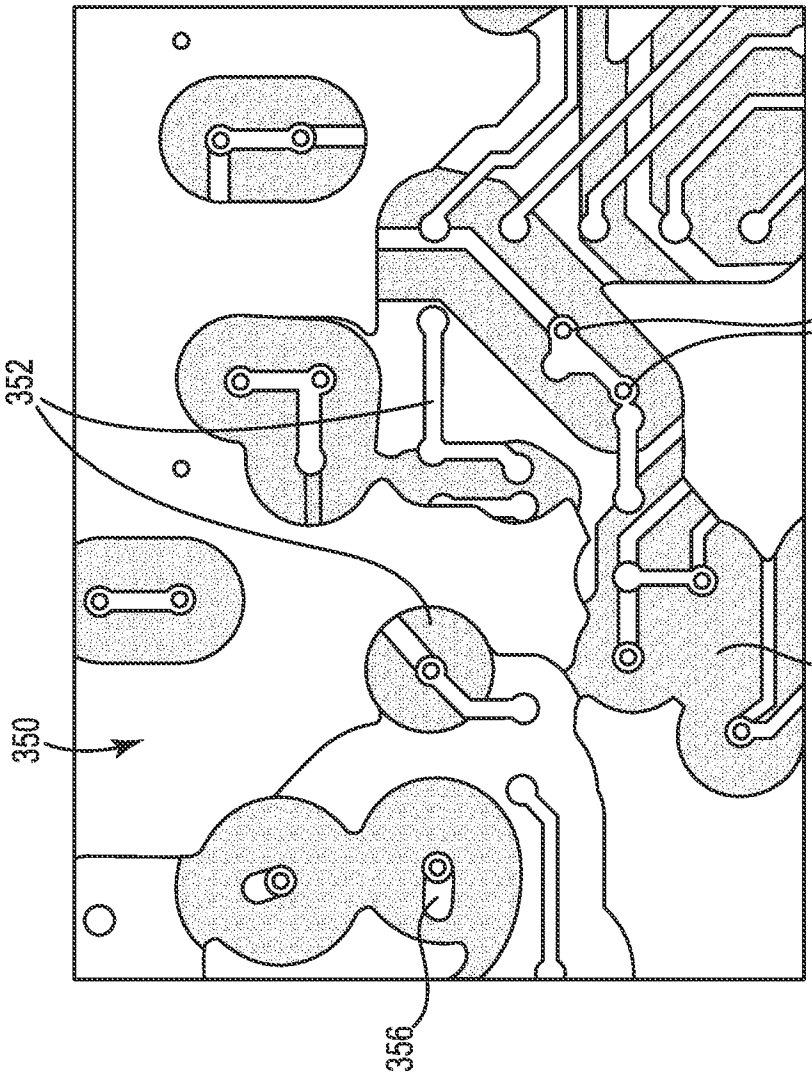


Fig. 18

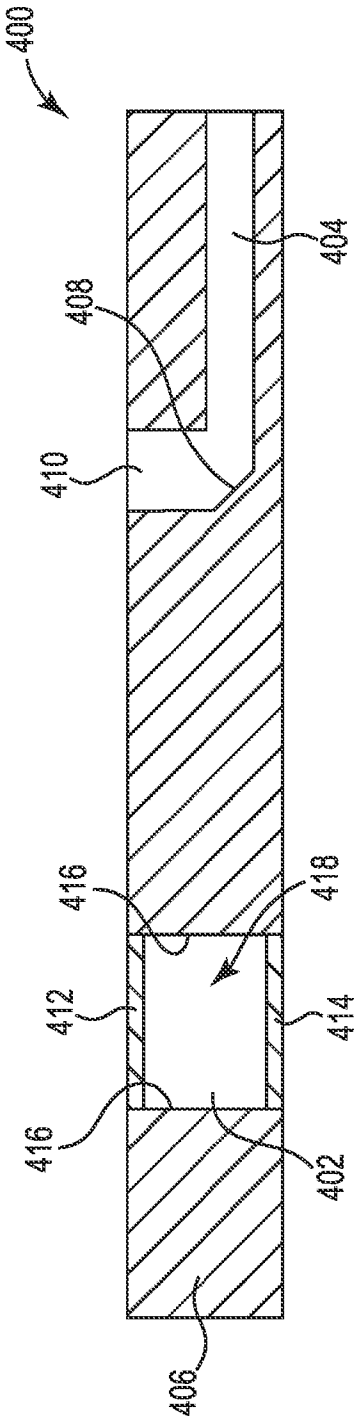

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Fig. 19

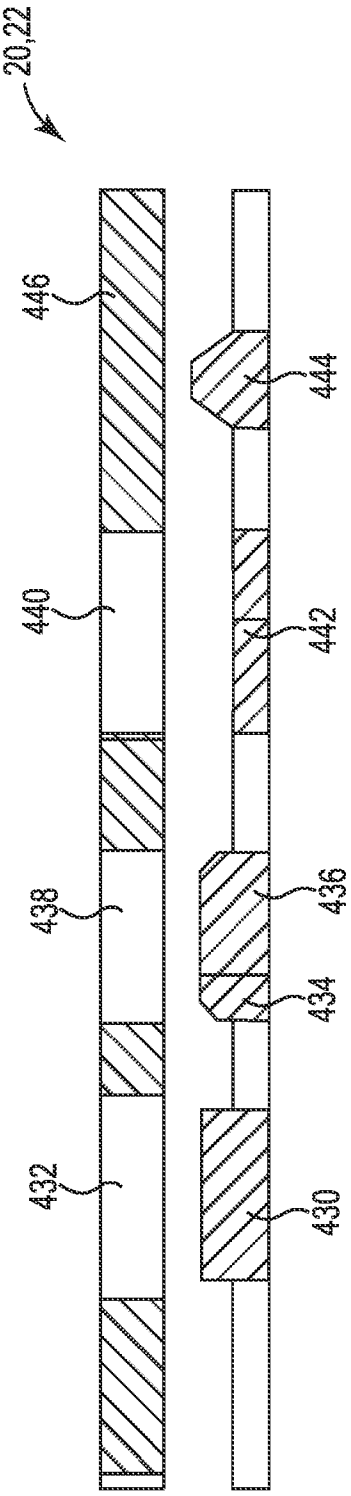

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Fig. 20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 13/30856

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H05K 1/18 (2013.01)
USPC - 257/777; 361/762
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 257/777; 361/762

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8): H05K 1/18 (2013.01); USPC: 257/692,773,774,777,778; 438/108,107, 109; 361/761,762,764,765
(keyword limited; terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase; PubWEST(USPT,PGPB,EPAB,JPAB); Google Scholar
Search Terms: density, high, low, liquid, dielectric, contact, pad, plated, IC, flexible, circuit, making, manufacturing, flip chip

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,454,161 A (BEILIN et al.) 03 October 1995 (03.10.1995), entire document, especially; FIG 1-13, col 1, ln 7-10, col 5, ln 45 to col 6, ln 47, col 7, ln 5-30, col 8, ln 10-31, col 10, ln 62 to col 11, ln 21, col 11, ln 29 to col 12, ln 12, col 13, ln 31-46.	1-20
Y	US 2008/0248596 A1 (DAS et al.) 09 October 2008 (09.10.2008), entire document, especially; para [0001], [0084].	1-20
A	US 5,527,998 A (ANDERSON et al.) 18 June 1996 (18.06.1996), entire document.	1-20
A	US 5,419,038 A (WANG et al.) 30 May 1995 (30.05.1995), entire document.	1-20
A	US 6,320,256 B1 (HO) 20 November 2001 (20.11.2001), entire document.	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 May 2013 (10.05.2013)	07 JUN 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)