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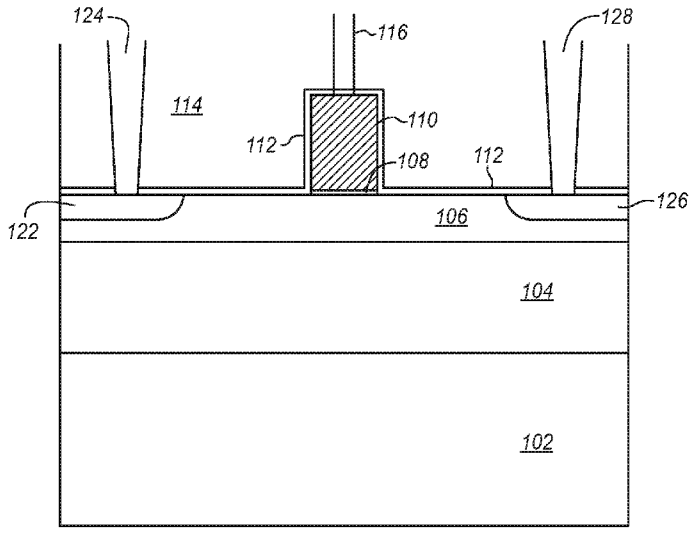
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(54) Title: SUBFIN LINER FOR FINFET DEVICES

FIG. 1



(57) Abstract: A subfin liner is described for use with FinFET devices. In one example, a FinFET device includes a semiconductor substrate having a front side surface, a fin extending from the front side surface, a node of the fin applied over the fin, a dielectric liner over the node, and inter-layer dielectric over the front side surface and the node.

WO 2018/125191 A1

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SUBFIN LINER FOR FINFET DEVICES

FIELD

The present description relates to the field of FinFET device fabrication for integrated circuit dies and, in particular to a device with a liner over the source and drain.

BACKGROUND

Fin Field Effect Transistors (FinFETs) present improvements over complementary metal oxide semiconductor (CMOS) transistors for use in semiconductor chips. CMOS transistors normally have a source, drain, and channel all formed on a flat silicon substrate. FinFETs have the source, drain, and channel formed in a long rib of semiconductor material, referred to as the fin, which extends upward from the semiconductor substrate. A raised source and drain are formed over the fin at each and of a region of the fin that becomes the channel. A gate is then formed over and around the channel between the source and drain.

In operation, the gate is turned on to put the channel in a highly conductive state that allows electrons or holes to easily move through the fin from source to drain. The FinFET reduces leakage current from the channel into the substrate that is a problem with planar CMOS transistors. The FinFET also has less leakage between the source and drain in the off state. This is all done in a device that can be made smaller.

In FinFET diodes and transistors, there is great interest in germanium and silicon germanium fins. The fin is isolated with a shallow trench isolation layer on either side and doped to form appropriate wells for the device. Attachment is made through gates that are formed by a gate oxide over the fin and a gate metal over the oxide. When silicon dioxide or silica (SiO_2) is the gate oxide, then existing CMOS technologies may be used to build up all the layers and connections that go over the gate oxide. The proven existing technologies allow for easy fast development and high yields with existing production tools and materials.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a simplified gate cut cross-sectional side view diagram of a FinFET transistor with a liner according to an embodiment.

Figures 2, 3, and 4 show a Ge/SiGe fin suitable for constructing a transistor according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figures 5, 6, and 7 show a Ge/SiGe fin with an added gate oxide and gate metal according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figures 8, 9, and 10 show a Ge/SiGe fin with excess gate oxide removed according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figures 11, 12, and 13 show a Ge/SiGe fin with spacers and raised source and drain according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figures 14, 15, and 16 show a Ge/SiGe fin with recessed shallow trench isolation according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figures 17, 18, and 19 show a Ge/SiGe fin with a liner over the source, drain and gate according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figures 20, 21, and 22 show a Ge/SiGe fin with a dielectric over the liner according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figures 23, 24, and 25 show a Ge/SiGe fin with contacts through the dielectric and through the liner according to an embodiment in a fin cut under the source, a gate cut and a fin cut under the gate, respectively.

Figure 26 is a block diagram of a computing device incorporating a die with FinFET devices using a liner according to an embodiment.

DETAILED DESCRIPTION

A germanium (Ge) transistor in a FinFET device offers distinct benefits for some applications especially when structured with a SiGe subfin. When SiO_2 is used as a gate oxide, however, both SiGe and Ge show a poor interface to SiO_2-based oxides. Accordingly, there are many different interface states at these interfaces. The different states provide a conduction path and which then contributes to leakage through the gate when the transistor is in an off-state.

This off-state leakage increases power consumption and increases the heat generated by the transistor as the leakage current is dissipated. In addition, the off-state leakage diminishes the difference between the on and the off state. This reduces the transistors effectiveness for many different circuit applications.

As described herein a liner is formed between the SiGe or Ge and SiO_2 interface. The liner may be applied over a SiGe subfin. The liner improves the interface and reduces the off-

state leakage. By using a liner with a good interface with Ge in between the Ge and the ILD (Inter-Layer Dielectric), a conventional ILD, such as SiO_2 may be used with improved current leakage.

As described below the liner may be applied after a dummy gate has been formed or after a subtractive gate has been formed in a FinFET transistor structure. The liner may also be formed after an RSD (Raised Source and Drain) has been formed. The liner remains in place and is not removed. In addition, by placing the liner over a dummy gate or subtractive gate, the liner does not affect the channels of the transistor.

Figure 1 is a simplified gate cut cross-sectional side view diagram of a FinFET transistor with a liner. The structure is built over a silicon substrate 102. A SiGe fin 104 is formed over the substrate. The substrate typically is referred to as having a front side and a back side. The active components are formed on the front side and the back side provides structure and, in some cases, a mounting surface. The fin extends from the front side and is shown in a transverse view extending across the page. An additional Ge fin layer is formed over the SiGe portion of the fin for source, drain, or another structure. A gate oxide 108 of e.g. SiO_2 is then deposited over the Ge.

A gate electrode 110 e.g. TiN or polysilicon is formed over the gate oxide. With gate electrode in place, an electrode liner 112 is applied over the gate metal. The liner is a thin layer of a non-conducting and electrically inert material, such as a ceramic or oxide. Additional layers 114 of dielectric and other layers for connection, wiring, isolation and structure are formed over the liner. A contact 116 is formed through these layers to make an electrical contact with the gate electrode. While only a gate electrode is shown, additional electrodes may be added, depending on the particular device. A similar structure may be used for a source, drain, and any other nodes or contacts of the device.

As examples for an n-type transistor, there is a first n-well 122 for a source and a contact 124 coupled to the n-well. There is a second n-well 126 for a drain and a contact 128 coupled to the well. The liner extends over the source and drain just as for the gate with an opening for the contact. Additional structure such as shallow trench isolation, oxides, overlying dielectrics, and distribution and connection layers are not shown in order not to obscure the liner and other aspects.

The structure is referred to typically as a finFET, however, the fin-based structure may be used to form other devices in addition to transistors, including diodes, control gates, switches, connecting nodes, etc. In the present description, a transistor will be described with a source, drain, and gate, however, the same structure, principles, and techniques may be applied to other

fin-based devices with other types of nodes. The principles of the present invention may be applied to a variety of different fin materials instead of SiGe and GE. The fin may be made of any semiconducting (e.g. III-V, II-V, C-containing), organic, or conducting dielectric (e.g. ZnO, NiO) materials.

Figures 2, 3, and 4 show a Ge/SiGe fin suitable for constructing a transistor as described herein. Figure 3 is a side view diagram along the fin similar to that of Figure 1. Figure 2 is an S/D fin cut cross-section of the same structure taken across the fin at the position of either the source or the drain. Figure 4 is a gate fin cut cross-section of Figure 3 structure taken across the fin at the position of the gate which is in the center of Figure 3.

In each of Figures 2, 3, and 4 a SiGe subfin 204 is formed over a silicon substrate 202. A Ge fin 208 is formed over the subfin and a shallow trench isolation (STI) is formed over the substrate 202 on both sides of the fin. Typically the silicon substrate 202 is a wafer with many parallel rows of fins. The STI is formed between all of the rows. While the illustrated fin has a Ge fin over a SiGe subfin, the wafer and portions of each die may have other types of dies and areas that do not have fins. The process described herein may be applied to a Ge-SiGe fin while other parts of the wafer are masked or at least masked for some parts of the process.

The substrate is described as silicon but may be formed of many other materials to suit different implementations. The substrate may be a semiconductor substrate but may also be another type of material such as oxide in silicon-on-insulator (SOI), partial SOI substrate, polysilicon, amorphous silicon, ceramic, glass or organic materials, etc. The semiconductor substrate may have multiple wafers or dies which are stacked or otherwise deposited or grown. The fin may be formed by removing material between the fins to create ridges from the substrate. Alternatively, the fin may be formed by applying or depositing material over the substrate

Figures 5, 6, and 7 show a second fabrication stage of the transistor of Figures 2, 3, and 4. At this stage a gate oxide layer 210 is deposited over the entire surface of the transistor and any other similar neighboring transistors. The gate oxide may be SiO_2 or any other suitable oxide, depending on the particular characteristics desired for the transistor. While referred to herein as a gate oxide, the layer may be formed of other dielectric materials that can be formed or patterned over the fin, such as high-k materials include hafnium silicate, zirconium silicate, hafnium dioxide and zirconium dioxide, etc. The gate dielectric may be applied by any of a variety of different techniques including atomic layer deposition.

The gate oxide is followed by the selective deposition of a gate metal, such as Cu, Ti, or Al. Alternatively, the gate 212 may be formed of polysilicon or another suitable non-metallic material. The gate metal may be deposited using photolithography or in any other way. In

photolithography, a photoresist is first applied and exposed over the planned transistor gates. The photoresist is removed over the portions for each gate. The gate metal is then deposited or plated and the photoresist is removed leaving the structure shown in the figures. The gate fin cut of Figure 7 shows the gate metal deposited over the gate oxide on the fin and the S/D fin cut of Figure 5 shows only the liner. There is no gate metal over the source and drain.

Figures 8, 9, and 10, show the transistor after excess gate oxide has been removed. In this process, the gate metal may be used as a mask over the gate oxide. All of the gate oxide that is not covered by the gate metal is removed. As shown in Figure 8 the source/drain and STI areas are exposed. The gates as shown in Figure 10 are covered in oxide. The gate metal provides a convenient mask for etching techniques but other processes may be used including applying the oxide only over the gates initially.

Figures 11, 12, and 13, show the transistor after spacers and RSD (Raised Soure/Drain) formations have been applied. The gate fin cut of Figure 13 shows that the gate is not directly affected, however Figure 12 shows that spacers 216 are applied on each side of the gate along and around the fin. The spacers serve to isolate the gate metal from layers that are applied later, such as the ILD (Inter-Layer Dielectric) layers.

In addition, a raised source and a raised drain 214 are applied over and around the fin. The shape of the RSD 214 is shown also in the S/D fin cut view of Figure 11, although other shapes may also be used. The RSD may be formed of doped Si, Ge, SiGe, or another suitable material. The particular shapes may be formed by epitaxial growth or by photolithography as discussed above or in any other suitable fashion. Alternatively, instead of a raised source and drain, the source and drain may be formed by doping the Ge fin

Figures 14, 15, and 16 are three views of the transistor after a process to recess the height of the STI 206. The STI is etched away using any of a variety of suitable techniques after the gate, source, drain and any other appropriate structures are masked. The etching leaves an exposed region 220 of the fin. This region is mostly the SiGe subfin, but depending on the particular configuration may also include some of the Ge fin. While there are many benefits to recessing the STI, the reduced STI layer leaves a part of the SiGe subfin exposed. If an ILD were to be applied directly over the structure, there would be a direct interface between the SiGe subfin and the ILD which typically includes a significant amount of silica (SiO_2). As mentioned above, there may be significant leakage from the SiGe subfin channel of this transistor and the ILD. A liner may be used to stop at least some of the leakage.

By etching the STI, the STI is prevented from being in contact with the P-N junction between the Ge and the n+Ge. This removes a potential source of current leakage from the P-N

junction. The STI may be etched before or after some of the other operations described here. The thickness of the STI may be configured to suit different purposes. In the described examples, the STI is etched sufficient to prevent the monolayer from being in contact with the Ge in order to avoid the leakage.

Figures 17, 18, and 19 are three views of depositing a liner 222 over the entire transistor structure and particularly in the exposed undercut regions 220 of the SiGe subfin. The layer may be deposited or plated and covers the entire transistor in this example. However there are areas that do not need to be covered such as the source, drain, and gate locations for the attachment of contacts or electrodes. Accordingly, the application of the liner may be modified to only include exposed parts of the fin and the RSD.

The liner is selected as a non-conductive or low conductivity material that adheres well to the materials of the fin. This may be Si and Ge but may be other materials, depending on the particular implementation. A variety of electrically inert materials may also be used. Some suitable materials are ceramics and oxides. Some examples of such materials include Al_2O_3, TiO_2, SiN, HfO_2, TiON, GeO_2, GeN, ZrO_2 and others.

As shown this non-conducting or dielectric liner material 222 forms an electrical conduction barrier around the fin on both sides as shown in both the S/D cut of Figure 17 and the gate cut of Figure 19. It also forms a barrier across the top of the fin including the gate electrode 212, the spacers 216 and the RSD 214. The ends of the fin 208 and the subfin 204 are also covered in the liner. The entire transistor is electrically isolated on the top. The only conduction path is therefore into the substrate 202 which is a very limited path for a FinFET structure.

Figures 20, 21, and 22 show the transistor structure after an ILD 230 has been applied over all or most of the wafer. The ILD is applied over the liner 222 so that the liner is between the ILD and the fin 204, 208 and between the ILD and the source 214, drain 214, and gate 212. The ILD may be formed of conventional materials including silica and there will be no or very little electrical conduction or leakage into the ILD 230 because of the liner 222.

In Figures 23, 24, and 25, the transistor is completed with the addition of source and drain contacts 232. In particular, holes are etched through the ILD 230 and the liner 222 to reach the source 214 and drain 214. These holes are then filled with a suitable conductor such as copper or aluminum. There may also be a gate contact 234 through the liner 222 to the gate metal 212. The arrangement and configuration of the contact may be adapted to suit different devices.

The device is then finished with any additional operations as may be suitable for the intended device such as adding additional metal and dielectric layers, creating further contacts,

conductive paths and connections, polishing and other finishing operations. The wafer is diced to form individual chips which are packaged as appropriate for the intended application.

While a single transistor with a single source, gate, and drain is shown, the principles described herein may be applied to other types of devices, such as diodes and control gates. There may be more gates, more source nodes, more drain nodes, etc. Additional devices may be formed over or under or beside the transistor to form more complex structures.

As described, the liner is applied after the gate and the RSD has been deposited. This allows for a wide variety of different liners to be used because the liner does not need to later be removed in part. In addition a liner in this location has very little effect on the channel so that a greater variety of different liners may be used.

Comparing Figure 24 with Figure 1 shows that a transistor structure may be produced with or without the raised source and drain. For other devices, there may be other source or drain structures or configurations. There may be more gates or no gates, depending on the type of device. The liner may also be applied to other types of FinFET devices.

Figure 26 illustrates a computing device 11 in accordance with one implementation. The computing device 11 houses a board 2. The board 2 may include a number of components, including but not limited to a processor 4 and at least one communication chip 6. The processor 4 is physically and electrically coupled to the board 2. In some implementations the at least one communication chip 6 is also physically and electrically coupled to the board 2. In further implementations, the communication chip 6 is part of the processor 4.

Depending on its applications, computing device 11 may include other components that may or may not be physically and electrically coupled to the board 2. These other components include, but are not limited to, volatile memory (e.g., DRAM) 8, non-volatile memory (e.g., ROM) 9, flash memory (not shown), a graphics processor 12, a digital signal processor (not shown), a crypto processor (not shown), a chipset 14, an antenna 16, a display 18 such as a touchscreen display, a touchscreen controller 20, a battery 22, an audio codec (not shown), a video codec (not shown), a power amplifier 24, a global positioning system (GPS) device 26, a compass 28, an accelerometer (not shown), a gyroscope (not shown), a speaker 30, a camera 32, and a mass storage device (such as hard disk drive) 10, compact disk (CD) (not shown), digital versatile disk (DVD) (not shown), and so forth). These components may be connected to the system board 2, mounted to the system board, or combined with any of the other components.

The communication chip 6 enables wireless and/or wired communications for the transfer of data to and from the computing device 11. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc.,

that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 6 may implement any of a number of wireless or wired standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, Ethernet derivatives thereof, as well as any other wireless and wired protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 11 may include a plurality of communication chips 6. For instance, a first communication chip 6 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 6 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

In some implementations, the integrated circuit die of the processor, memory devices, communication devices, or other components are fabricated to include two transistor, one resistor memory cells with an RRAM or other element as described herein. The described memory cells may be embedded as memory for other components in a CMOS or other logic processing die or a standalone memory array may be made on its own die. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In various implementations, the computing device 11 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 11 may be any other electronic device that processes data including a wearable device.

Embodiments may be implemented as a part of one or more memory chips, controllers, CPUs (Central Processing Unit), microchips or integrated circuits interconnected using a motherboard, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA).

References to "one embodiment", "an embodiment", "example embodiment", "various embodiments", etc., indicate that the embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the

particular features, structures, or characteristics. Further, some embodiments may have some, all, or none of the features described for other embodiments.

In the following description and claims, the term "coupled" along with its derivatives, may be used. "Coupled" is used to indicate that two or more elements co-operate or interact with each other, but they may or may not have intervening physical or electrical components between them.

As used in the claims, unless otherwise specified, the use of the ordinal adjectives "first", "second", "third", etc., to describe a common element, merely indicate that different instances of like elements are being referred to, and are not intended to imply that the elements so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

In the drawings, for purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of the disclosed techniques may have less than perfect straight lines, right angles, etc., and some features may have surface topology or otherwise be non-smooth, given real world limitations of fabrication processes. In short, the figures are provided merely to show example structures.

The drawings and the forgoing description give examples of embodiments. Those skilled in the art will appreciate that one or more of the described elements may well be combined into a single functional element. Alternatively, certain elements may be split into multiple functional elements. Elements from one embodiment may be added to another embodiment. For example, orders of processes described herein may be changed and are not limited to the manner described herein. Moreover, the actions of any flow diagram need not be implemented in the order shown; nor do all of the acts necessarily need to be performed. Also, those acts that are not dependent on other acts may be performed in parallel with the other acts. The scope of embodiments is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of embodiments is at least as broad as given by the following claims.

The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications. Some embodiments pertain to a structure that includes a subfin liner for use with FinFET devices. In one example, a FinFET device includes a semiconductor substrate having a front side surface, a fin extending from the front side surface, a

node of the fin applied over the fin, a dielectric liner over the node, and inter-layer dielectric over the front side surface and the node.

In some embodiments the liner is also over the fin.

Further embodiments include shallow trench isolation beside the fin and wherein the liner is also over the shallow trench isolation.

In some embodiments the device comprises a transistor, wherein the node comprises a gate, the transistor further comprising a raised source as a node and a raised drain as a node and wherein the liner is over the gate, the source and the drain.

In some embodiments the liner is formed of a ceramic.

In some embodiments the liner is formed a material selected from a group consisting of of Al2O3, TiO2, SiN, HfO2, TiON, GeO2, GeN, and ZrO2

In some embodiments the inter-layer dielectric is formed of silica.

In some embodiments the fin comprises a silicon germanium sub fin and a germanium fin over the sub fin and wherein the liner covers a portion of the subfin.

In some embodiments the fin is formed from the semiconductor substrate.

Further embodiments include a gate over the fin, the gate comprising a gate oxide over the fin and a gate metal over the gate oxide and wherein the liner is over the gate metal.

In some embodiments the gate oxide is formed of silica and the liner is formed of a dielectric material other than silica.

Some embodiments pertain to a method of forming a fin-based device that includes forming a fin on a front side surface of a semiconductor substrate, forming a node over the fin;

forming a dielectric liner over the node, and forming an inter-layer dielectric over the front side surface and the node.

In some embodiments forming a liner comprises forming the liner also over the fin.

Further embodiments include forming a shallow trench isolation over the substrate beside the fin before forming the node and recessing the shallow trench isolation after forming the node and before forming the liner.

Further embodiments include forming spacers beside the node and wherein forming the liner comprises forming the liner over the spacers.

Further embodiments include etching a hole through the inter-layer dielectric and the liner to reach the node and forming a contact to the node in the hole.

In some embodiments the fin is formed of Ge and the liner is formed of silica.

Some embodiments pertain to a computing system that includes a memory having instructions stored thereon, and a processor coupled to the memory to execute the instructions,

the processor having transistors formed over a silicon substrate having a front side surface, at least some of the transistors having a fin extending from the front side surface, a node of the fin applied over the fin, a dielectric liner over the node, and inter-layer dielectric over the front side surface and the node.

In some embodiments the transistors further comprise a raised source as a node and a raised drain as a node and wherein the liner is over the gate, the source and the drain.

In some embodiments the liner is formed of a ceramic.

CLAIMS

1. A fin-based semiconductor device comprising:

a semiconductor substrate having a front side surface:

a fin extending from the front side surface;

a node of the fin applied over the fin;

a dielectric liner over the node; and

inter-layer dielectric over the front side surface and the node.

2. The device of Claim 1, wherein the liner is also over the fin.

3. The device of Claim 2, further comprising shallow trench isolation beside the fin and wherein the liner is also over the shallow trench isolation.

4. The device of any one or more of the above claims, wherein the device comprises a transistor, wherein the node comprises a gate, the transistor further comprising a raised source as a node and a raised drain as a node and wherein the liner is over the gate, the source and the drain.

5. The device of any one or more of the above claims, wherein the liner is formed of a ceramic.

6. The device of Claim 4, wherein the liner is formed a material selected from a group consisting of of Al_2O_3, TiO_2, SiN, HfO_2, TiON, GeO_2, GeN, and ZrO_2

7. The device of any one or more of the above claims, wherein the inter-layer dielectric is formed of silica.

8. The device of any one or more of the above claims, wherein the fin comprises a silicon germanium sub fin and a germanium fin over the sub fin and wherein the liner covers a portion of the subfin.

9. The device of Claim 1, wherein the fin is formed from the semiconductor substrate.

10. The device of any one or more of the above claims, further comprising a gate over the fin, the gate comprising a gate oxide over the fin and a gate metal over the gate oxide and wherein the liner is over the gate metal.

11. The device of Claim 10, wherein the gate oxide is formed of silica and the liner is formed of a dielectric material other than silica.

12. A method of forming a fin-based device comprising:

forming a fin on a front side surface of a semiconductor substrate:

forming a node over the fin;

forming a dielectric liner over the node; and

forming an inter-layer dielectric over the front side surface and the node.

13. The method of Claim 12, wherein forming a liner comprises forming the liner also over the fin.

14. The method of Claim 12 or 13, further comprising forming a shallow trench isolation over the substrate beside the fin before forming the node and recessing the shallow trench isolation after forming the node and before forming the liner.

15. The method of any one or more of claims 12 to 14, further comprising forming spacers beside the node and wherein forming the liner comprises forming the liner over the spacers.

16. The method of any one or more of claims 12 to 15, further comprising etching a hole through the inter-layer dielectric and the liner to reach the node and forming a contact to the node in the hole.

17. The method of any one or more of claims 12 to 16, wherein the fin is formed of Ge and the liner is formed of silica.

18. A computing system comprising:

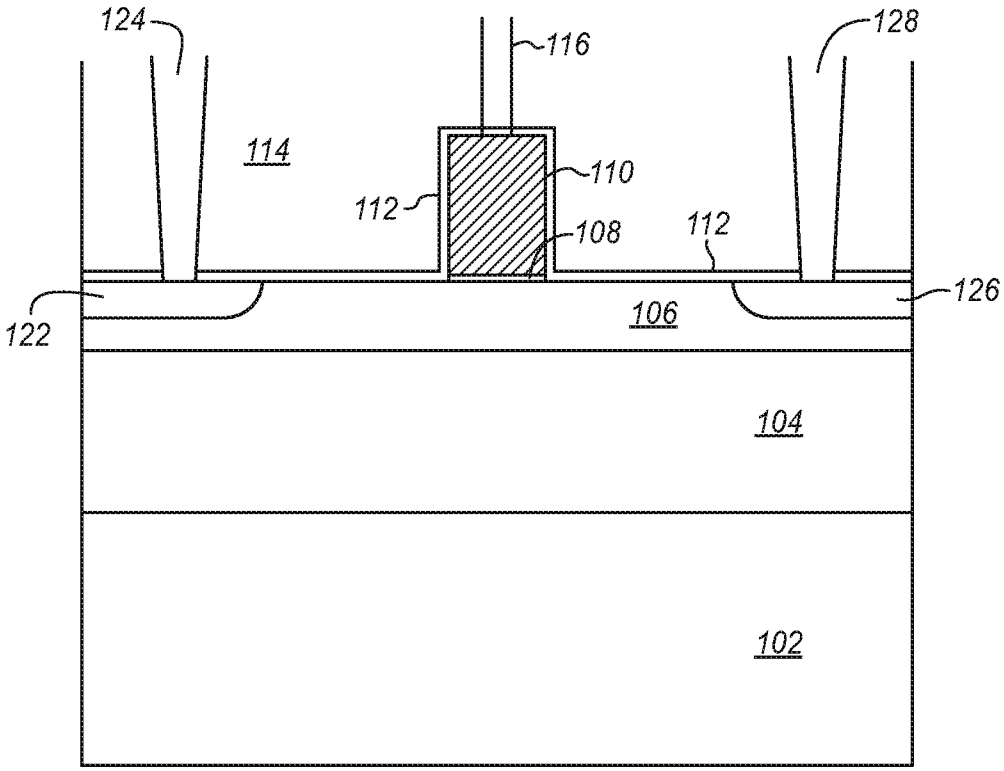
a memory having instructions stored thereon; and

a processor coupled to the memory to execute the instructions, the processor having transistors formed over a silicon substrate having a front side surface, at least some of the transistors having a fin extending from the front side surface, a node of the fin applied over the fin, a dielectric liner over the node, and inter-layer dielectric over the front side surface and the node.

19. The computing system of Claim 18, wherein the transistors further comprise a raised source as a node and a raised drain as a node and wherein the liner is over the gate, the source and the drain.

20. The computing system of Claim 18 or 19, wherein the liner is formed of a ceramic.

FIG. 1



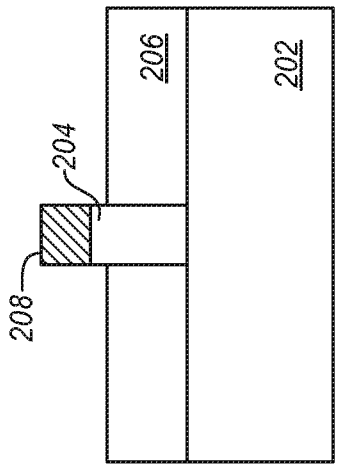


FIG. 4

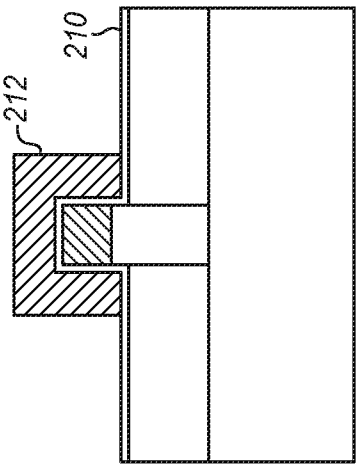


FIG. 7

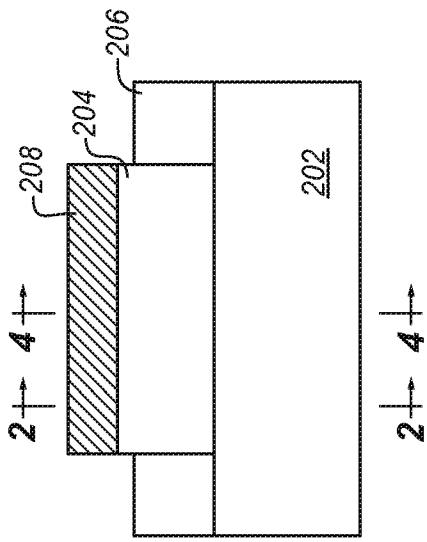


FIG. 3

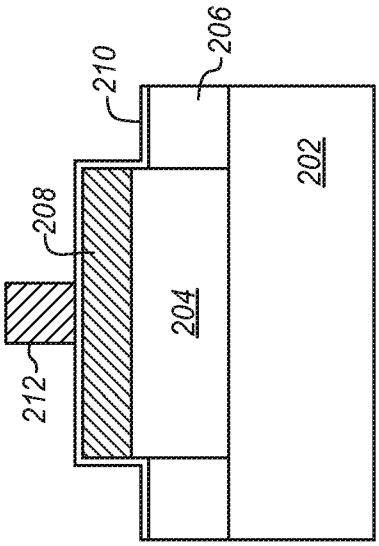


FIG. 6

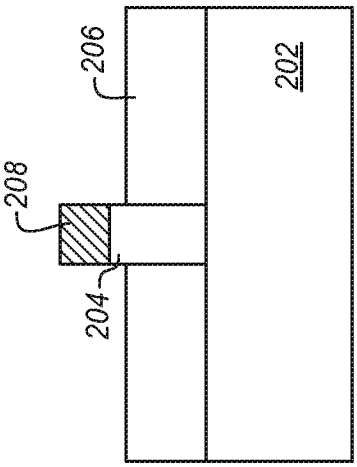


FIG. 2

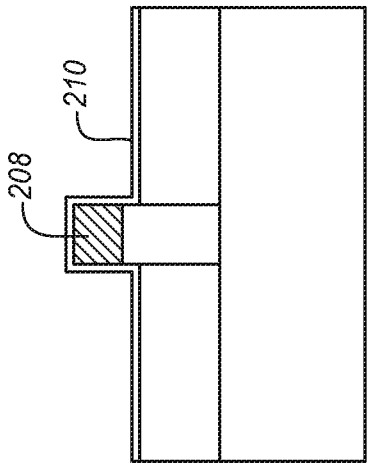


FIG. 5

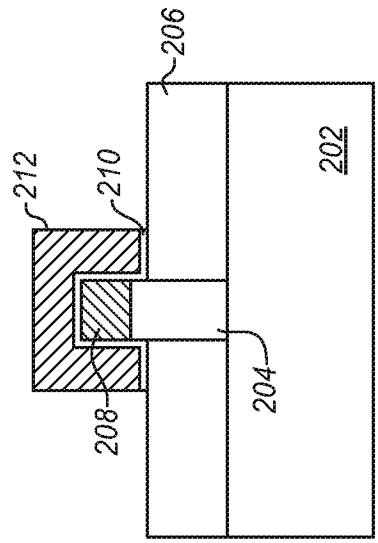


FIG. 10

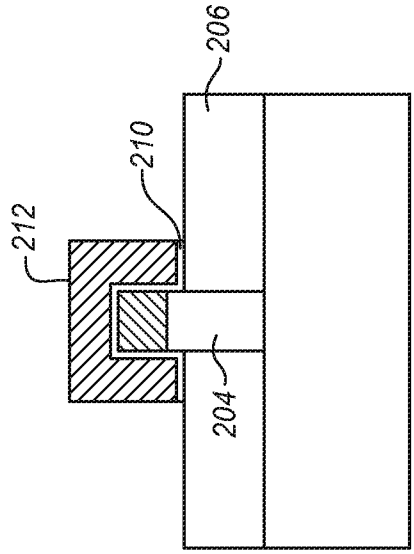


FIG. 13

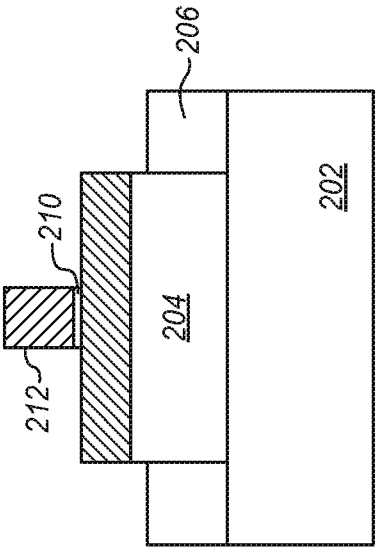


FIG. 9

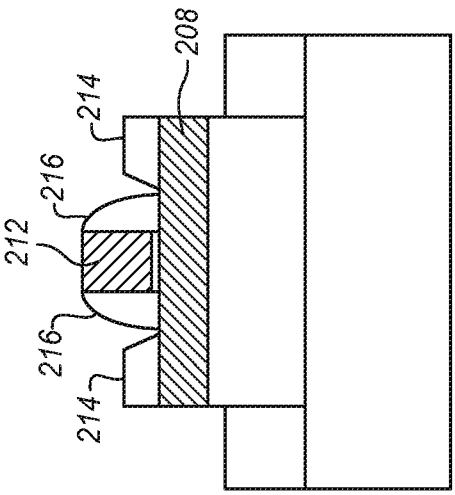


FIG. 12

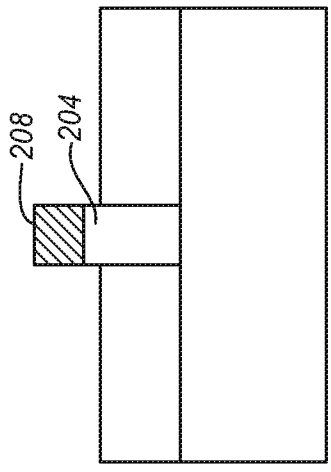


FIG. 8

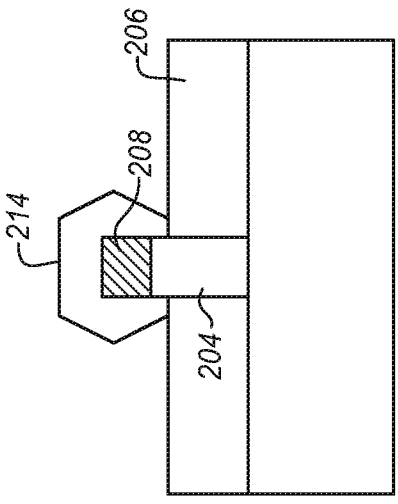


FIG. 11

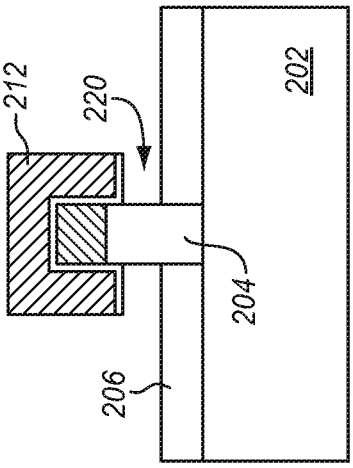


FIG. 16

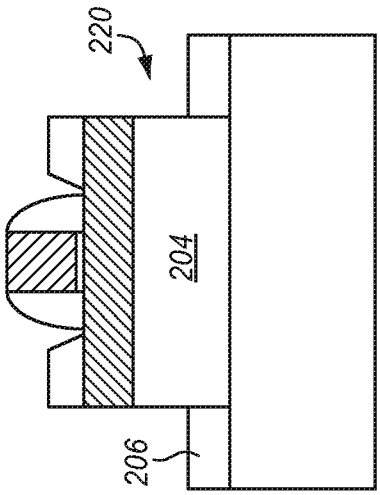


FIG. 15

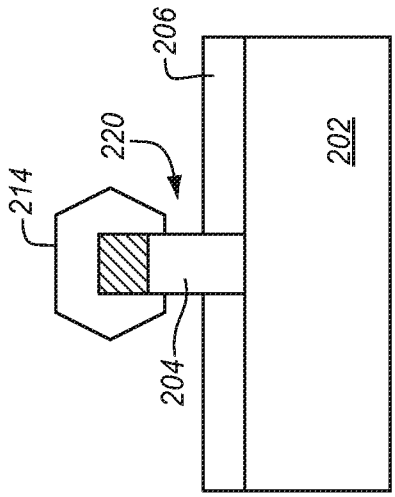


FIG. 14

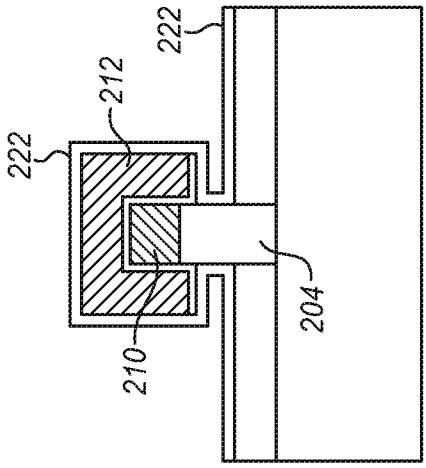


FIG. 19

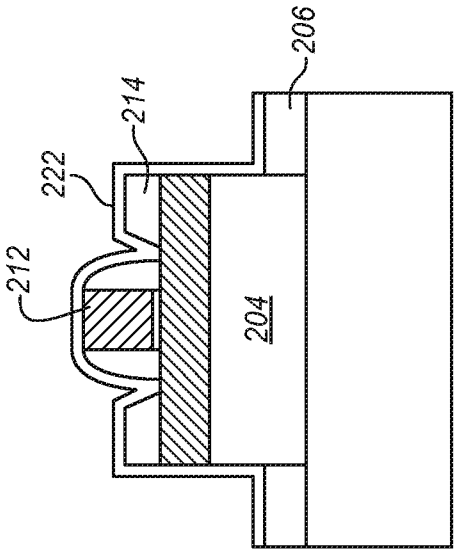


FIG. 18

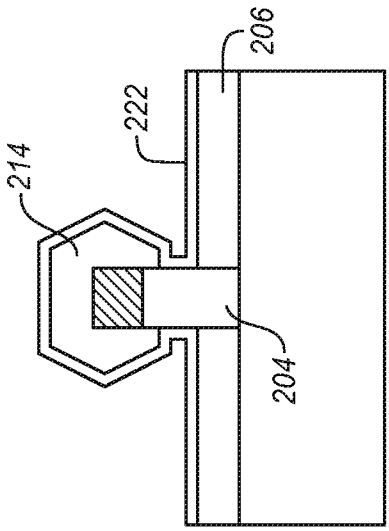


FIG. 17

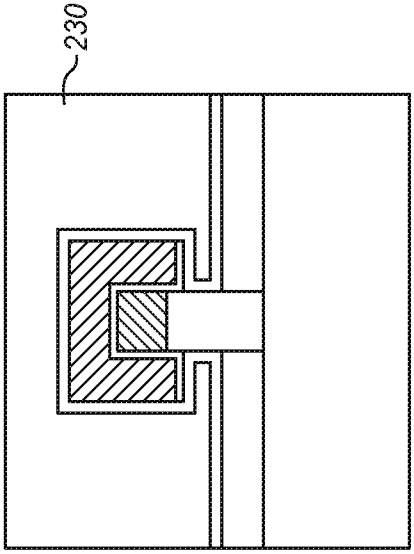


FIG. 22

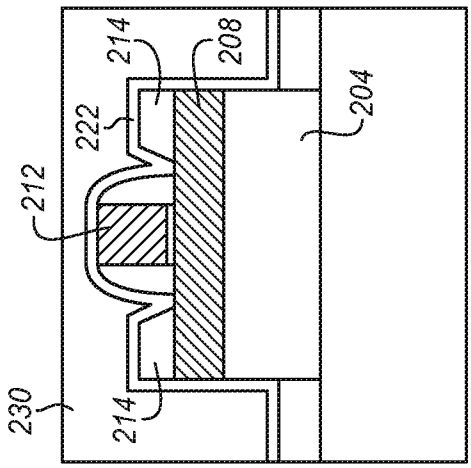


FIG. 21

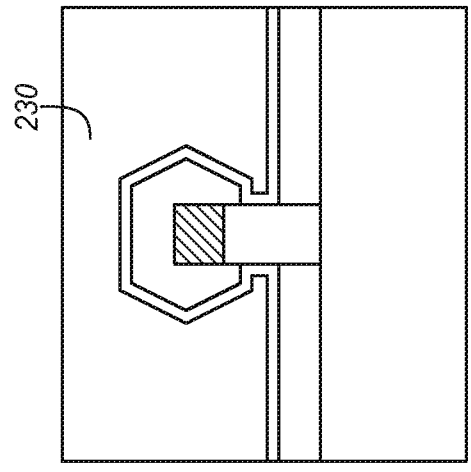


FIG. 20

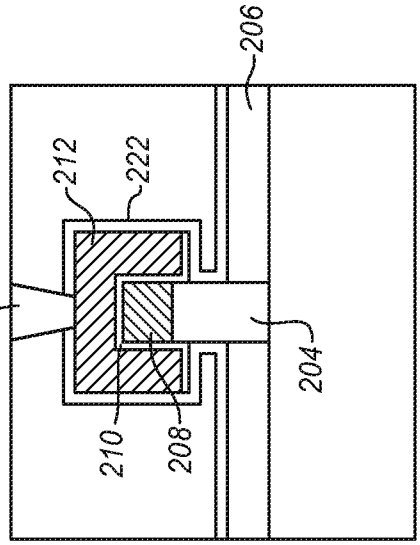


FIG. 25

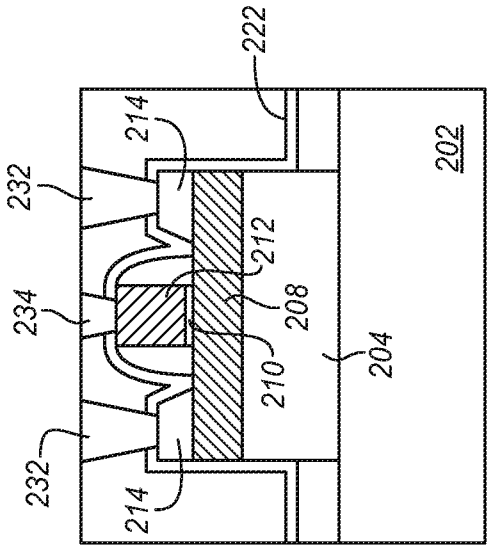


FIG. 24

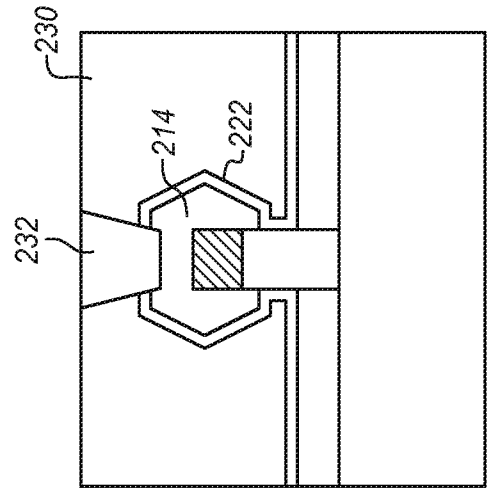
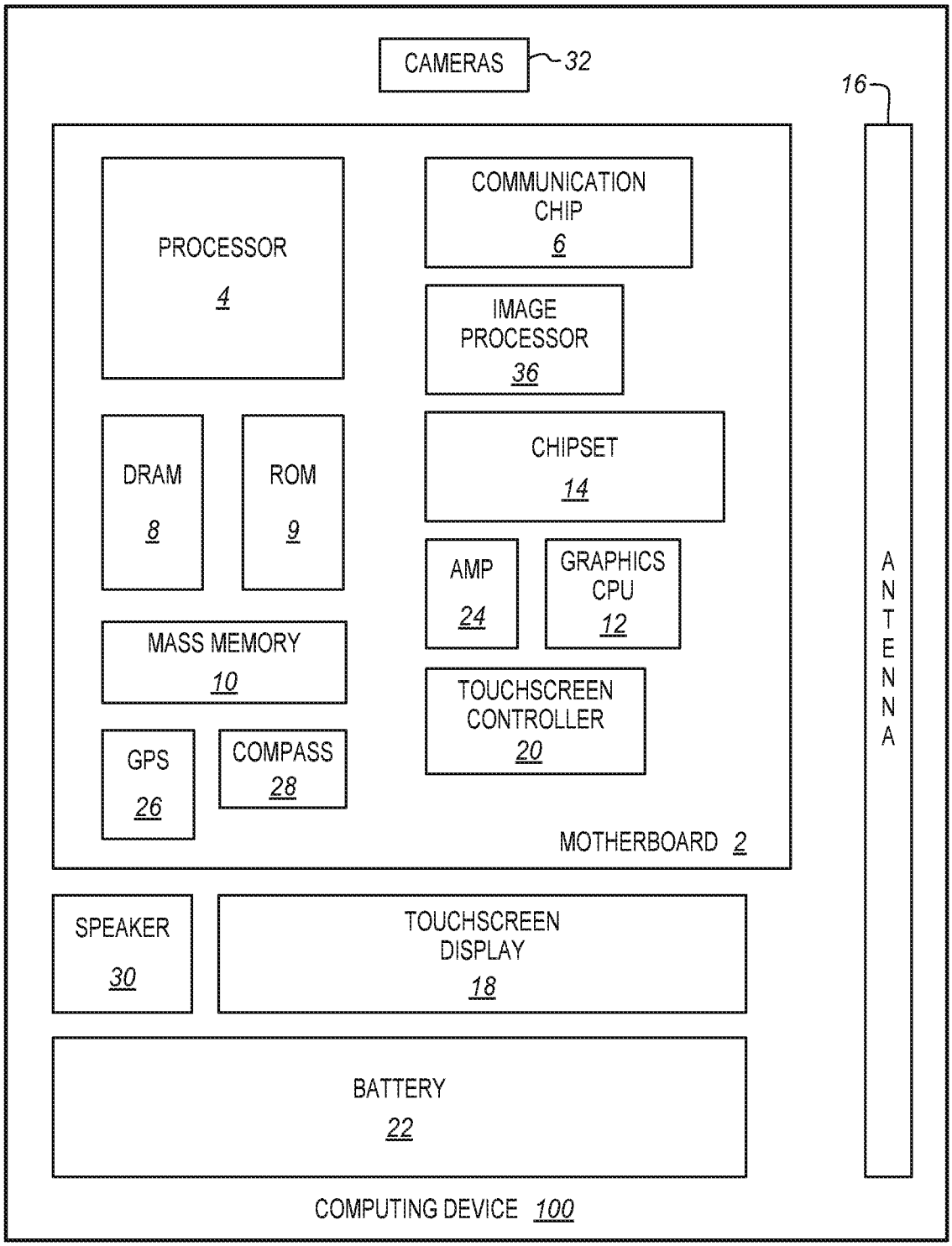


FIG. 23

FIG. 26


CAMERAS
32
16
PROCESSOR
4
COMMUNICATION CHIP
6
IMAGE PROCESSOR
36
DRAM
8
ROM
9
CHIPSET
14
AMP
24
GRAPHICS CPU
12
MASS MEMORY
10
TOUCHSCREEN CONTROLLER
20
GPS
26
COMPASS
28
MOTHERBOARD 2
ANTENNA
SPEAKER
30
TOUCHSCREEN DISPLAY
18
BATTERY
22
COMPUTING DEVICE 100

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/069415

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 29/66(2006.01)i, H01L 29/417(2006.01)i, H01L 21/8238(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 29/08; H01L 21/28; H01L 21/8238; H01L 29/66; H01L 27/092; H01L 27/12; H01L 29/417

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: finfet, liner, cover, dielectric, source, drain

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013-0154005 A1 (BASKER et al.) 20 June 2013 See paragraphs [0045]-[0048], [0079]-[0088] and figures 2, 9A-10B.	1-3,9,12-14,18-20
Y	US 2014-0138742 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 22 May 2014 See paragraphs [0008], [0016]-[0017] and figures 1, 9-10.	1-3,9,12-14,18-20
A	US 2015-0035069 A1 (UNITED MICROELECTRONICS CORP.) 05 February 2015 See claims 1-3 and figures 1-11.	1-3,9,12-14,18-20
A	US 2015-0179756 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 25 June 2015 See claims 1-7 and figures 1-10.	1-3,9,12-14,18-20
A	US 2016-0099342 A1 (INTERNALTIONAL BUSINESS MACHINES CORPORATION) 07 April 2016 See claims 1-6 and figures 1-13B.	1-3,9,12-14,18-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 September 2017 (19.09.2017)	**19 September 2017 (19.09.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KANG, Sung Chul
Telephone No. +82-42-481-8405

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/069415

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 6, 11
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claim 6 is unclear, because it refers to multiple dependent claim 4 which does not comply with PCT Rule 6.4(a).
Claim 11 is unclear, because it refers to multiple dependent claim 10 which does not comply with PCT Rule 6.4(a).

3. ☒ Claims Nos.: 4-5, 7-8, 10, 15-17
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/069415

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0154005 A1	20/06/2013	CN 104247016 A	24/12/2014
		CN 104247016 B	22/02/2017
		DE 112012004932 B4	03/12/2015
		DE 112012004932 T5	11/09/2014
		GB 2512240 A	24/09/2014
		GB 2512240 B	04/11/2015
		TW 201342433 A	16/10/2013
		TW I534864 B	21/05/2016
		US 2013-0154006 A1	20/06/2013
		US 2014-0339640 A1	20/11/2014
		US 8445334 B1	21/05/2013
		US 8723262 B2	13/05/2014
		US 8871626 B2	28/10/2014
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		DE 102013105608 B3	13/02/2014
		KR 10-1543508 B1	11/08/2015
		KR 10-2014-0107078 A	04/09/2014
		US 2014-0239396 A1	28/08/2014
		US 8981496 B2	17/03/2015
		US 9331179 B2	03/05/2016
US 2016-0099342 A1	07/04/2016	US 2016-0099246 A1	07/04/2016
		US 9362285 B2	07/06/2016
		US 9484348 B2	01/11/2016