

[54] **CREDIT-ACCUMULATING
ARRANGEMENT**

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[51] Int. Cl. G06f 7/385
[58] Field of Search 235/175, 173, 168, 174, 92 CN;
133/8; 194/10

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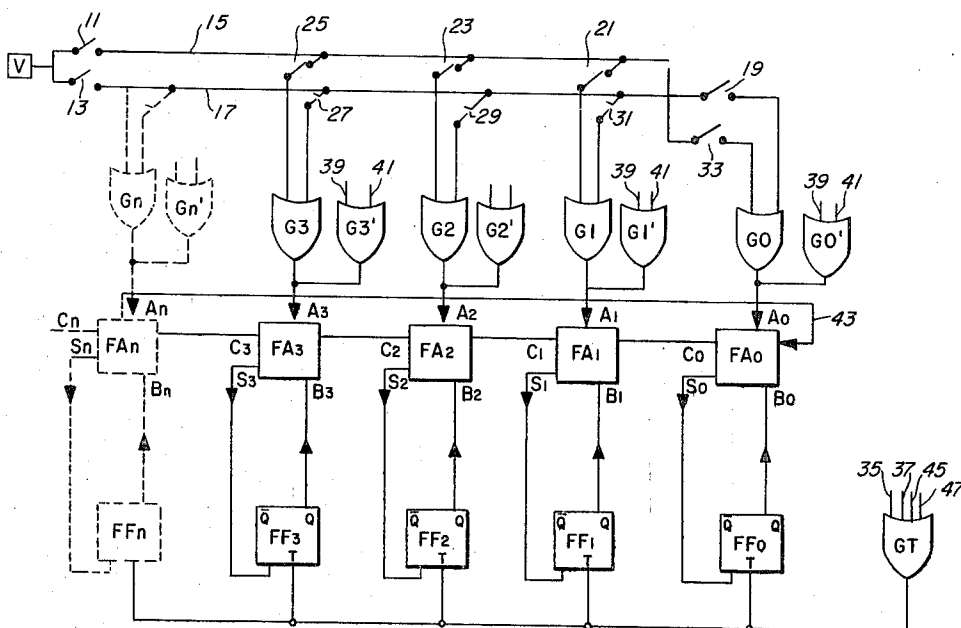
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[57] **ABSTRACT**

Addition of credits and subtraction of debits is electronically achieved by utilizing an accumulator circuit having multiple stages, each of which includes a binary full adder with a delay flip-flop in a feedback loop.

22 Claims, 6 Drawing Figures



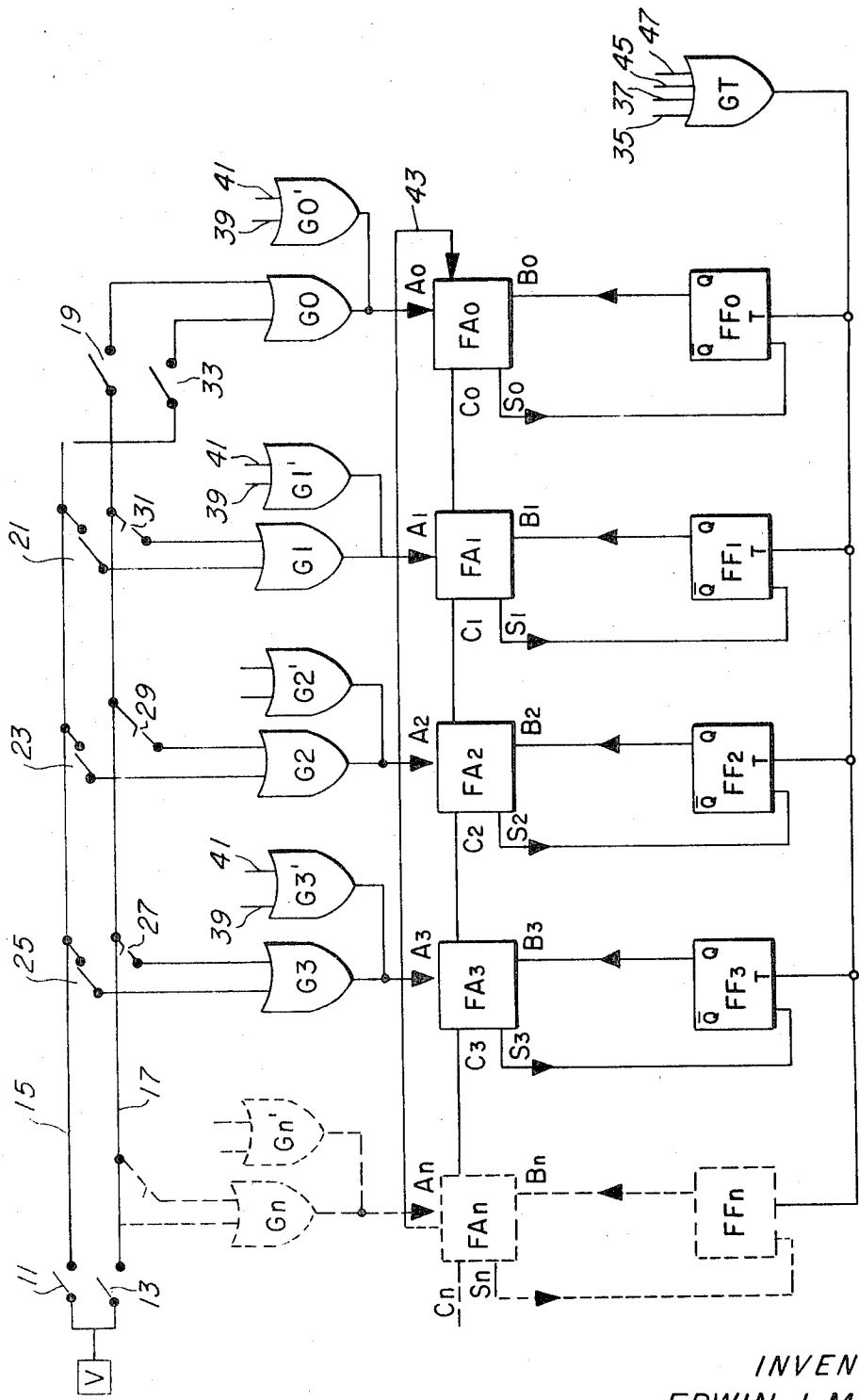
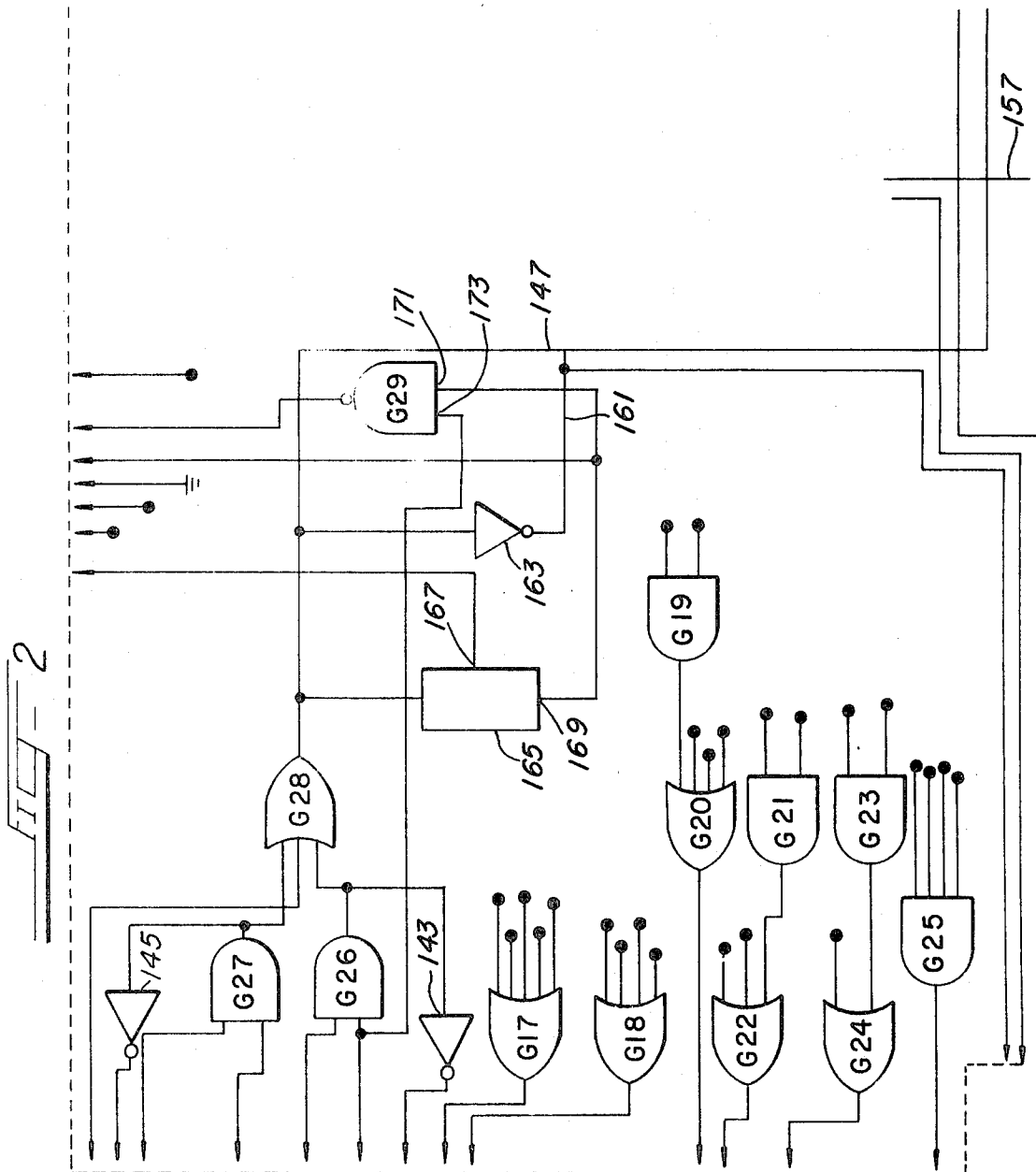


FIG. 1

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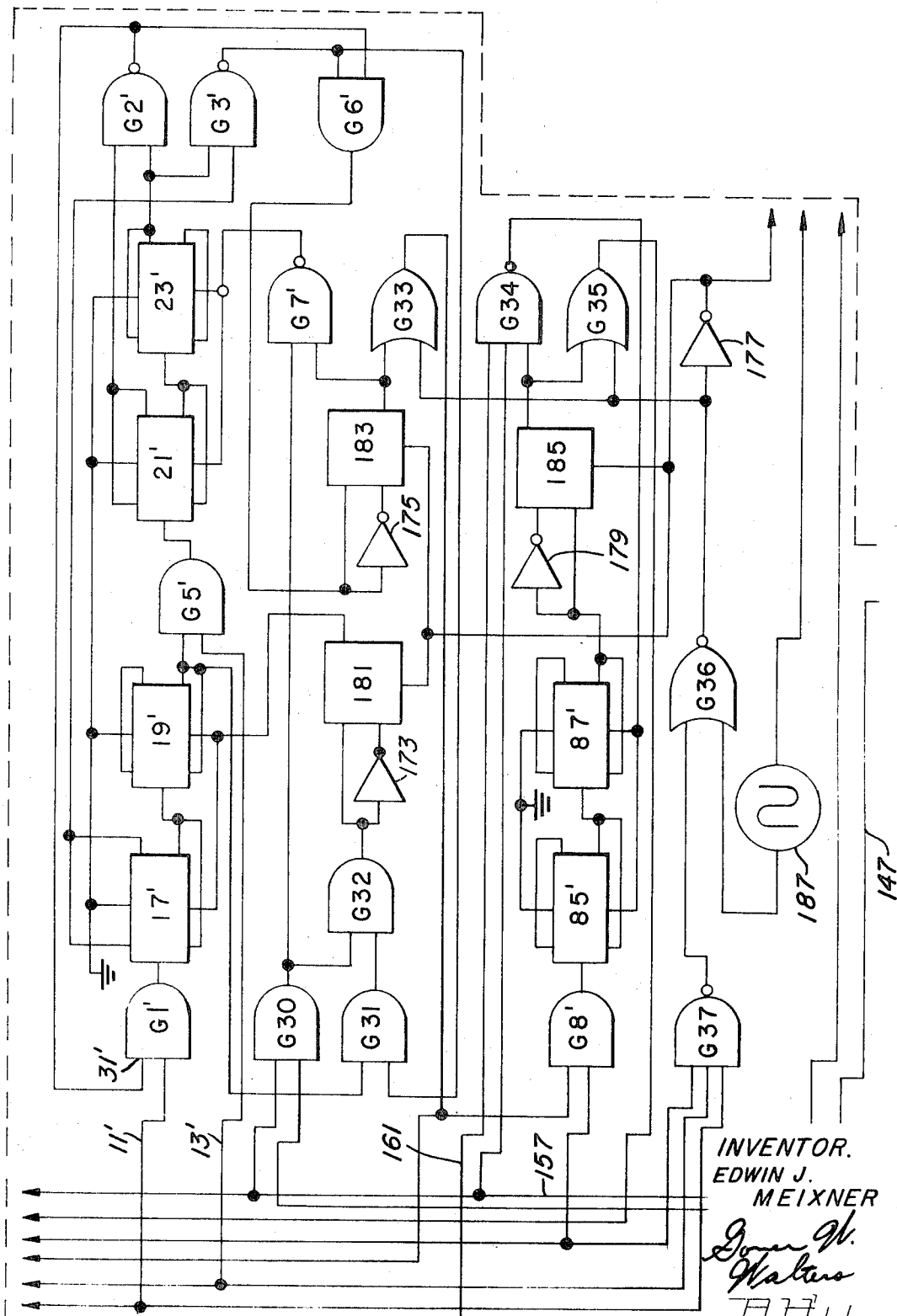
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FIG. 3



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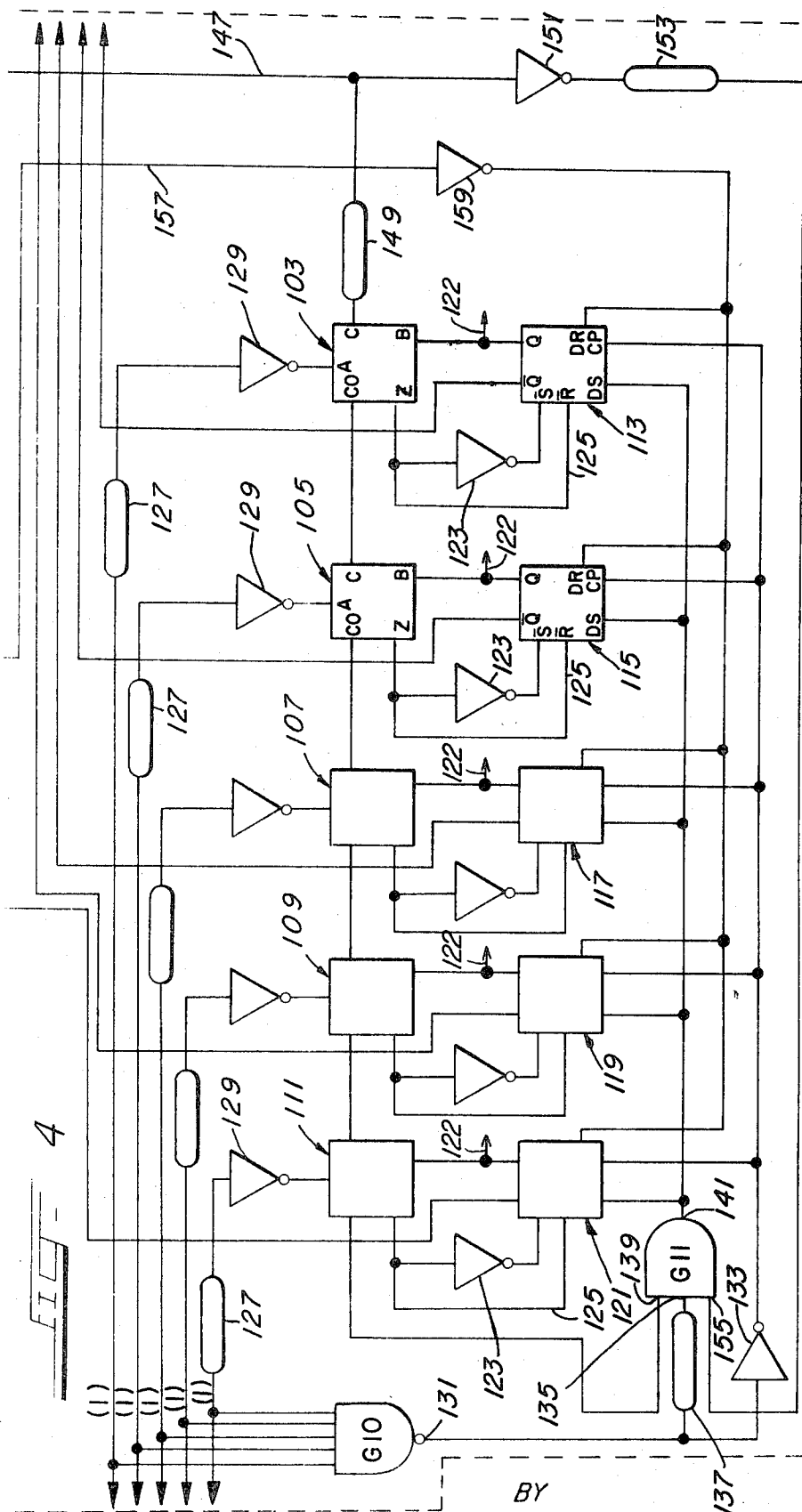


FIG. 2

FIG. 3

FIG. 4

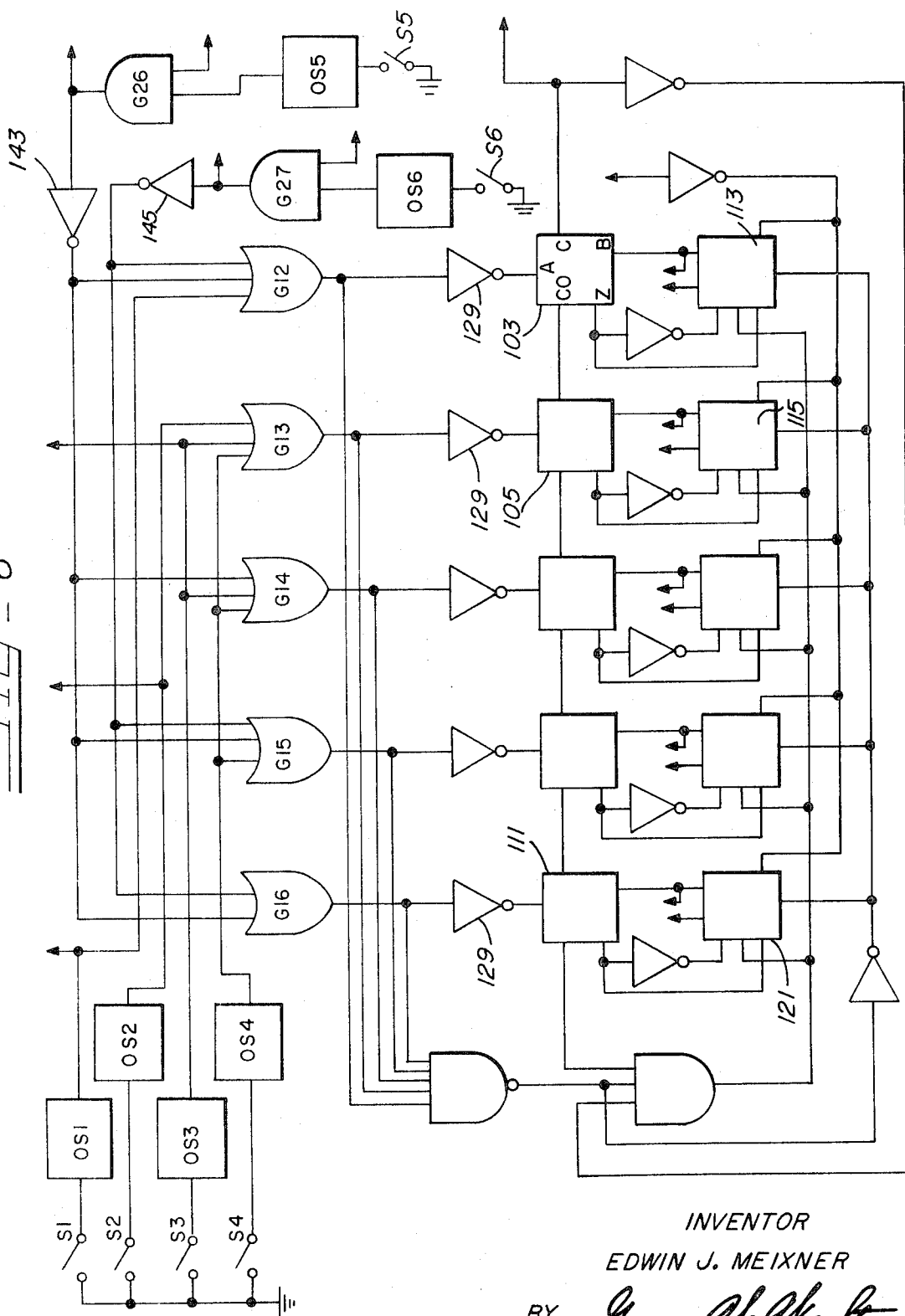
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FIG. 6



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CREDIT-ACCUMULATING ARRANGEMENT

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to an accumulator circuit for totaling credit inputs and subtracting debit inputs therefrom, and more specifically this invention relates to an electronic accumulator circuit utilizing a binary full adder and flip-flop circuit combination to provide credit and price comparisons for vending apparatus.

2. Description of the Prior Art

In the past, the accumulation of credit representative of deposited coins and the subtraction of the price of vended articles therefrom was generally achieved with mechanical and electromechanical devices. Such arrangements have been functional, but there are many disadvantages connected therewith. For instance, such arrangements are generally relatively slow due to the necessity of overcoming the inertia of mechanically movable parts and the general limitations on the speed with which mechanical structures may be moved. The delay in registering a credit for a properly deposited coin, or the delay in having the price of a vended article subtracted from the accumulator total, leads to such problems as opportunity for cheating, multiple vends, jamming the machine, and general customer dissatisfaction.

Attempts have been made to produce a wholly electronic accumulator. Some of these prior art electronic arrangements have some advantages over the mechanical or electromechanical accumulators, but in general they create almost as many problems as they do away with. One of the disadvantages of the prior art electrical approaches to an accumulator problem is that they have generally tended to require the inclusion of an electronic clock to regulate the operation of flip-flop circuits and other circuit elements. Further, the prior art approaches have generally tended to adopt lumped parameter circuit elements with the attendant problems of circuit construction, low reliability, and relative bulkiness. Further, while many of these electronic circuits are superior to the mechanical or electromechanical arrangement with respect to the speed of operation, they still generally do not provide the nearly instantaneous operation that is required for vending machine applications.

SUMMARY OF THE INVENTION

The present invention obviates the difficulties that are found in prior art devices and provides a relatively noncomplex, very compact, reliable, and extremely fast-acting credit-adding and price-subtracting arrangement.

Briefly, in the preferred embodiments disclosed herein, the present invention relates to an electronic accumulator that utilizes electronic arrangements that provide a full adding function (i.e., arithmetically add two or more numbers and produce an output indicative of a columnar digit and a carry output for inclusion in an adjacent columnar sum). The columnar digital information at the output of the adder circuit is passed through a memory storage and signal delay circuit, the output of which is fed back into the input of the adder circuit. Logic elements are utilized to aid in the energization of selected adder circuits. The energizing signals conveyed by the logic elements are representative of predetermined credit increment values. Subtraction of debits from accumulated values is achieved by complementary addition.

With the advent of integrated circuit concepts, the possibility of greatly miniaturized components and functions has become a reality. This is particularly true of the second generation of such devices, commonly referred to as monolithic integrated circuits. In these latter circuit arrangements, the concept of individual circuit parameters has practically disappeared. With modern practices, essentially whole circuit portions are diffused into minute chips of semiconductor material. The opportunity of achieving many goals not thought possible with the prior art individual parameter circuits now seem within reach. However, the utilization of the

new integrated circuit concepts require a whole new approach. As with many advances, the benefits thereof have been greatly diluted by too strict adherence to established principles and approaches. At the present time, there is a great deal of interest in the integrated circuit area and much research is being conducted. However, the practical utilization of the new technology in commercial situations is somewhat lagging.

With specific reference to the features of the present invention, an electronic accumulator has been developed with many advantageous features that are particularly adapted for use with integrated circuit technology, although the benefits of this circuit are not limited to its use in integrated circuit form. A multiple stage accumulator is provided, each stage being essentially formed of a binary full adder circuit and a flip-flop circuit in a feedback line from the output of the full adder to its input. The flip-flop circuit provides both a delay and a memory function. Coin switch inputs, representative of credit increments based on the value of the coins, are applied to selected full adder circuits to produce credit accumulation. Switching means are provided to selectively couple the coin switches to predetermined sets of full adders to permit an operator to choose the coin value to be associated with a switch and to adjustably set the credit increments to be allocated to the pulse of any coin switch. This flexibility in determining the programming of the coin and credit arrangement is an important feature of this invention.

Level detect logic circuitry is provided for determining the accumulated credit in the accumulator, and debit logic circuitry compares the accumulated credit to the price of a selected article. If sufficient credit has been established, the debit logic proceeds to subtract the price of the vended article from the accumulated credit. As is the case with the coin switch and credit increments the price increments are completely adjustable, since subtraction is achieved by complementary addition and is thus identical to the main accumulating function. With this arrangement, an essentially instantaneous operation of both addition and subtraction is realized. Also, the tooling cost and other manufacturing expenses are relatively low. Further, the circuit is completely clockless and thus avoids the prior art problems associated with the use of a controlling clock. When utilized in association with monolithic integrated circuit principles, all of these advantages are incorporated in an extremely small package with many less maintenance and failure problems.

Accordingly, it is a primary object of this invention to provide an accumulator circuit which provides essentially instantaneous addition and subtraction.

Another object of this invention is to provide a relatively inexpensive and extremely durable electronic accumulator circuit.

Yet another object of this invention is to provide an electronic accumulator circuit that does not require the use of a regulating clock.

A further object of this invention is to provide an electronic accumulator circuit in which credit and price levels may be easily adjusted.

Still a further object of this invention is to provide an electronic accumulator circuit that is especially adaptable for use with monolithic integrated circuitry.

These and other objects, advantages, and features of the subject invention will hereafter appear and for purposes of illustration, but not of limitation, exemplary embodiments of the subject invention are shown in the appended drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic circuit diagram of a preferred embodiment of this invention.

FIGS. 2, 3, and 4 jointly form a schematic circuit diagram of a circuit incorporating another preferred embodiment of this invention.

FIG. 5 illustrates the relationship between FIGS. 2, 3, and 4.

FIG. 6 is a schematic circuit diagram illustrating other features of a preferred embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The credit accounting system toward which this application is directed may be better understood by reference to the drawing hereof. Specifically, in FIG. 1 a schematic circuit diagram of a preferred embodiment of this invention illustrates the features thereof.

This description is based on the assumption that separate credit pulses, each representative of a particular credit value (e.g., nickel, dime, or quarter), are to be utilized by a customer in establishing credit equal to a given purchase price. Each of the credit values will be equivalent to a specified number of credit increments, with a credit increment being assigned, for example, to each five cents of value.

To accumulate the credit increments representative of deposited credit values, this invention involves the utilization of binary full adder circuits in combination with a delayed feedback and memory arrangement, such as inclusion of a conventional bistable device, commonly known as a flip-flop circuit, in the feedback loop. A delay would be built into the action of the flip-flop. The delay circuit in the feedback loop must also provide a memory function for purposes of subsequent accumulation. The basic form of the preferred embodiment of this invention is illustrated in FIG. 1.

The accumulator or counter illustrated in FIG. 1 has a multiplicity of stages, each stage having a binary full adder generally designated FA and a delay flip-flop generally designated FF. Each of the binary full adders FA is adapted to arithmetically sum two binary digits and provide a count output signal and a carry output signal. The primary digits being added by a full adder are pulses generally identified as inputs A and representing separate credit increments. The other digits to be added is the output of the full adder from the previous excitation, as fed back through delay flip-flop FF. This latter signal is generally designated B. The outputs of the representative binary full adders are designated $S_0, S_1, S_2, S_3,$ and S_n . Similarly, the carry output signals from each of the binary full adder stages are designated as $C_0, C_1, C_2, C_3,$ and C_n .

The primary output of a full adder is supplied to a delay flip-flop FF. As the output signal S is applied to the flip-flop FF, the signal is not immediately transferred to the Q output of the flip-flop. Rather, the signal is stored until a pulse is applied to the toggle terminal T of the flip-flop to toggle the signal S to the output terminal Q. Since the application of a pulse to terminal B of the full adder FA will cause the output signal on terminal S of the full adder to change simultaneously, a delay is necessary between the S terminal of the full adder and the B terminal thereof. If this delay were not introduced, a "race" situation would exist.

Pulse signals to drive the full adders FA are obtained from coin switches 11 and 13. Coin switches 11 and 13 are connected to a pulse source V which will provide pulses on lines 15 or 17 upon closure of switch 11 or switch 13. Although only two coin switches 11 and 13 are illustrated, it should be realized that any desired number of coin switches could be included in the circuit. Also, the particular coins adapted to actuate coin switches 11 and 13 and the number of credit increments to be granted therefor may be chosen as desired by the operator. The permit this latter function, selector switches 19, 21, 23, 25, 27, 29, 31, and 33 are utilized to adjust the number of credit increments that will be granted upon closure of a coin switch 11 or 13. As an example, suppose that it was desired to have coin switch 11 responsive to the depositing of nickels and it was desired to give one credit increment for each nickel deposited. To achieve this function, switch 33 would be closed so that each coin deposited to close coin switch 11 would result in pulsing of binary full adder FAO to have one credit increment in the accumulator.

Now suppose that it was desired to make coin switch 13 responsive to quarters and to award five credit increments for

each quarter deposited. In this case, switches 19 and 29 would be closed. Thus, when a quarter is deposited to close coin switch 13, pulses would be applied to binary full adders FAO and FA2. The pulse applied to FAO would, of course, cause the accumulator to add one credit increment to its total. A "1" located at the position of full adder FAO would indicate a quantity of one in the binary terminology. A "1" in the full adder FA1 position would indicate a count of 2, while a "1" in the FA2 position would indicate a count of 4. Therefore, by applying pulses to FAO and FA2 the binary count of five is registered in the accumulator. If it were desired to award six credit increments for each quarter deposited, and coin switch 13 was chosen to be responsive to the quarter, switches 29 and 31 would be closed to provide registration of counts of two and four, for a total of six, in the accumulator.

Pulses from coin switches 11 and 13 are conveyed to lines 15 and 17, through closed selector switches, to one or more of the associated OR-gates G0, G1, G2, G3, and Gn. OR-gates G are responsive to any signal applied thereto to pulse the associated binary full adder FA. The coin switch pulses on lines 15 and 17 are also applied to inputs 35 and 37 of a toggle gate GT. Toggle gate GT provides signals to the toggle terminals T of flip-flops FF to transfer or toggle the full adder outputs S to the Q terminals of the flip-flops.

Assuming that the circuit is in an initial or quiescent state, the A and B inputs and C and S outputs would all be in a binary "0" state. If a pulse is applied to the full adder FAO in these circumstances, a "1" will be achieved at S_0 . The "1" at S_0 is then toggled to the Q output of FF0 by a signal from the toggling gate GT. The inherent delay of the flip-flops FSO prevents the S_0 signal of full adder FAO which is changing state as a result of the "1" applied to terminal B₀ from being conveyed to the Q terminal of flip-flop FFO.

If another A_0 pulse is then applied to FAO, the "1" at A_0 and the "1" at B_0 will add to produce a "0" at S_0 , but a "1" will appear at the carry terminal C_0 , thus indicating an accumulation of two credit increments. The indication of an accumulation of two credit increments is achieved by the C_0 "1" signal being added in the FA1 full adder to produce a "1" at S_1 . Subsequent operation of the accumulator by the insertion of A pulse inputs to the binary full adders will produce a continuous accumulation of the credit increments represented by the A pulses, up to a limit determined by the number of stages utilized.

When a customer makes a selection, the price of this selection must be subtracted from the accumulated credit in the accumulator. To achieve this function, subtraction is performed by complementary addition. In other words, due to the finite limits of the number of credit increments the counter can accumulate, the addition of a number that is the difference between the number to be subtracted and the total number of counts registerable will yield the same result as directly subtracting the number itself. Thus, if we assume that only four stages are utilized, the maximum number of counts registerable by the accumulator would be 15, although it is generally regarded as a 16-count counter, as it takes 16 counts to return to counter to its initial state. Assume that a credit of 10 credit increments has been accumulated and that a selection priced at four credit increments has been made. In the binary system, the 10 credit level would be represented as 1010. The result of that we wish to obtain (i.e., a remainder in the accumulator of six credit increments) will be expressed as 0110. The complement of the price (i.e., 16-4, or 12) will be written as 1100. Now if binary addition of the numbers 1010 and 1100 is performed, the result is 0110, the desired result. In calculating the complementary number in this arrangement, however, the total counts are taken as 15, since a carry pulse is always supplied by the debit logic when a subtract function is generated.

To achieve the subtraction effect by complementary addition, supplementary OR-gates G0', G1', G2', G3', Gn' are utilized to supply pulses to the binary full adders FA. Upon selection by a customer the price is applied to an appropriate OR-gate G0', G1', G2', G3', Gn' on an appropriate lead 39 or

41. A feedback from the last stage of the counter to the first stage is utilized to provide the necessary carry signal for complementary addition. As in the case of binary addition, toggling signals are obtained from toggling OR-gate GT. The toggling signals are obtained from line 39 or 41 and are applied to inputs 45 and 47 of OR-gate GT.

While a preferred embodiment of the invention to which this application is directed has been described, the operation thereof may be more completely understood by reference to FIGS. 2-4 which illustrate another embodiment of the credit accumulating circuit of this invention as incorporated in a pricing unit. This pricing unit has been especially designed for construction as a monolithic integrated circuit package. The relationship of the individual portions of the circuit illustrated in FIGS. 2-4 is depicted in FIG. 5.

The basic accumulator with which the bonus generating system is utilized comprises a plurality of stages with each stage including the combination of a binary full adder and a flip-flop circuit. Binary full adders 103, 105, 107, 109, and 111 are combined, respectively, with flip-flops 113, 115, 117, 119, and 121. The flip-flops are essentially the same as those previously discussed in connection with the basic credit accumulating system. The binary full adders are electronic devices that perform arithmetic binary addition, including a carry function to preserve multiple column veracity. In this invention, the full adder has been combined with a flip-flop circuit to provide arithmetic accumulation and subtraction of credit inputs.

Each of the binary full adders 103, 105, 107, 109, and 111 has three input terminals, the two primary input terminals A and B and the carry input terminal C. The basic output of the full adders is obtained at the terminal Z, while information regarding the credit must be carried over to the next page appears on terminal CO.

The Z terminal of each of the binary full adders is connected to the not set of terminal S of the associated flip-flop through an inverting amplifier 123. Further, each Z terminal is also connected directly by a lead 125 to the not reset terminal R of the associated flip-flop. Each of the binary full adders receives pulses representative to a specific credit increment on its A terminal through a delay element 127 and an inverting amplifier 129. Each of the credit increment inputs going to the binary full adders is also applied to a NAND-gate G10. The output 131 of NAND-gate G10 is connected to the CP terminals of the flip-flops through an inverting amplifier 133. The CP terminals of the flip-flops are those by which toggling of the flip-flop circuit is controlled. The output 131 of NAND-gate G10 is also connected to an input 135 of an AND-gate G11 through a delay element 137. Another input 139 of AND-gate G11 is connected to the CO terminal of full adder 111. Output 141 of AND-gate G11 is connected to the direct set terminals DS of the flip-flops 113, 115, 117, 119, and 121.

In operation, an input signal will be applied, for example, to the A terminal of binary full adder 103. Assuming that the circuit is in a quiescent state, the C and B terminals will each have a "0" thereon. A binary addition of the "1" appearing on terminal A with the "0" on terminals B and C results in the production of an output pulse "1" on terminal Z. The "1" of terminal Z is then conveyed to the S and R terminals of flip-flop 113, and the "1" on the R terminal and the "0" on the S terminal are toggled to the Q and Q terminals respectively upon energization of the CP terminal by the trailing edge of the applied pulse that is passed through NAND-gate G10 and inverting amplifier 133. Upon the application of another "1" to the same full adder, the "1" on the A and the "1" on the B terminals are added to produce a "0" on the Z terminal and a "1" on the CO terminal. Insertion of additional inputs representative of credit increments will be accumulated in the counter up to a maximum of 31 credit increments.

Each of the credit values that is inserted by a customer (e.g., nickels, dimes or quarters) is applied to the appropriate full adder stages to give the required credit increment information that is needed for accumulation. This feature may be better

comprehended by reference to FIG. 6, in which the production of pulses for conveyance to the full adders is illustrated. It should be noted that the delay elements 127 have been omitted for purposes of this discussion.

Credit information for the system is obtained from coin input switches S1-S4 and their respective one-shot circuits OS1-OS4. The switches S1-S4 will be actuated, for example, by a nickel, a dime, a quarter, and a half dollar respectively. Upon closure of any of the switches, a pulse is produced and shaped by the associated one-shot circuit and conveyed to an appropriate OR-gate G12-G16. The OR-gates G12-G16 are connected to the A terminals of full adders 103, 105, 107, 109, and 111 respectively. The connection of one-shot circuits OS1-OS4 to the OR-gates G12-G16 is dependent upon the number of credit increments that are represented by each of the full adder stages connected to the OR gates. The stage including binary full adder 103 is representative of one credit increment, the stage including full adder 105 is representative of two credit increments, the stage containing full adder 107 represents four credit increments, the stage including full adder 109 represents eight credit increments, and the stage including full adder 111 represents 16 credit increments. Therefore, to have the appropriate number of credit increments accumulated, the pulse from OS1 produced by a nickel would be applied to G12 to be conveyed to full adder 103, the two credit increments allocated to a dime would be produced by connecting OS2 to G13, the six credit increments allocated to a quarter would be accumulated by connecting one-shot OS3 to G13 and G14, and the 14 credits allocated to a half dollar would be realized by connecting OS4 to OR-gates G13, G14, and G15.

One difficulty that might be encountered in accumulating the credit values is that more credit might be deposited than can be represented by the 31 credit increment maximum of the accumulator. If enough credit were deposited to exceed the 31 credit increment maximum of the accumulator would merely start counting from zero again, so that the customer would be deprived of a major part of the credit actually due to him. To overcome this problem, an AND-gate G11 (FIG. 4) is provided. If the counter should reach its maximum of 31 accumulated credit increments, the CO terminal of binary full adder 111 would have a "1" thereon; and since NAND-gate G10 would always produce a "1" if a signal is present, a "1" would be placed on output 141 of AND-gate G11. The "1" on output 141 of AND-gate G11 would be connected to the direct set terminals DS of the flip-flops 113, 115, 117, 119, and 121 to lock out the trigger pulse supplied to the terminal CP and maintain the output terminal Q at a "1" state. Thus, the accumulator would be maintained in the maximum position of 31 counts, so that an over-depositor would at least be credited with the maximum amount that can be accumulated in the counter.

In determining whether enough credit has been deposited to permit a customer to have an article vended at a given price, it is necessary to detect the credit levels in the accumulator. Credit levels are checked at the Q terminals of the flip-flops, the Q signals being obtained from terminals 122. The circuit arrangements utilized for performing the credit level check is illustrated in FIG. 2 and involves the gates G17-G25. In the example illustrated there, it is desired to detect credit levels of one credit increment or greater, two credit increments or greater, three credit increments or greater, six credit increments or greater, 12 credit increments or greater, and 30 credit increments or greater. For purposes of obtaining this information, the output terminals Q of the flip-flops 113, 115, 117, 119, and 121 are utilized.

When it is desired to detect if one or more credit increments have been accumulated, the Q terminals of all of the flip-flops are connected to an OR-gate G17. In the case of detecting two credit increments or greater, the Q terminals of all flip-flops are connected to an OR-gate G18, with the exception of the Q terminal of flip-flop 113. When it is desired to detect three credit increments or greater, the Q terminals of flip-flops 113

and 115 are connected to the inputs of an AND-gate G19, the output of which is conveyed to an OR-gate G20, which also has as inputs the pulses appearing on the Q terminals of flip-flops 117, 119, and 121. To determine the existence of six credit increments or greater, the Q terminals of flip-flops 115 and 117 are connected to the inputs of an AND-gate G21, the output of which is connected to an OR-gate G22, along with the Q terminals of flip-flops 119 and 121. For twelve credit increments or greater, the Q terminals of flip-flops 117 and 119 are connected to the inputs of an AND-gate G23, the output of which is connected to an input of an OR-gate G24, along with the Q terminal of flip-flop 121. To detect credit increments of 30 or greater, the Q terminals of flip-flops 115, 117, 119, and 121 are connected to the inputs of an AND-gate G25.

To utilize the credit level detection arrangements, the desired credit level outputs are connected to AND gates such as G26 and G27 (FIG. 6). The other input to the AND gates would come from a selector switch and an associated one-shot circuit that would represent a debit pulse corresponding to the price of the article or serve selected. For example, assume that a single selection (in a coin-operated phonograph) is made to be played for two credit increments and that such choice is made by pressing selector switch S5. Closure of switch S5 would produce a pulse shaped by the one-shot circuit OS5 and conveyed to an input of gate G26. For the other input to G26 the output of OR-gate G18 would present a pulse if the accumulated credit had reached a level of two credit increments or greater. Thus, if sufficient credit has been deposited a pulse would appear at the output of gate G26.

The output of pulse would pass through an inverting amplifier 143 to selected OR gates from the gates G12-G16. The purpose of this pulse, of course, is to subtract from the accumulator the amount debited to the selection made by the customer.

In this system, subtraction is achieved by complementary addition. Thus, for a two credit increment selection, the complement (in this 31-count accumulator) would be 29 counts. Normally the complement would be calculated on the basis of the full 32 counts, but due to a carry signal always applied to the subtraction process the calculation is actually based on 31 counts. As may be seen in FIG. 6, the pulse passing through inverting amplifier 143 is connected to OR-gates G12, G14, G15, and G16, which produce a total of 29 credit increments to be added to the accumulator.

As another example, still with reference to a coin-operated phonograph, an album selection might be given a value of six credit increments. Thus, depression of selector switch S6 would produce, after passing through one-shot circuit OS6, a pulse at the input of gate G27, the other input to which would be taken from the output of OR-gate G22. If sufficient credit had been deposited, a pulse would appear at the output of gate G27 and be conveyed through inverting amplifier 145 to add a total of 25 credit increments to the accumulator, and thus actually subtract six credit increments from the accumulated value.

In addition to subtracting the number of credit increments allocated to the choice made by the customer, the outputs of the AND-gates G26 and G27 are also applied to an OR-gate G28 (FIG. 2) to perform additional functions. A signal in the output of gate G28 is applied, through line 147 and delay element 149, to the C terminal on binary full adder 103 to provide the carry signal needed during the subtract function. The signal at the output of G28 is also connected through inverting amplifier 151 and delay element 153 to an input 155 of AND-gate G11.

A reset signal on line 157 is passed through inverting amplifier 159 and applied to the direct reset terminals DR of flip-flops 113, 115, 117, 119, and 121.

The output of OR-gate G28 is also utilized to provide a reset for the bonus registering circuit on line 161 through inverting amplifier 163. Further, the signal at the output of OR-gate G28 is utilized to actuate a 50-millisecond one-shot circuit

165. One output of the one-shot circuit 165 is utilized to control the actuation of the vend motor and its associated elements, while another output 169 is connected to an input 171 of a NAND-gate G29. An input 173 of NAND-gate G29 is obtained from the input to AND-gate G26. The output of NAND-gate G29 is utilized to release a selector key that has been held depressed for the 50-millisecond period in order to permit a customer to finish making a selection.

FIG. 3 illustrates a bonus awarding circuit. The operation of this circuit is set forth in detail in an application entitled "Bonus Crediting System" now U.S. Pat. No. 3,548,387 filed in the name of Casimer J. Dabrowski concurrently herewith and assigned to the same assignee as the present invention.

To briefly summarize the operation of the bonus credit awarding circuit, credit increment representing pulses are applied to the bonus credit awarding circuit simultaneously with their application of the accumulator circuit. A series of logic gates and flip-flop circuits are utilized to accumulate the total credit registered before a vend is initiated and provide bonus credit awarding information if certain credit levels are reached. A clock circuit 187 is included to insure that bonus credit pulses are not applied to the circuit before coin switch pulses are completely removed, thus insuring that the benefit of the bonus credit is not lost.

It should be understood that the embodiments described are exemplary of the preferred practice of the present invention and that various changes, modifications, and variations may be made in the arrangements, details of construction, and operations of the elements disclosed herein, without departing from the spirit and scope of the present invention.

What is claimed is:

1. A credit-accumulating arrangement comprising:

credit input means actuated by the establishment of credit to produce a credit pulse on an associated input line, said credit pulse being representative of the credit increments allocated to the established credit;

a plurality of binary full adder circuits connected in series to produce a binary representation of accumulated credits, each of said full adder circuits having a pulse input, a feedback input, a carry input, a primary output, and a carry output;

means connecting the carry output of each of said full adder circuits to the carry input of the next succeeding full adder circuit;

switching means for simultaneously directing said credit pulse to the pulse inputs of selected ones of said full adder circuits;

a plurality of delay flip-flop circuits, each of said flip-flop circuits connected to feed back a binary signal on the primary output of an associated one of said full adder circuits to the feedback input thereof; and

toggle means connected to simultaneously energized all of said flip-flop circuits, after said full adder circuits have had time to respond to all input data, in order to simultaneously apply the binary signals on the primary outputs of all of said full adder circuits to the feedback inputs thereof to produce credit output signals, the primary output signals of said full adder circuits being utilized for accumulated credit information only at the time said toggle means are actuated.

2. A credit-accumulating arrangement as claimed in claim 1 and further comprising a plurality of OR gates, each OR gate connected to the pulse input of a corresponding one of said full adder circuits, said input line being connected to selected ones of said OR gates by said switching means.

3. A credit-accumulating arrangement as claimed in claim 1 wherein said toggle means comprises circuit elements adapted to simultaneously apply the trailing edge of said credit pulse to all of said flip-flop circuits to cause the binary signal on the primary output of each of said full adder circuits to be conveyed from an input of the associated flip-flop circuit to an output thereof.

4. A credit-accumulating arrangement as claimed in claim 1 and further comprising credit level detection means for determining the amount of credit accumulated in said full adder circuits.

5. A credit-accumulating arrangement as claimed in claim 1 and further comprising debit logic circuitry adapted to compare a credit accumulated in said full adder circuits with the price of an article selected to be vended and to initiate subtraction of the price of said article from the accumulated credit in said full adder circuits upon vending thereof.

6. An accumulating arrangement comprising:

a plurality of binary full adder circuits connected in series, each of said full adder circuits having a pulse input, a feedback input, a carry input, a primary output, and a carry output;

input means simultaneously applying input pulses to the pulse inputs of selected ones of said full adder circuits;

a memory circuit connected between the primary output and feedback input of each of said full adder circuits; and

transfer means adapted to simultaneously actuate all of said memory circuits after said full adder circuits have had time to respond to all input data to simultaneously apply the binary signal on the primary output of each of said full adder circuits to the feedback input thereof to produce credit output signals representative to the states of said full adder circuits only at the time said transfer means are actuated,

whereby the input pulses applied to said full adder circuits are accumulated by essentially simultaneous operation of all full adder circuits to which input pulses are applied at a given time.

7. An accumulating arrangement as claimed in claim 6 wherein each of said memory circuits comprises a flip-flop circuit having an input terminal connected to the primary output of the associated full adder circuit, an output terminal connected to the feedback input of the associated full adder circuit, and a toggle terminal connected to said transfer means.

8. An accumulating arrangement as claimed in claim 7 wherein said transfer means comprises circuit elements adapted to convert the trailing edge of each input pulse into a toggle signal which is simultaneously applied to the toggle terminal of each of said flip-flop circuit to transfer the binary signal on the input terminal thereof to the output terminal thereof.

9. An accumulating arrangement as claimed in claim 6 wherein the carry output of each of said full adder circuits, except for the last full adder circuit in said series of full adder circuits, is connected to the carry input of the next succeeding full adder circuit.

10. An accumulating arrangement as claimed in claim 9 and further comprising retaining means for maintaining said memory circuits in their existing condition upon production of a signal at the carry output of said last full adder circuit.

11. A credit-accumulating arrangement for use in a vending machine comprising:

a plurality of binary full adder circuits connected in series, each of said full adder circuits having a pulse input, a feedback input, a carry input, a primary output, and a carry output, the carry output of all but the last of said full adder circuits being connected to the carry input of the next succeeding one of said full adder circuits;

a plurality of coin switches, each coin switch adapted to produce a credit pulse on an associated input line in response to deposit of a corresponding coin in the vending machine;

credit switching means connecting each of said input lines to the pulse inputs of selected ones of said full adder circuits to simultaneously apply a credit pulse appearing on an input line to all of the full adder circuits selected for that input line;

a plurality of flip-flop circuits, each of said flip-flop circuits having an input terminal, an output terminal, and a toggle terminal, the input and output terminals of each of said

flip-flop circuits connected, respectively, to the primary output in feedback input of an associated one of said full adder circuits; and

toggle means producing a toggle pulse from the trailing edge of each credit pulse, each toggle pulse being simultaneously applied to the toggle terminal of all of said flip-flop circuits to simultaneously apply the signal at the primary output of each full adder circuit to the feedback input thereof to produce credit output signals representative of the state of said full adder circuits only at the time said toggle means is actuated.

12. A credit-accumulating arrangement as claimed in claim 11 and further comprising:

selecting switches providing pricing signals representative of the price of an item selected for vending;

level detection means providing accumulated credit signals indicative of the credit accumulated in said full adder circuits;

comparing means for producing a debit pulse in response to the application of a predetermined pricing signal and a predetermined accumulated credit signal thereto to initiate vending of a selected item; and

debit switching means applying each debit pulse to selected ones of said full adder circuits to cause subtraction of credits corresponding to the price of the item being vended,

whereby an item is vended and the price thereof is subtracted from the credits accumulated in said full adder circuits.

13. A credit-accumulating arrangement as claimed in claim 12 wherein said debit switching means connects the debit pulses to selected full adder circuits representing an arithmetical sum of credit increments which is the complement of the arithmetical sum of the credit increments allocated to the debit pulses in order to produce subtraction by complementary addition.

14. A credit-accumulating arrangement as claimed in claim 12 wherein said comparing means comprises a first AND gate.

15. A credit-accumulating arrangement as claimed in claim 12 wherein said level detection means comprises OR gates and AND gates appropriately connected to the output terminals of said flip-flop circuits.

16. A credit-accumulating arrangement as claimed in claim 12 wherein said credit switching means and said debit switching means each comprises a set of manually actuatable switches.

17. A credit-accumulating arrangement as claimed in claim 12 wherein said toggle means comprises a NAND gate receiving an input from each of said input lines and an inverting amplifier connected between the output of said NAND gate and the toggle terminals of said flip-flop circuits.

18. A credit-accumulating arrangement as claimed in claim 17 and further comprising:

a set terminal on each of said flip-flop circuits; and

a second AND gate receiving inputs from said comparing means, from said NAND gate, and from the carry output of the last full adder circuit in said series of full adder circuits, the output of said second AND gate being connected to the set terminals of said flip-flop circuits,

whereby said flip-flop circuits are maintained in the maximum credit state upon production of a signal on the carry output of said last full adder circuit until a debit pulse is produced by said comparing means.

19. A credit-accumulating arrangement comprising:

supply means for producing upon actuation thereof pulses representative of selected credit increments;

a counter circuit having a plurality of stages;

directing means connecting the pulses produced by said supply means to appropriate ones of said counter stages;

a plurality of memory devices, each of said memory devices adapted upon actuation thereof to store a signal representing the state of an associated counter stage; and

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retaining means for maintaining each of said memory devices in its existing condition when said counter circuit registers a full count.

20. A credit-accumulating arrangement as claimed in claim 19 wherein:

each of said counter circuit stages comprises a binary full adder circuit having a pulse input, a feedback input, a carry input, a primary output, and a carry output; and each of said memory devices comprises a flip-flop circuit having an input terminal, an output terminal, and a set terminal.

21. A credit-accumulating arrangement as claimed in claim 20 wherein said retaining means comprises an AND gate

receiving inputs from said supply means and the carry output of the last full adder stage in said counter circuit, the output of said AND gate being connected to the set terminals of said flip-flop circuits, whereby said flip-flop circuits are maintained in the maximum credit state upon production of a signal on the carry output of said last full adder circuit.

22. A credit-accumulating arrangement as claimed in claim 21 and further comprising another input to said AND gate to render said AND gate inoperative to set the said flip-flop circuits upon the deduction of credit from the credit-accumulating arrangement.

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