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(54) **Title**: VERTICAL-CAVITY SURFACE-EMITTING LASER SYSTEM AND METHOD FOR FABRICATING THE SAME

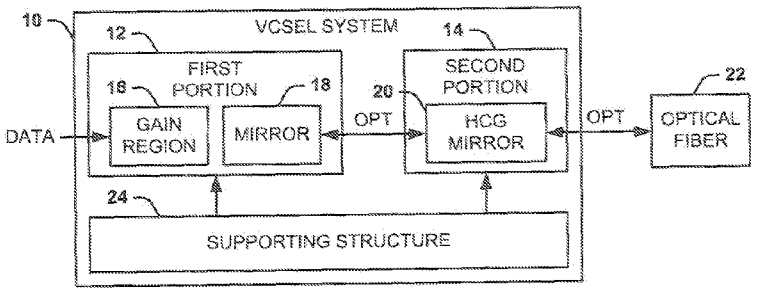


FIG. 1

(57) **Abstract**: A vertical cavity surface emitting laser (VCSEL) system (10) and method (750) of fabrication are included. The VCSEL system (10) includes a first portion (12) comprising a first mirror (18) and a gain region (16) to amplify an optical signal in response to a data signal, the first portion (12) being fabricated on a first wafer. The system (10) also includes a second portion (14) comprising a second mirror (20) that is partially-reflective to couple the optical signal to an optical fiber (22). The second portion (14) can be fabricated on a second wafer (152). The system (10) further includes a supporting structure (24) to couple the first and second portions (12, 14) such that the first and second mirrors (18, 20) are arranged as a laser cavity having a predetermined length to resonate the optical signal.

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TITLE: VERTICAL-CAVITY SURFACE-EMITTING LASER SYSTEM AND METHOD FOR FABRICATING THE SAME

BACKGROUND

[0001] A vertical-cavity surface-emitting laser (VCSEL) is a type of semiconductor laser diode with laser beam emission perpendicular from a top surface. VCSELs differ from other types of edge-emitting semiconductor lasers that emit laser beams from surfaces formed by cleaving an individual chip out of a wafer. The perpendicular emission of the laser from a VCSEL allows a VCSEL to be tested at various stages throughout the fabrication process to check for material quality and processing issues, unlike edge-emitting lasers that cannot be tested until the end of a production process. Thus, if an edge-emitting laser does not work at the end of the fabrication process, the production time and the processing materials have been wasted.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] FIG. 1 illustrates an example of a VCSEL system.

[0003] FIG. 2 illustrates an example of a cross-sectional view of a VCSEL system.

[0004] FIG. 3 illustrates an example of a first portion of the VCSEL system of FIG. 2.

[0005] FIG. 4 illustrates an example diagram of a cross-sectional view of an SOI structure including a photoresist layer.

[0006] FIG. 5 illustrates an example diagram of the SOI structure of FIG. 4 with the photoresist layer having been patterned.

[0007] FIG. 6 illustrates an example diagram of the SOI structure of FIG. 5 undergoing an etching step.

[0008] FIG. 7 illustrates an example diagram of the SOI structure of FIG. 6 after the etching step is substantially complete.

[0009] FIG. 8 illustrates an example diagram of a top view of the SOI structure of FIG. 7.

[0010] FIG. 9 illustrates an example diagram of a cross-sectional view of the SOI structure of FIG. 7 with a photoresist layer.

[0011] FIG. 10 illustrates an example diagram of the SOI structure of FIG. 9 with the photoresist layer having been patterned.

[0012] FIG. 11 illustrates an example diagram of the SOI structure of FIG. 10 undergoing an etching step.

[0013] FIG. 12 illustrates an example diagram of the SOI structure of FIG. 11 after the etching step is substantially complete.

[0014] FIG. 13 illustrates an example diagram of a top view of the SOI structure of FIG. 12.

[0015] FIG. 14 illustrates an example diagram of a cross-sectional view of the SOI structure of FIG. 12 being coupled with an optical fiber.

[0016] FIG. 15 illustrates an example of a VCSEL system array.

[0017] FIG. 16 illustrates an example of a method for fabricating a VCSEL system.

DETAILED DESCRIPTION

[0018] FIG. 1 illustrates an example of a vertical-cavity surface-emitting laser (VCSEL) system 10. The VCSEL system 10 can be implemented in a variety of optical applications, such as optical computing and communications. The VCSEL system 10 includes a first portion 12 and a second portion 14. In the example of FIG. 1, the first portion 12 includes a gain region 16 that is configured to generate an optical signal (OPT) in response to a signal (DATA). As an example, the signal (DATA) could be an RF baseband data signal. The first portion 12 also includes a mirror 18. As an example, the mirror 18 can be configured as a multi-layer n-doped distributed Bragg reflector (n-DBR).

[0019] The second portion 14 includes a high-contrast grating (HCG) mirror 20. The HCG mirror 20 can be configured as a partially-reflective mirror (*e.g.*, approximately 98% reflective), such that the mirror 18 and the HCG mirror 20 can cooperate to form a laser cavity to resonate the optical signal (OPT). Thus, a portion of the optical signal (OPT) can be emitted from the laser cavity and launched into an optical fiber 22. For example, the optical fiber 22 can be substantially aligned with the HCG mirror 20 based on the fabrication of the second portion 14, as described herein. As an example, the optical fiber 22 can be a single-mode fiber, such as to propagate the optical signal (OPT) for processing at a destination or as part of a

multiplexed optical signal, such as based on launching the optical signal (OPT) into a multimode fiber.

[0020] As an example, the first and second portions 12 and 14 can be fabricated from separate semiconductor wafers. For example, the first portion 12 can merely be fabricated as a VCSEL without an associated second mirror (*e.g.*, HCG mirror). However, the second portion 14 can be fabricated from a separate silicon-on-insulator (SOI) wafer, such as including two layers of silicon (Si) separated by an insulator (*e.g.*, SiO_2). As an example, the second portion 14 can be fabricated such that the HCG mirror 20 can be patterned onto one of the layers of silicon of the SOI wafer and the other layer of silicon can be etched to receive the optical fiber 22, such that the HCG mirror 20 can be substantially aligned with the optical fiber 22. As a result, the optical signal (OPT) can be easily coupled into the optical fiber 22 to provide a much more precise output mode of the optical signal (OPT) as launched into the optical fiber 22.

[0021] Therefore, because the first and second portions 12 and 14 are fabricated from separate wafers, the first and second portions 12 and 14 can be arranged as separate and independent pieces. Thus, the VCSEL system 10 further includes a supporting structure 24 that is configured to couple the first and second portions 12 and 14 such that the HCG mirror 20 can be substantially aligned with the mirror 18 to form the laser cavity. As an example the supporting structure 24 can include a non-etched portion of the wafer from which the first portion 12 is fabricated, such as bonded to both the first and second portions 12 and 14. Thus, the supporting structure 24 can be easily adjusted, such that the lasing wavelength of the optical signal (OPT) can be easily tuned based on a length of the laser cavity. Accordingly, the VCSEL system 10 can provide numerous advantages over typical monolithic VCSEL systems.

[0022] FIG. 2 illustrates an example of a cross-sectional view of a VCSEL system 50. The VCSEL system 50 can correspond to the VCSEL system 10 in the example of FIG. 1. Therefore, reference is to be made to the example of FIG. 1 in the following description of the example of FIG. 2.

[0023] The VCSEL system 50 demonstrates the first portion 12 and the second portion 14 of the VCSEL system 50. As described above, the first and second portions 12 and 14 can be fabricated separately from separate wafers. The

first portion 12 includes a p-contact region 52 and an n-contact region 54 that act as contacts of a diode through which the signal (DATA) passes to generate the optical signal (OPT). The n-contact region 54 is covered by a substrate layer 56. As an example, the substrate layer 56 can be an N-doped gallium arsenide (GaAs) layer. The first portion 12 also includes a multi-layer n-doped DBR 58 that acts as an approximately 100% reflective mirror. The n-doped DBR 58 can thus correspond to the mirror 18 in the VCSEL system 10 in the example of FIG. 1.

[0024] The first portion 12 also includes a silicon nitride (SiN) passivation layer 60 and a polyimide 62 that substantially surround a GaAs multiple quantum well (MQW) 64. The MQW 64 acts as a gain region for the signal (DATA) to generate the optical signal (OPT). The optical signal (OPT) is thus generated at the MQW 64 and reflected from the n-doped DBR 58 to be emitted from an aperture 66 in an oxide layer 68. In the example of FIG. 2, the optical signal (OPT) is shown at 70. The first portion 12 can be coupled to the second portion 14 by a supporting structure (not shown), such as the supporting structure 24 in the example of FIG. 1, to suspend the second portion 14 over the first portion 12 by a predetermined amount.

[0025] As described in greater detail below, the second portion 14 can be fabricated from an SOI structure. Specifically, the second portion 14 includes a first silicon layer 72 that is separated from the aperture 66 by a distance L. The distance L can be adjusted based on the supporting structure 24 to tune the lasing wavelength of the optical signal (OPT). The first silicon layer 72 can include an etched pattern 74 that can form an HCG mirror 76. The etched pattern 74 can include sub-wavelength etchings into the first silicon layer 72, such as holes, grooves, and/or posts, such that the HCG mirror 76 can be partially-reflective (*e.g.*, 98%). Therefore, the n-doped DBR 58 and the HCG mirror 76 cooperate to act as a laser cavity to resonate the optical signal (OPT). In addition, the HCG mirror 76 can be patterned in a manner to control the shape of the optical signal (OPT) to simulate a curved mirror, such that the optical signal (OPT) is focused into the aperture 66 upon being reflected from the HCG mirror 76. Furthermore, the patterning of the HCG mirror 76 can tune the lasing wavelength of the optical signal (OPT).

[0026] The second portion 14 also includes an insulator layer 78, which can be a glass layer such as SiO_2. Thus, the insulator layer 78 can be selected to have approximately 0% reflectivity. The insulator layer 78 separates the first silicon layer

72 from a second silicon layer 80. The second silicon layer 80 can be fabricated to have a hole etched down to the insulator layer 78, with the hole being etched at approximately the same location as the HCG mirror 76 on the opposite surface of the insulator layer 78. Thus, the optical fiber 22 can be received in the hole in the second silicon layer 80. The hole in the second silicon layer 80 can be etched to have an inside diameter (ID) that is approximately equal to an outside diameter (OD) of the optical fiber 22, such that the core of the optical fiber 22 can be substantially aligned with the HCG mirror 76. As a result, unreflected energy of the optical signal (OPT) can pass through the HCG mirror 76 to be launched directly into the optical fiber 22.

[0027] As an example, the optical fiber 22 can include a single mode core 82, such that the optical fiber 22 can be a single mode fiber. Thus, because the single mode core 82 of the optical signal 22 can be substantially aligned with the HCG mirror 76, the optical signal (OPT) can be coupled into the optical fiber 22 to provide a much more precise output mode of the optical signal (OPT) when launched into the optical fiber 22. In addition, as demonstrated in the example of FIG. 2, the HCG mirror 76 is fabricated such that it is a layer that is coupled to the insulator layer 78, as opposed to being suspended over the aperture 66 via being coupled to the p-contact 52, such as occurring in typical VCSEL systems. Therefore, the laser cavity formed by the n-doped DBR 58 and the HCG mirror 76 experiences much greater spatial stability than in typical VCSEL systems.

[0028] Fabrication of the VCSEL system 50 will now be described. In the following description of the examples of FIGS. 3-14, reference is to be made and like reference numbers are made to the example of FIG. 2.

[0029] FIG. 3 illustrates an example diagram 100 of the first portion 12 of the VCSEL system 50 of FIG. 2. The first portion 12 can be fabricated in a variety of manners to include the p-contact region and n-contact regions 52 and 54, the substrate layer 56, and the multi-layer n-doped DBR 58. In addition, the first portion 100 can be fabricated to include the SiN passivation layer 60, the polyimide 62, and the GaAs MQW 64. Therefore, the first portion 12 can be fabricated such that the first portion 100 is grown as a high-speed oxide-confined VCSEL portion, such that the first portion 12 includes a gain region (e.g., the MQW 64) to generate the optical

signal (OPT) and a mirror (*e.g.*, the n-doped DBR 58) to act as part of a laser cavity to resonate the optical signal (OPT).

[0030] FIG. 4 illustrates an example of a cross-sectional view diagram 150 of an SOI structure 152 including a photoresist layer 154. The SOI structure 152 is demonstrated in the example of FIG. 4 as a portion of an inverted SOI wafer that includes the first silicon layer 72, the insulator layer 78, and the second silicon layer 80, which can act as a substrate during fabrication of the SOI structure 152. As an example, the SOI structure 152 can be formed via a Separation by Implantation of Oxygen (SIMOX) process. The basic steps of the SIMOX process can include implanting oxygen beneath the surface of a silicon wafer. A high temperature annealing step can next be performed to coalesce the implanted oxygen atoms into a uniform layer of SiO_2. The annealing step can typically be performed at temperatures greater than 1250° C for several hours to coalesce the implanted oxygen and achieve solid state recrystallization of the second silicon layer 80 from the surface downward. Thus, as an example, the second silicon layer 80 can be grown to have a thickness of approximately 500 μm.

[0031] The SOI structure 152 is also illustrated as including the photoresist layer 154 formed on the second silicon layer 80. The photoresist layer 154 can have a thickness of about 500 Å - 5000 Å. However, it is to be appreciated that the thickness thereof may be of any dimension suitable for fabricating the second portion 14. Accordingly, the thickness of the photoresist layer 154 can vary in correspondence with the wavelength of radiation used to pattern the photoresist layer 154. The photoresist layer 154 may be formed over the second silicon layer 80 via conventional spin-coating or spin casting deposition techniques.

[0032] FIG. 5 illustrates an example diagram 200 of the SOI structure 152 of FIG. 4 with the photoresist layer 154 having been patterned. Specifically, photoresist layer 154 is patterned using conventional techniques to form a hole having an ID that is approximately equal to the OD of the optical fiber 22. As an example, the hole ID can be approximately 125 μm. The patterned photoresist layer 154 can thus serve as an etch mask layer for processing or etching the underlying second silicon layer 80.

[0033] FIG. 6 illustrates an example diagram 250 of the SOI structure 152 of FIG. 5 undergoing an etching step. The etch can be an anisotropic deep reactive ion etching (DRIE), as indicated by the arrows 252. Any suitable DRIE etch technique

may be used to etch the second silicon layer 80. For example, the second silicon layer 80 can be anisotropically etched with one or more plasma gases, such as carbon tetrafloride (CF_4) containing fluorine ions, in a commercially available etcher, such as a parallel plate DRIE apparatus or, alternatively, an electron cyclotron resonance (ECR) plasma reactor to replicate the mask pattern of the patterned photoresist layer 154.

[0034] FIG. 7 illustrates an example diagram 300 of the SOI structure 152 of FIG. 6 after the etching step is substantially complete. Specifically, the diagram 300 illustrates a partially complete SOI structure 152 after a stripping step (*e.g.*, ashing in an O_2 plasma) is substantially complete to remove remaining portions of the patterned photoresist layer 154. Therefore, the SOI structure 152 includes a hole 302 that has been etched via the DRIE etch process of the example of FIG. 6 in the second silicon layer 80. The DRIE etch process is thus demonstrated in the example of FIG. 7 as having etched the second silicon layer 80 completely down to the insulator layer 78, such that the hole can have a depth of approximately 500 μm. FIG. 8 illustrates an example diagram 350 of a top view of the SOI structure 152 of FIG. 7. In the example of FIG. 8, the hole 302 is demonstrated as having a substantially round dimension. However, it is to be understood that the hole 302 could have a variety of types of dimensions, such as being rectangular, oval, or irregular.

[0035] FIG. 9 illustrates an example diagram 400 of a cross-sectional view of the SOI structure 152 of FIG. 7 with a photoresist layer 402. In the example of FIG. 9, the SOI structure 152 is demonstrated as having been inverted, such as that the SOI structure 152 is demonstrated as upside-down relative to as demonstrated in the examples of FIGS. 4-8, and thus oriented the same as a typical SOI wafer. The SOI structure 152 thus still includes the first silicon layer 72, the insulator layer 78, and the second silicon layer 80. The SOI structure 152 is also illustrated as including the photoresist layer 402 formed on the first silicon layer 72. The photoresist layer 402 can have a thickness suitable for fabricating the second portion 14 (*e.g.*, about 500 Å - 5000 Å), such as based on the wavelength of radiation used to pattern the photoresist layer 402. The photoresist layer 402 may be formed over the first silicon layer 72 via conventional spin-coating or spin casting deposition techniques.

[0036] FIG. 10 illustrates an example diagram 450 of the SOI structure 152 of FIG. 9 with the photoresist layer 402 having been patterned. Specifically, photoresist layer 154 is patterned using conventional techniques to form a plurality of openings 452. The patterned photoresist layer 402 can thus serve as an etch mask layer for processing or etching the underlying first silicon layer 72 to form sub-wavelength etchings that act as a partially-reflective grating.

[0037] FIG. 11 illustrates an example diagram 500 of the SOI structure 152 of FIG. 10 undergoing an etching step. The etch can be an anisotropic DRIE etch, as indicated by the arrows 502. Any suitable DRIE etch technique may be used to etch the first silicon layer 72. For example, the first silicon layer 72 can be anisotropically etched with one or more plasma gases, such as carbon tetrafloride (CF_4) containing fluorine ions, in a commercially available etcher, such as a parallel plate DRIE apparatus or, alternatively, an electron cyclotron resonance (ECR) plasma reactor to replicate the mask pattern of the patterned photoresist layer 402. However, it is to be understood that other etching techniques can be implemented in the etching step described in the example of FIG. 11.

[0038] FIG. 12 illustrates an example diagram 550 of the SOI structure 152 of FIG. 11 after the etching step is substantially complete. Specifically, the diagram 550 illustrates a view of the complete second portion 14 after a stripping step is substantially complete to remove remaining portions of the patterned photoresist layer 402. Therefore, the SOI structure 152 includes an etched pattern 552 that have been etched via the DRIE etch process of the example of FIG. 11 in the first silicon layer 72 corresponding to the openings 452 that were patterned into the photoresist layer 402 (*e.g.*, to form a grating). Thus, the etching of the openings 552 corresponds to the patterning of the HCG mirror 76 on the first silicon layer 72. FIG. 13 illustrates an example diagram 600 of a top view of the SOI structure 152 of FIG. 12. In the example of FIG. 13, the openings 552 constituting the HCG grating 76 are demonstrated as being substantially centered with the hole 302 and are substantially enclosed in a circular outer diameter that is concentric with the hole 302.

[0039] FIG. 14 illustrates an example diagram 650 of a cross-sectional view of the second portion 14 of FIG. 12 being coupled with the optical fiber 22. The optical fiber 22 is received within the hole 302, such that the OD of the optical fiber 22 is substantially flush with the ID of the hole 302. The optical fiber 22 can then be butt-

coupled directly to the insulator layer 78. As a result, the single-mode core 82 is substantially aligned with the HCG mirror 76 formed by the openings 552 on the opposite surface. Accordingly, the supporting structure 22 can suspend the completed second portion 14 over the first portion 12, such that the optical signal (OPT) can be resonated by the n-doped DBR 58 and the HCG mirror 76 and launched into the optical fiber 22.

[0040] FIG. 15 illustrates an example of a VCSEL system array 700. The VCSEL array system 700 includes an array 702 of VCSEL systems 704, numbered in the example of FIG. 15 from 1 to N, where N is a positive integer greater than one. Each of the VCSEL systems 704 can be configured substantially similar to the VCSEL system 50 in the example of FIG. 2. As an example, each of the VCSEL systems 704 can include a first portion and a second portion that are each fabricated from separate wafers. More specifically, all of the first portions of the VCSEL systems 704 can be fabricated from a single wafer and all of the second portions of the VCSEL systems 704 can be fabricated from a separate single wafer, such as an SOI wafer.

[0041] Each of the VCSEL systems 704 generates a respective optical signal, demonstrated as optical signals OPT_1 through OPT_N in the example of FIG. 15, that are launched into respective single mode optical fibers 706, respectively numbered 1 through N. Each of the single mode optical fibers 706 can be coupled to each of the respective VCSEL systems 704 in a manner similar to the coupling of the optical fiber 22 to the second portion 14, similar to as demonstrated in the example of FIG. 14 in which the optical fiber 22 has an OD that is approximately the same as the ID of the etched hole in the second silicon layer 80. Therefore, the single mode optical fibers 706 are each substantially aligned with the laser cavities of the VCSEL systems 704, such that the optical signals OPT_1 through OPT_N are directly coupled into the single mode optical fibers 706. The optical signals OPT_1 through OPT_N can then propagate through the respective single mode optical fibers 706 and be collectively launched into a multi-mode fiber 708 having a multi-mode core. As a result, the optical signals OPT_1 through OPT_N can be multiplexed, such as wavelength division multiplexed, polarization multiplexed, and/or time-division multiplexed, within the multi-mode fiber 708.

[0042] In view of the foregoing structural and functional features described above, an example method will be better appreciated with reference to FIG. 16. While, for purposes of simplicity of explanation, the method of FIG. 16 is shown and described as executing serially, it is to be understood and appreciated that the method is not limited by the illustrated order, as parts of the method could occur in different orders and/or concurrently from that shown and described herein.

[0043] FIG. 16 illustrates an example of a method 750 for capturing a photograph of a subject. At 752, an SOI structure having a first silicon layer, an insulator layer over the first silicon layer, and a second silicon layer over the insulator layer is provided. At 754, a hole is formed in the first silicon layer, the hole being dimensioned to receive an optical fiber. At 756, a partially-reflective high-contrast grating (HCG) mirror is patterned in the second silicon layer, the partially-reflective HCG mirror in the second silicon layer being substantially aligned with the hole in the first silicon layer. At 758, a VCSEL structure is provided to generate an optical signal, the VCSEL structure comprising a mirror. At 760, the SOI structure is coupled to the VCSEL structure such that the mirror and the partially-reflective mirror are arranged as a laser cavity having a predetermined length to resonate the optical signal

[0044] What have been described above are examples. It is, of course, not possible to describe every conceivable combination of components or methodologies, but one of ordinary skill in the art will recognize that many further combinations and permutations are possible. Accordingly, the invention is intended to embrace all such alterations, modifications, and variations that fall within the scope of this application, including the appended claims. Additionally, where the disclosure or claims recite "a," "an," "a first," or "another" element, or the equivalent thereof, it should be interpreted to include one or more than one such element, neither requiring nor excluding two or more such elements.

CLAIMS

What is claimed is:

1. A vertical cavity surface emitting laser (VCSEL) system (10) comprising:

a first portion (12) comprising a first mirror (18) and a gain region (16) to amplify an optical signal in response to a data signal, the first portion (12) being fabricated on a first wafer;

a second portion (14) comprising a second mirror (20) that is partially-reflective to couple the optical signal to an optical fiber (22), the second portion (14) being fabricated on a second wafer; and

a supporting structure (24) to couple the first and second portions (12, 14) such that the first and second mirrors (18, 20) are arranged as a laser cavity having a predetermined length to resonate the optical signal.

2. The system of claim 1, wherein the second wafer is a silicon-on-insulator (SOI) wafer (152) comprising a first silicon layer (72), an insulator layer (78) over the first silicon layer (72), and a second silicon layer (80) over the insulator layer (78).

3. The system of claim 2, wherein the second mirror comprises a high-contrast grating (HCG) mirror (76) that is patterned on the first silicon layer (72).

4. The system of claim 3, wherein the first portion (12) comprises an aperture (66) through which the optical signal resonates between the first and second mirrors (18, 76), the HCG mirror (76) focusing the optical signal through the aperture (66).

5. The system of claim 3, wherein a lasing wavelength of the optical signal is determined based on at least one of a mirror phase of the HCG mirror (76) and the predetermined length of the laser cavity.

6. The system of claim 1, wherein the second portion (14) comprises a hole (302) etched in a silicon layer (80) on a first surface of the second portion (14), the hole (302) being substantially aligned with the second mirror (20) on a second surface of the second portion (14) opposite the first surface.

7. The system of claim 6, wherein the hole (302) receives the optical fiber (22), such that the optical fiber (22) is substantially aligned with the second mirror (20).

8. A laser array (702) comprising a plurality of the VCSEL systems (704) of claim 1, each of the plurality of VCSEL systems (704) generating respective optical signals that are launched into a multi-mode optical fiber (708).

9. A method (750) for fabricating a vertical cavity surface emitting laser (VCSEL) system (10), the method comprising:

providing a silicon-on-insulator (SOI) structure (152) having a first silicon layer (80), an insulator layer (74) over the first silicon layer (80), and a second silicon layer (72) over the insulator layer (78);

forming a hole (302) in the first silicon layer (80), the hole (302) being dimensioned to receive an optical fiber (22) subsequent to fabrication;

patterning a partially-reflective high-contrast grating (HCG) mirror (76) in the second silicon layer (72), the partially-reflective HCG mirror (76) in the second silicon layer (72) being substantially aligned with the hole (302) in the first silicon layer (80);

providing a VCSEL structure (12) that amplifies an optical signal, the VCSEL structure (12) comprising a mirror (18); and

coupling the SOI structure (152) to the VCSEL structure (12) such that the mirror (18) and the partially-reflective HCG mirror (76) are arranged as a laser cavity having a predetermined length to resonate the optical signal.

10. The method of claim 9, wherein forming the hole (302) in the first silicon layer (80) comprises:

patterning a photoresist material (154) to form a mask for the hole (302); and

performing a reactive-ion etch (252) to form the hole (302) in the first silicon layer (80).

11. The method of claim 9, wherein patterning the partially-reflective HCG mirror (76) in the second silicon layer (72) comprises:

patterning a photoresist material (402) to form a mask (452) for the partially-reflective HCG mirror (76); and

performing a reactive-ion etch (502) to form the partially-reflective HCG mirror (76) in the first silicon layer (72).

12. The method of claim 9, further comprising selecting the predetermined length of the laser cavity to tune a lasing wavelength of the optical signal.

13. The method of claim 9, wherein patterning the partially-reflective HCG mirror (76) comprises tuning the lasing wavelength of the optical signal based on the mask (452) for the partially-reflective HCG mirror (76).

14. The method of claim 9, wherein providing the VCSEL structure (12) comprises providing the VCSEL structure (12) having an aperture (66) in an oxide layer (68) through which the partially-reflective HCG mirror (76) focuses the optical signal to resonate the optical signal between the mirror (18) and the partially-reflective HCG mirror (76).

15. The method of claim 9, wherein forming the hole (302) in the first silicon layer (80) comprises forming the hole (302) to have an inner diameter (ID) that is approximately equal to an outer diameter (OD) of the optical fiber (22), such that the optical fiber (22) is substantially aligned with the partially-reflective HCG mirror (76) upon being received in the hole (302) in the first silicon layer (80).

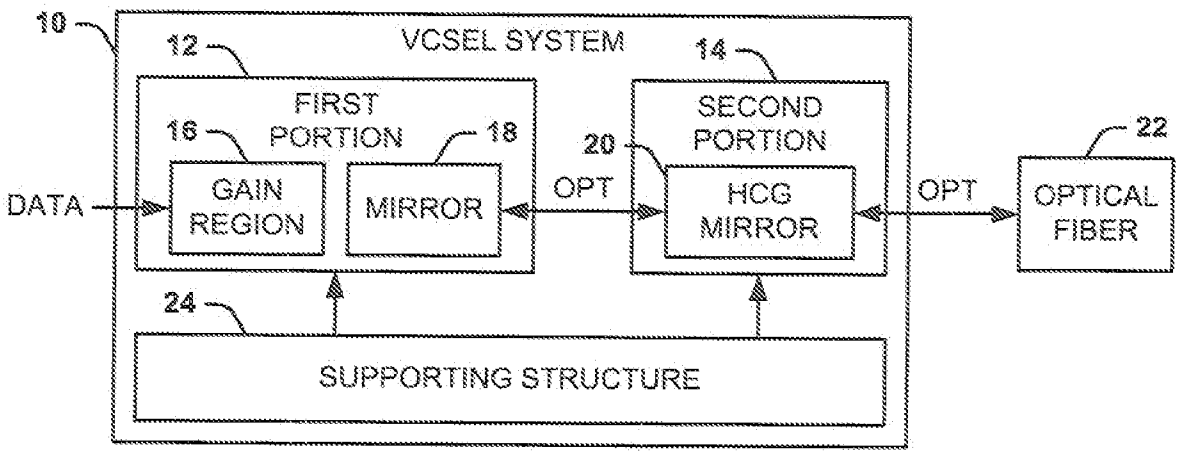

10
12
VCSEL SYSTEM
14
FIRST PORTION
16
18
SECOND PORTION
20
22
DATA
GAIN REGION
MIRROR
OPT
HCG MIRROR
OPT
OPTICAL FIBER
24
SUPPORTING STRUCTURE

FIG. 1

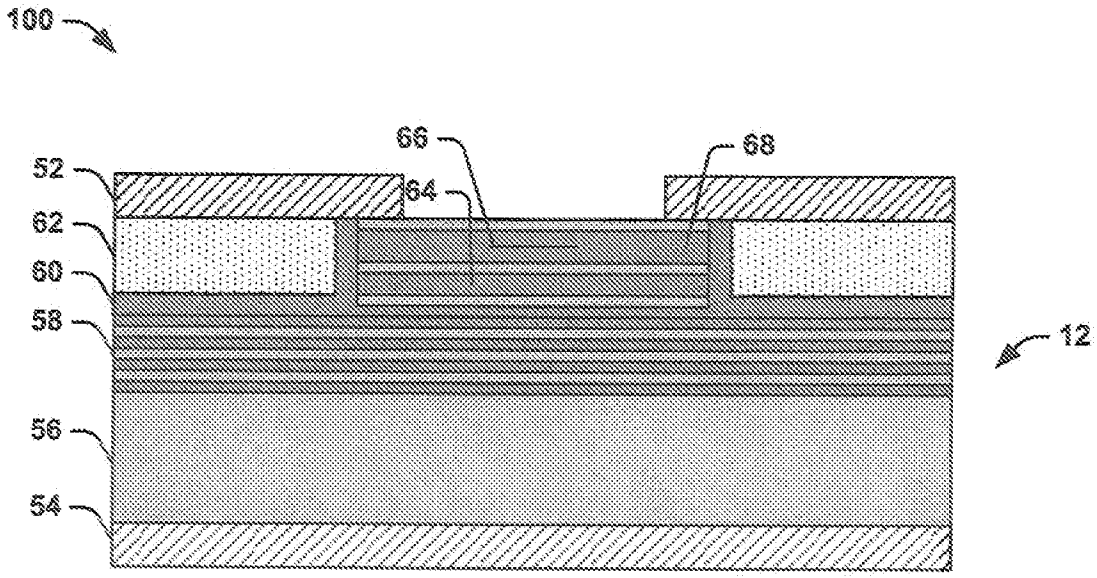

100
66
68
52
64
62
60
58
12
56
54

FIG. 3

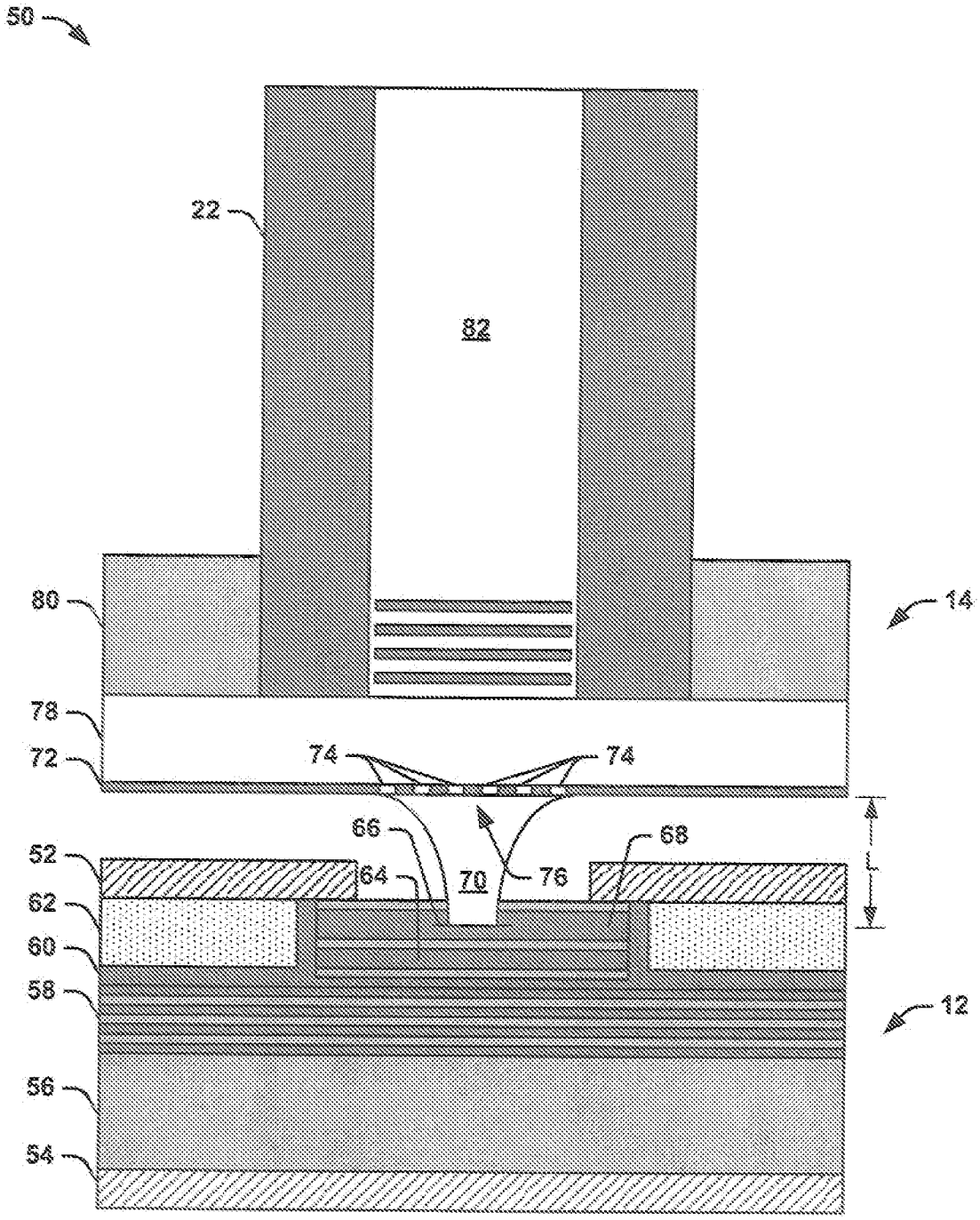


FIG. 2

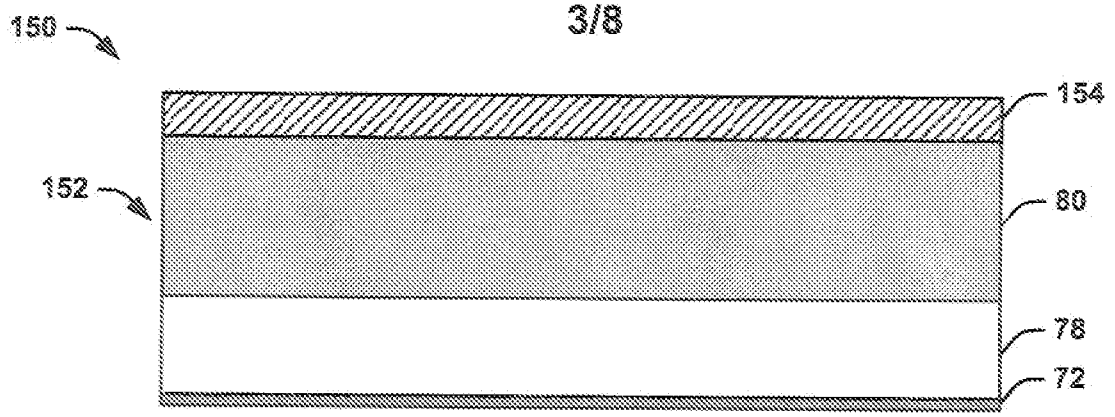


FIG. 4

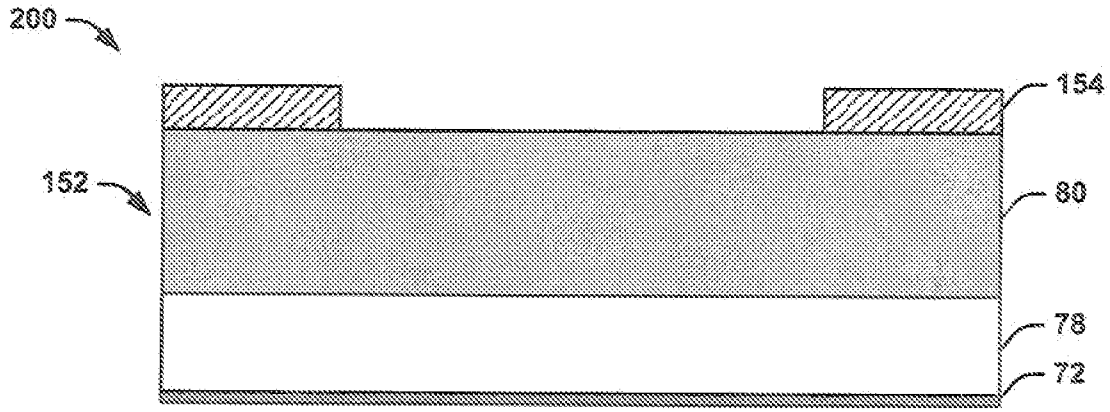


FIG. 5

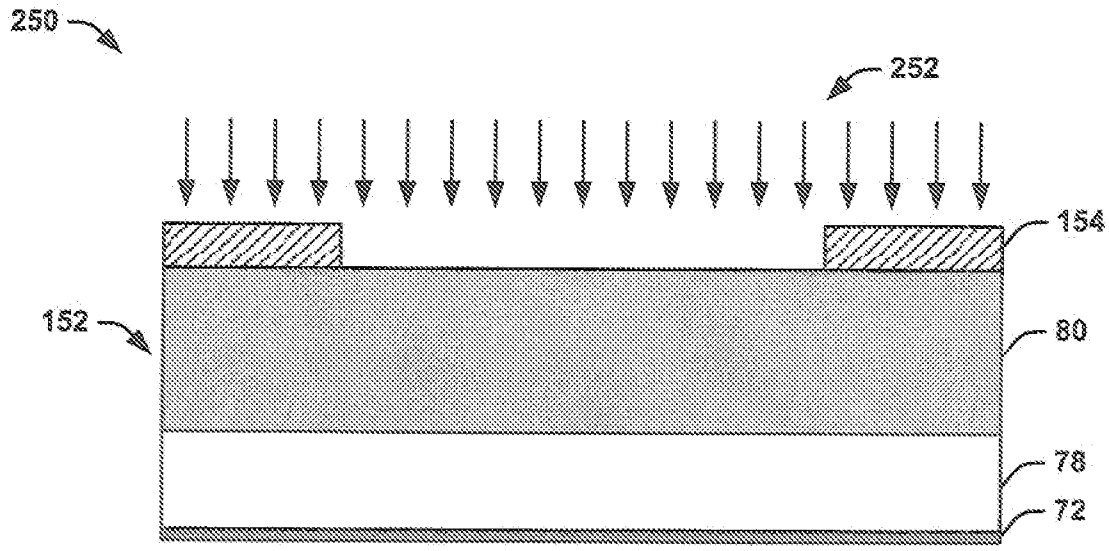


FIG. 6

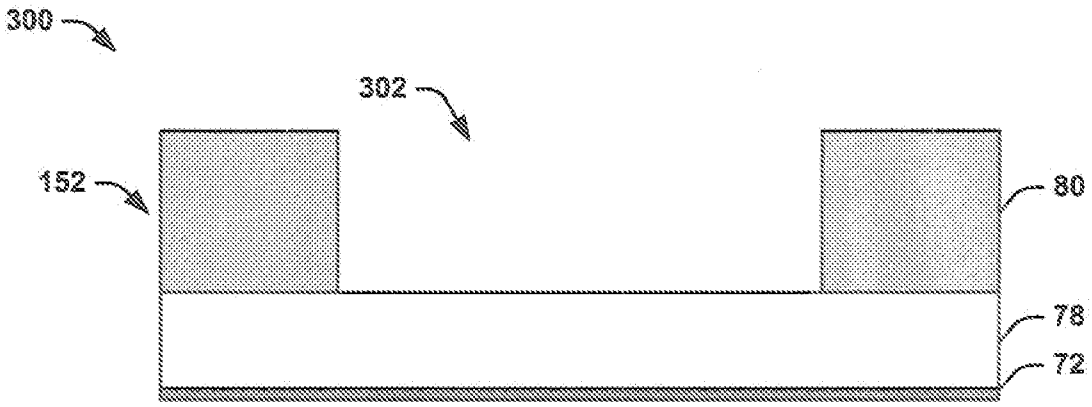


FIG. 7

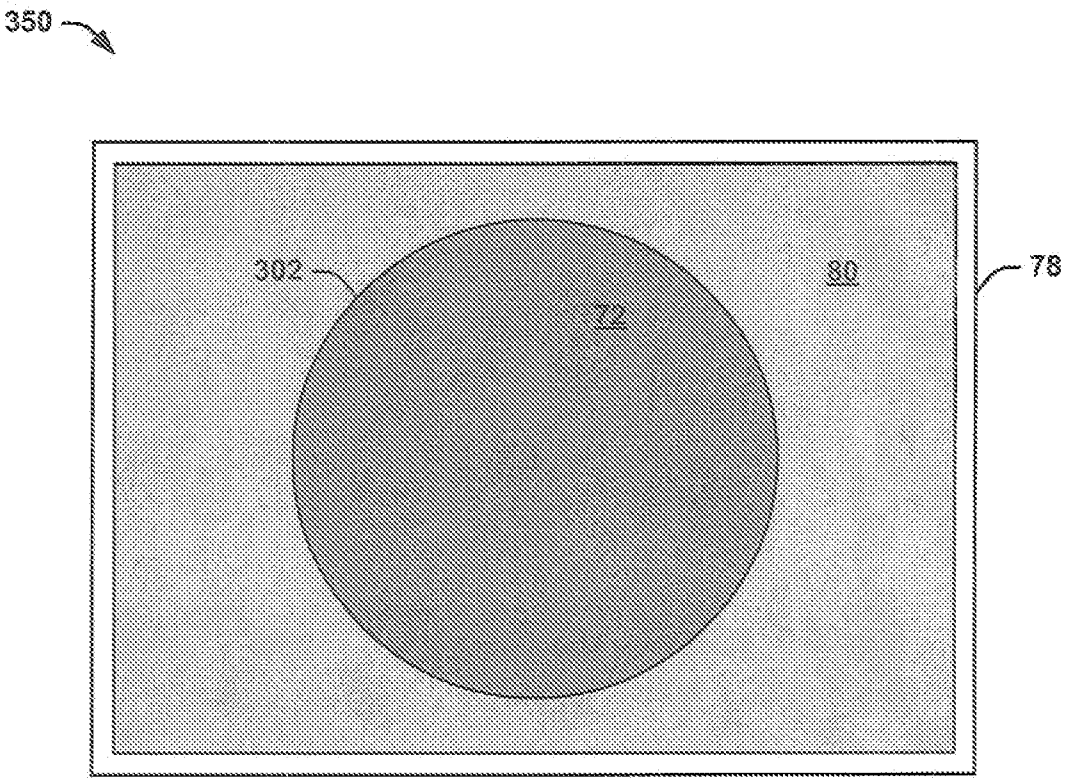


FIG. 8

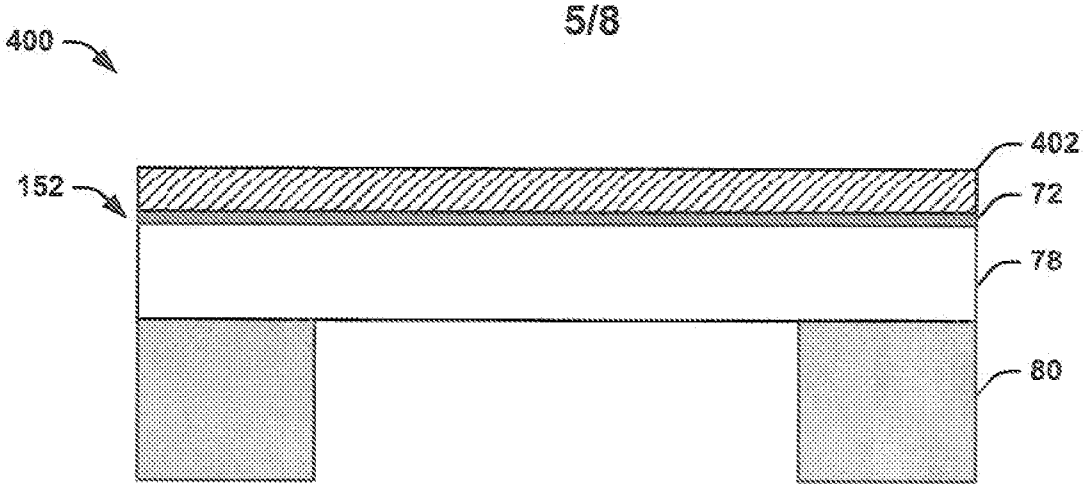


FIG. 9

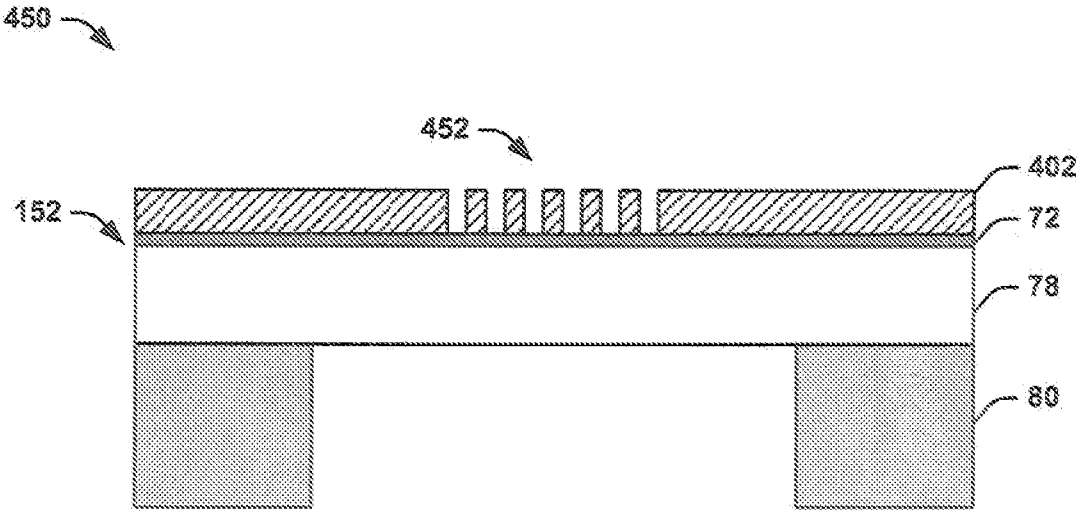


FIG. 10

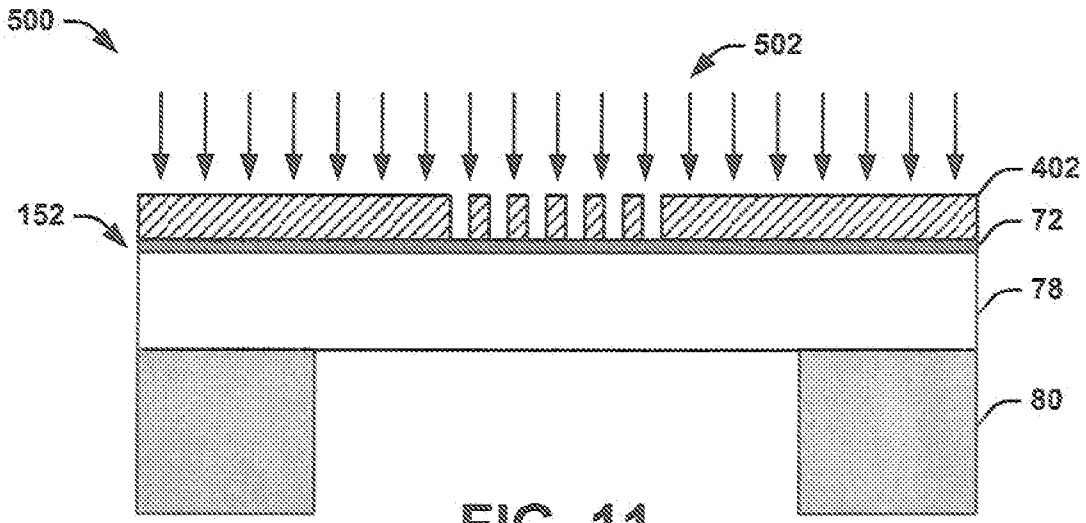


FIG. 11

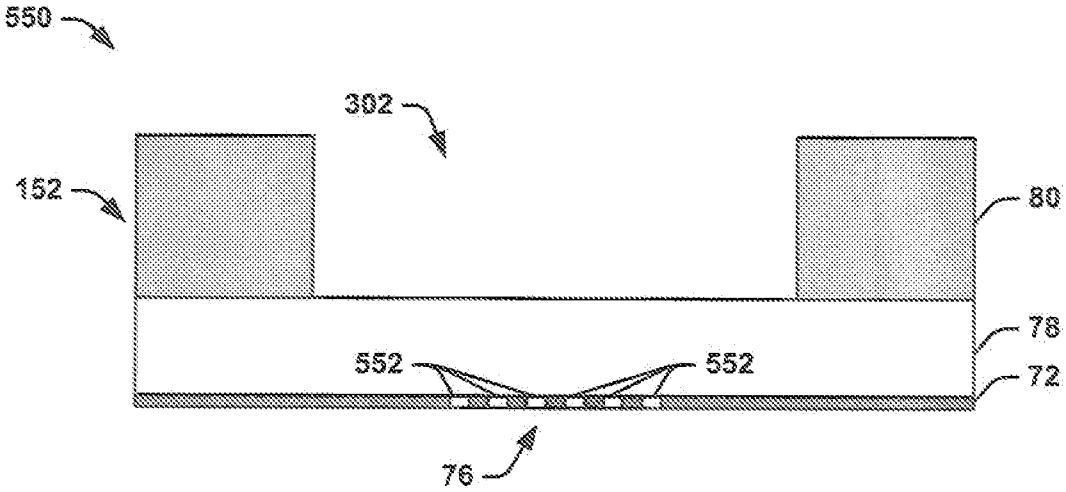


FIG. 12

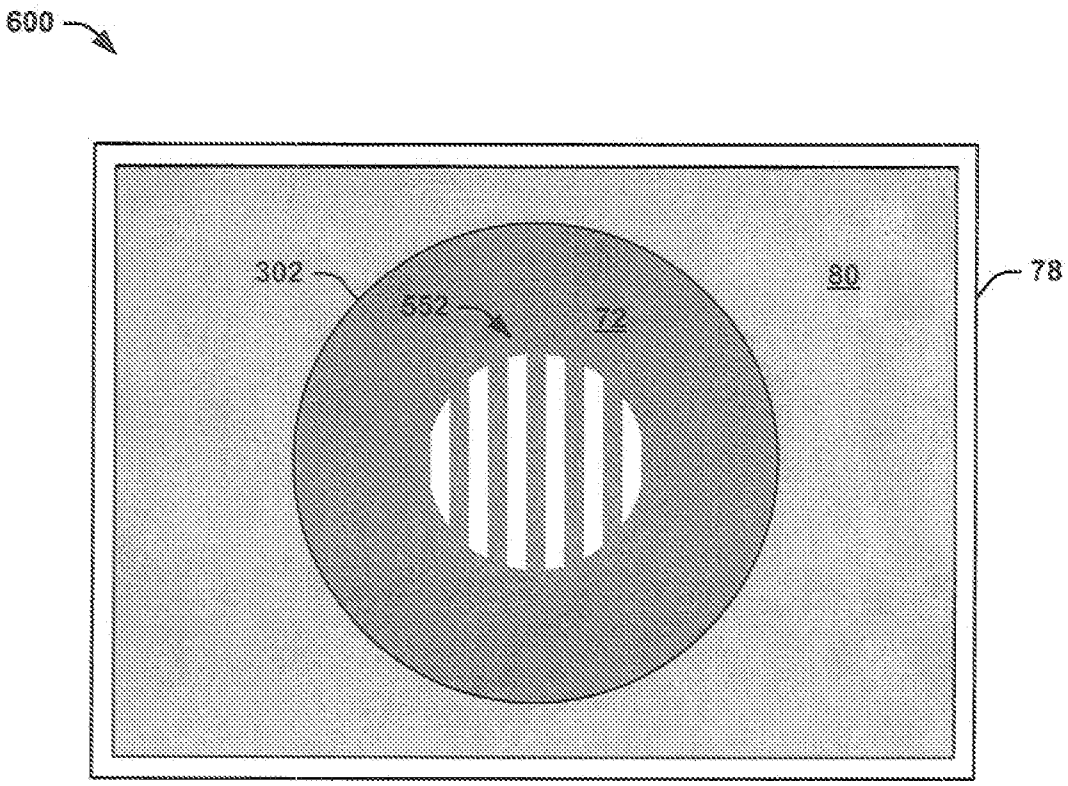


FIG. 13

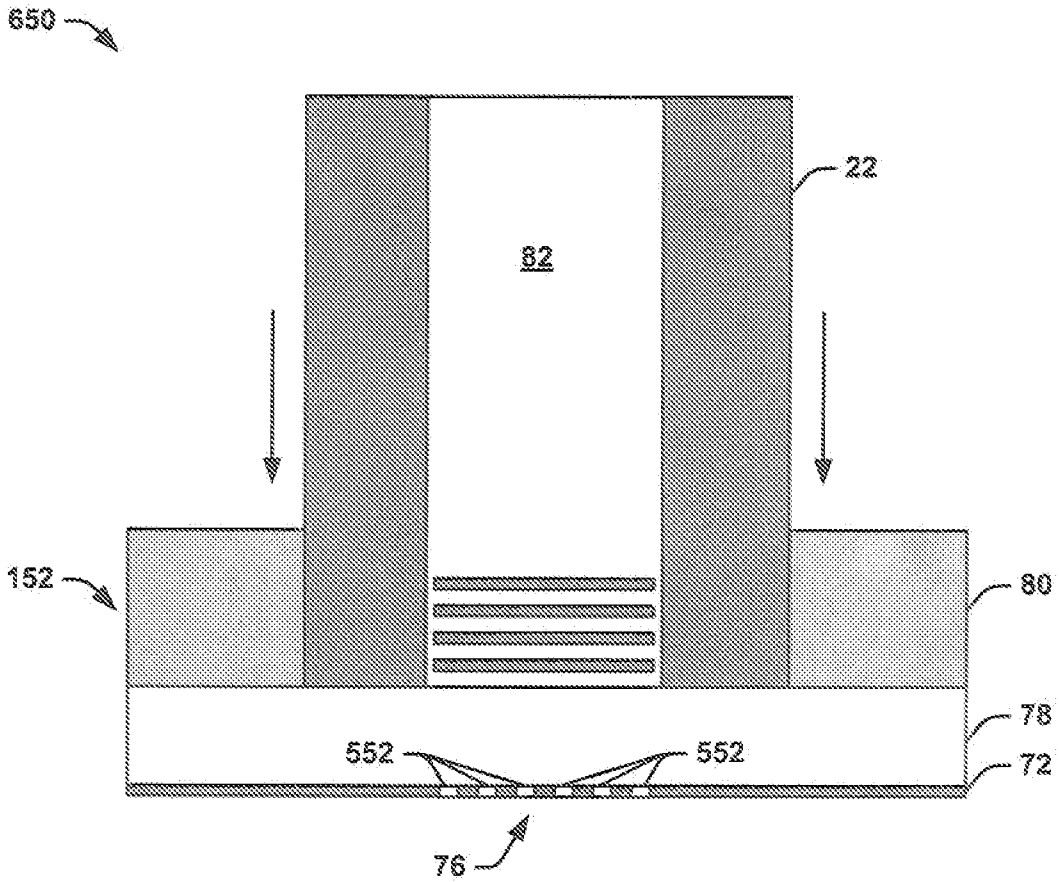

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80
78
552
552
72
76

FIG. 14

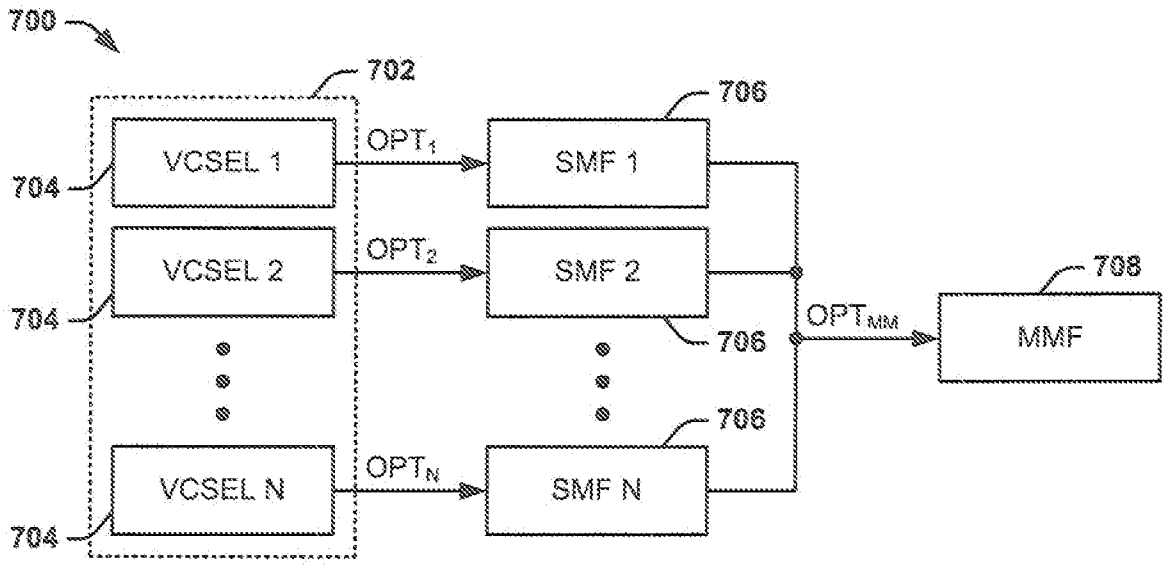

700
702
706
VCSEL 1
OPT1
SMF 1
704
VCSEL 2
OPT2
SMF 2
708
704
706
OPTMM
MMF
706
VCSEL N
OPTN
SMF N
704

FIG. 15

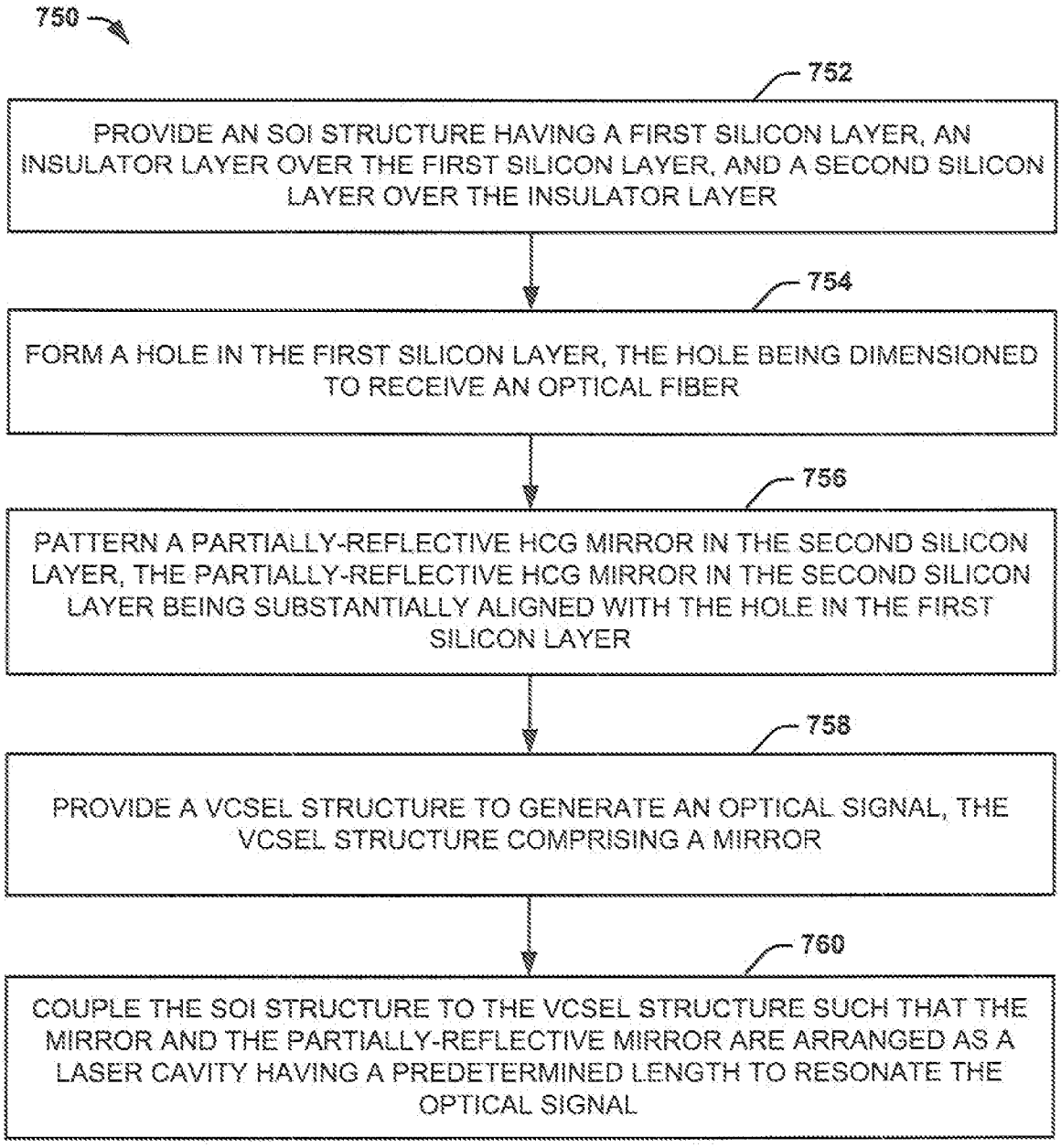

750
752
PROVIDE AN SOI STRUCTURE HAVING A FIRST SILICON LAYER, AN INSULATOR LAYER OVER THE FIRST SILICON LAYER, AND A SECOND SILICON LAYER OVER THE INSULATOR LAYER
754
FORM A HOLE IN THE FIRST SILICON LAYER, THE HOLE BEING DIMENSIONED TO RECEIVE AN OPTICAL FIBER
756
PATTERN A PARTIALLY-REFLECTIVE HCG MIRROR IN THE SECOND SILICON LAYER, THE PARTIALLY-REFLECTIVE HCG MIRROR IN THE SECOND SILICON LAYER BEING SUBSTANTIALLY ALIGNED WITH THE HOLE IN THE FIRST SILICON LAYER
758
PROVIDE A VCSEL STRUCTURE TO GENERATE AN OPTICAL SIGNAL, THE VCSEL STRUCTURE COMPRISING A MIRROR
760
COUPLE THE SOI STRUCTURE TO THE VCSEL STRUCTURE SUCH THAT THE MIRROR AND THE PARTIALLY-REFLECTIVE MIRROR ARE ARRANGED AS A LASER CAVITY HAVING A PREDETERMINED LENGTH TO RESONATE THE OPTICAL SIGNAL

FIG. 16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/061326

A. CLASSIFICATION OF SUBJECT MATTER

H01S 5/183(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01S 5/183; H01S 3/10; H01S 5/026; H01S 5/20; H01S 3/19; G02B 6/30; H01L 21/00; H01S 3/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: VERTICAL, CAVITY, SURFACE, EMITTING, LASER, OPTICAL, FIBER, VCSEL, WAFER

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003-0012231 A1 (PARVIZ TAYEBATI et al.) 16 January 2003 See paragraph 20 - paragraph 24; claim 1 and figures 1-2.	1-15
A	US 2010-0265983 A1 (ADACHI KOICHIRO et al.) 21 October 2010 See paragraph 83 - paragraph 87; claim 1 and figure 5.	1-15
A	US 2003-0072523 A1 (CHIH-HSIANG LIN et al.) 17 April 2003 See paragraph 29 - paragraph 41; claim 1 and figure 2.	1-15
A	US 05912913A A (KONDOW; MASAHIKO et al.) 15 June 1999 See column 6, line 40 - column 8, line 10; claim 1 and figure 2.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 SEPTEMBER 2011 (27.09.2011)	**28 SEPTEMBER 2011 (28.09.2011)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
Government Complex-Daejeon, 189 Cheongsa-ro,
Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

NAM, Jeong Kil

Telephone No. 82-42-481-5675

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2010/061326

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003-0012231 A1	16.01.2003	AU 1999-20174 A1	19.07.1999
		AU 1999-20174 B2	28.08.2003
		AU 2002-252381 A8	08.10.2002
		CA 2316858 A1	08.07.1999
		CA 2436737 A1	11.07.2002
		CN 1179191 C0	08.12.2004
		CN 1285034 A0	21.02.2001
		EP 1053574 A2	22.11.2000
		EP 1053574 A4	06.11.2002
		EP 1354378 A1	22.10.2003
		JP 2002-500446 A	08.01.2002
		JP 2002-500446 T	08.01.2002
		US 2002-0031155 A1	14.03.2002
		US 2002-0061042 A1	23.05.2002
		US 2002-0176470 A1	28.11.2002
		US 2003-0091072 A1	15.05.2003
		US 2004-0057473 A1	25.03.2004
		US 6438149 B1	20.08.2002
		US 6584126 B2	24.06.2003
		US 6639932 B1	28.10.2003
		US 6645784 B2	11.11.2003
		US 6813291 B2	02.11.2004
		WO 02-054546 A1	11.07.2002
		WO 02-075872 A1	26.09.2002
		WO 02-075879 A1	26.09.2002
		WO 02-077673 A2	03.10.2002
		WO 02-077673 A3	03.10.2002
		WO 99-34484 A2	08.07.1999
		WO 99-34484A3	10.09.1999
US 2010-0265983 A1	21.10.2010	JP 2010-251649 A	04.11.2010
US 2003-0072523 A1	17.04.2003	US 6669367 B2	30.12.2003
US 05912913A A	15.06.1999	JP 03-748140 B2	22.02.2006
		JP 09-237942 A	09.09.1997
		JP 2005-223351 A	18.08.2005