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(54) Title: SURFACE MODIFICATION TO IMPROVE AMORPHOUS SILICON GAPFILL

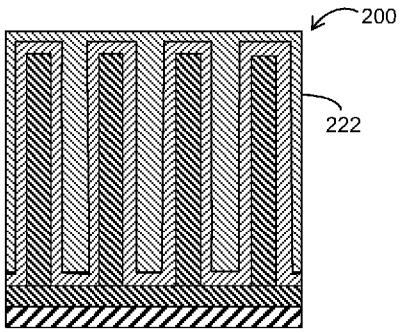

Figure 2C

(57) Abstract: Methods for gapfilling semiconductor device features, such as high aspect ratio trenches, with amorphous silicon (a-Si) film that involves pretreating the surface of the substrate to modify the underlying hydroxy-terminated silicon (Si-OH) or hydrogen-terminated silicon (Si-H) surface to oxynitride-terminated silicon (Si-ON) or nitride-terminated silicon (Si-N) and enhance the subsequent a-Si deposition are provided. First, a substrate having features formed in a first surface of the substrate is provided. The surface of the substrate is then pretreated to enhance the surface of the substrate for the flowable deposition of amorphous silicon that follows. A flowable deposition process is then performed to deposit a flowable silicon layer over the surface of the substrate. Methods described herein generally improve overall etch selectivity by the conformal silicon deposition and the flowable silicon deposition process to realize seam-free gapfilling between features with high quality amorphous silicon film.

SURFACE MODIFICATION TO IMPROVE AMORPHOUS SILICON GAPFILL

BACKGROUND

Field

[0001] Examples of the present disclosure generally relate to semiconductor manufacturing processes, more particularly, to methods for gapfilling high aspect ratio trenches of semiconductor devices with amorphous silicon film, and devices formed by the methods.

Description of the Related Art

[0002] For many semiconductor device manufacturing processes, there is a need to fill narrow trenches having high aspect ratios greater than, for example, 10:1, with no voiding. One example of such a process is shallow trench isolation (STI) in which the film needs to be of high quality and have very low leakage throughout the trench. As the dimensions of semiconductor device structures continue to decrease and the aspect ratios increase, post-curing processes become increasingly difficult and result in films with varying composition throughout the filled trench.

[0003] Conventionally, amorphous silicon (a-Si) has been used in semiconductor manufacturing processes since a-Si generally provides good etch selectivity with respect to other films, such as silicon oxide (SiO) and amorphous carbon (a-C). The conventional a-Si deposition methods, such as plasma-enhanced chemical vapor deposition (PECVD) and conformal deposition, however, cannot be used to gapfill high aspect ratio trenches because a seam forms in the high aspect ratio trenches. A seam may result in the formation of one or more gaps in the trench between the sidewalls, which may be further opened up during post-curing processes. Such seems and gaps ultimately cause decreased throughput or even semiconductor device failure. Additionally, PECVD of a-Si may also result in voiding at the bottom of the trench, which may also result in semiconductor device failure.

[0004] Additionally, the success of gapfilling high aspect ratio trenches with a-Si depends on the nature of the underlying surface. For example, when the underlying surface is hydroxy-terminated silicon (Si-OH), or hydrogen-terminated silicon (Si-H), microporosity and microvoiding has been observed.

[0005] Therefore, there is a need for methods for gapfilling high aspect ratio trenches of semiconductor devices that can provide seam-free and void-free film growth.

SUMMARY

[0006] Methods are provided for gapfilling semiconductor device features, such as high aspect ratio trenches, with amorphous silicon (a-Si) film that involve pretreating the surface of the substrate. The pretreatment modifies the underlying hydroxy-terminated silicon (Si-OH) or hydrogen-terminated silicon (Si-H) surface to oxynitride-terminated silicon (Si-ON) or nitride-terminated silicon (Si-N), and enhances the subsequent a-Si deposition. First, a substrate having features formed in a first surface of the substrate is positioned in a processing chamber. The surface of the substrate is then pretreated to enhance the surface of the substrate for the flowable deposition of amorphous silicon that follows. A flowable deposition process is then performed to deposit a flowable silicon layer over the surface of the substrate. Methods described herein generally improve overall etch selectivity by the conformal silicon deposition and the flowable silicon deposition process to realize seam-free gapfilling between features with high quality amorphous silicon film.

[0007] In one example, a method for manufacturing a semiconductor device is disclosed. The method includes positioning a substrate having at least one feature formed in a surface of the substrate in a processing chamber, the at least one feature having sidewalls and a bottom surface, exposing the at least one feature formed in the surface of the substrate to a pretreatment process, and filling the at least one feature with a flowable silicon film. The pretreatment process includes exposing the surface of the

substrate to an inert gas and exposing the surface of the substrate to reactive plasma.

[0008] In another example, a method for manufacturing a semiconductor device is disclosed. The method includes positioning a substrate having at least one feature formed in a surface of the substrate in a processing chamber, the at least one feature having sidewalls and a bottom surface, exposing the at least one feature formed in the surface of the substrate to a pretreatment process, and filling the at least one feature with a flowable silicon film. The pretreatment process includes exposing the surface of the substrate to one or more reactive radicals.

[0009] In yet another example, a semiconductor device is disclosed. The semiconductor device includes a substrate having at least one feature formed in a surface of the substrate, the at least one feature having sidewalls and a bottom surface, an oxynitride-terminated silicon layer disposed over the surface of the substrate and the sidewalls and the bottom surface of the at least one feature, and a flowable silicon film disposed over the oxynitride-terminated silicon layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to examples, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical examples of this disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective examples.

[0011] Figure 1 is a flow diagram summarizing a method according to one example described herein.

[0012] Figures 2A-2C depict stages of fabrication of a semiconductor device in accordance with the method of Figure 1.

[0013] Figure 3 is a schematic cross-section view of a processing chamber according to an embodiment.

[0014] To facilitate understanding, identical reference numerals have been used, wherever possible, to designate identical elements that are common to the Figures. Additionally, elements of one example may be advantageously adapted for utilization in other examples described herein.

DETAILED DESCRIPTION

[0015] Methods are provided for gapfilling semiconductor device features, such as high aspect ratio trenches, with amorphous silicon (a-Si) film that involves pretreating the surface of the substrate to modify the underlying hydroxy-terminated silicon (Si-OH) or hydrogen-terminated silicon (Si-H) surface to oxynitride-terminated silicon (Si-ON) or nitride-terminated silicon (Si-N) and enhance the subsequent a-Si deposition. First, a substrate having features formed in a first surface of the substrate is positioned in a processing chamber. The surface of the substrate is then pretreated to enhance the surface of the substrate for the flowable deposition of amorphous silicon that follows. A flowable deposition process is then performed to deposit a flowable silicon layer over the surface of the substrate. Methods described herein generally improve overall etch selectivity by the conformal silicon deposition and the flowable silicon deposition process to realize seam-free gapfilling between features with high quality amorphous silicon film.

[0016] Figure 1 is a flow diagram summarizing a method 100 for gapfilling high aspect ratio trenches of a semiconductor device with amorphous silicon film. Figures 2A-2C depict stages of fabrication of a semiconductor device 200 in accordance with the method 100 of Figure 1. The method 100 is described below in accordance with stages of gapfilling high aspect ratio trenches of a semiconductor device 200 with amorphous silicon film as illustrated in Figures 2A-2C. The description that follows will refer to high aspect ratio trenches formed on a substrate, such as a silicon substrate; however, methods described herein are also applicable to gapfilling between other semiconductor device features. Features generally have any suitable

shape, including, but not limited to, trenches and cylindrical vias. Generally, "feature" means any intentional surface irregularity. Suitable examples of features include, but are not limited to, trenches which have a top, two sidewalls and a bottom, peaks which have a top and two sidewalls. Features can have any suitable aspect ratio, or ratio of the depth of the feature to the width of the feature. In some examples, the aspect ratio is greater than or equal to about 5:1, 10:1, 15:1, 20:1, 25:1, 30:1, 35:1, or 40:1.

[0017] The method 100 begins at operation 102 in which a substrate 208 with a plurality of features 212 (shown as trenches) formed in a silicon containing layer 210 of the substrate 208, as shown in Figure 2A, is positioned within a processing chamber. The substrate 208 may be any suitable size and material, for example, a 300 mm substrate. The features 212 generally extend from a surface of the substrate 213 to a depth (D) to a bottom surface 214. The features 212 generally include a first sidewall 216 and a second sidewall 218 that define a width (W) of the feature 212. As shown in Figure 2A, the substrate 208 has a plurality of features 212; however, it is contemplated that the substrate 208 can have one or more than one feature 212. As discussed above, the silicon containing layer 210 of the surface of the substrate 208 is generally hydroxy or hydrogen-terminated, which often results in microporosity and microvoiding issues.

[0018] At operation 104, prior to deposition of a flowable silicon film on the substrate 208, but after the substrate 208 having features 212 has been positioned in a processing chamber, a pretreatment process may be performed to pretreat the surface of the substrate 213, thus forming a pretreated surface layer 220 on the surface of the substrate 213, sidewalls 216, and bottoms 214, as shown in Figure 2B. Operation 104 generally modifies the underlying hydroxy-terminated silicon (Si-OH) or hydrogen-terminated silicon (Si-H) surface of the substrate to oxynitride-terminated silicon (Si-ON) or nitride-terminated silicon (Si-N) to enhance the subsequent a-Si deposition. As described below, various pretreatment processes may be used.

[0019] In one example, the pretreatment process of operation 104 generally includes treating the surface of the substrate 213 and features 212 formed therein with a pretreatment gas mixture. The pretreatment gas mixture generally includes at least a reactive gas, including but not limited to at least one of a hydrogen gas (H_2), ammonia (NH_3), oxygen gas (O_2), and nitrous oxide (N_2O). An inert gas, including but not limited to at least one of helium (He), argon (Ar), and the like, is generally also supplied into the pretreatment gas mixture. By exposing the surface of the substrate 213 to the inert gas and exposing the surface of the substrate to reactive plasma, the surface of the substrate 213 is modified to contain a oxynitride or nitrogen-terminated silicon pretreated surface layer 220, which causes enhanced subsequent flowable amorphous silicon deposition, and thus, enhanced and seam-free gapfilling. The pretreatment gas mixture is generally supplied by a remote plasma source (RPS), such as a capacitively coupled plasma (CCP) source, or any other suitable source.

[0020] In another example, the pretreatment process of operation 104 generally includes treating the surface of the substrate 213 and features 212 formed therein with reactive radicals. The reactive radicals may be radical species from a plasma from ions have been filtered out. The reactive radicals generally include, but are not limited to, one or more of NH_3, H_2, O_2, N_2O, and N_2. The reactive radicals are generally supplied by an RPS, such as a CCP source, or any other suitable source. By exposing the surface of the substrate 213 to reactive radicals, the surface of the substrate 213 is modified to contain an oxynitride or nitrogen-terminated silicon pretreated surface layer 220, which causes enhanced subsequent flowable amorphous silicon deposition, and thus, enhanced and seam-free gapfilling.

[0021] During the pretreatment process of operation 104, several processing parameters are generally regulated to control the pretreatment process. For example, when a CCP source is used, the frequency is 13.6 megahertz (MHz) or 2MHz. The pretreatment process pressure in the process chamber is generally between about 1 Torr (T) and about 50T, such

as 5 Torr to about 40 Torr, for example about 10 Torr to about 30 Torr. An RF power between about 10 Watts (W) and about 1000W is generally applied to maintain plasma in the pretreatment gas mixture. A temperature of the pretreatment process is generally between about 0 degrees Celsius (°C) and about 400°C.

[0022] In yet another example, the pretreatment process of operation 104 generally includes treating the surface of the substrate 213 and features 212 formed therein with chemical passivation of the Si-OH or Si-H bonds using at least one of aminosilanes and chlorosilanes. Examples of aminosilanes include, but are not limited to, silanamine (H_5NSi) and (3-Aminopropyl)triethoxysilane (APTES). Examples of chlorosilanes include, but are not limited to, ClH_3Si. By performing chemical passivation on the surface of the substrate 213 using at least one of aminosilanes and chlorosilanes, the surface of the substrate 213 is modified to contain an oxynitride or nitrogen-terminated silicon pretreated surface layer 220, which causes enhanced subsequent flowable amorphous silicon deposition, and thus, enhanced and seam-free gapfilling.

[0023] In even further examples, the pretreatment process of operation 104 generally includes any combination of the aforementioned pretreatment processes.

[0024] At operation 106, the feature 212 is filled with a flowable silicon film 222, as shown in Figure 2C. In one example, the flowable silicon film 222 is deposited on and in contact with the silicon liner layer 220. The flowable silicon film 222 generally comprises amorphous silicon having hydrogen (H) concentration of greater than about 30%. The flowable silicon film 222 fills the remaining space in the features 212 so that substantially no seam is formed in the features 212. The flowable silicon film 222 can be deposited by any suitable process, such as the process described in U.S Patent Application Serial No. 62/354,743, which is herein incorporated by reference in its entirety, and is discussed below.

[0025] In one example, the flowable silicon film 222 is deposited by a PECVD process. The PECVD process generally begins by exposing the surface of the substrate 213 to a reactive gas, which generally includes one or more species. For example, the reactive gas generally includes a second precursor and a plasma gas, which is used as a diluent or carrier gas for the first precursor. The second precursor generally includes one or more of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), and tetrasilane (Si_4H_{10}). The plasma gas generally includes one or more of helium (He), argon (Ar), hydrogen gas (H_2), krypton (Kr), nitrogen gas (N_2), oxygen gas (O_2), ozone (O_3), or ammonia (NH_3).

[0026] The plasma can be generated or ignited within a processing chamber (e.g., a direct plasma) or can be generated outside of a processing chamber and flowed into the processing chamber (e.g., a remote plasma). The radiofrequency (RF) power used for igniting the plasma is generally between about 10 watts (W) and about 200W. During the PECVD process for depositing the flowable silicon film, the temperature in the processing environment is generally between about -100°C and about 50°C, and the pressure is generally between about 1Torr and about 10 Torr.

[0027] The flowable silicon film 222 is generally of a suitable thickness to fill the remaining space in the features 212. In the example discussed above in which the features 212 have a width (W) of about 20nm, then the flowable silicon film 222 generally has a thickness of about 4nm to provide a seam-free gapfill in the features 212.

[0028] After operation 106, further processing operations may be performed, such as curing and or annealing operations, to increase the density o the flowable silicon film 222. Additionally, it is contemplated that operations, such as precleaning, may be performed prior to or between operations 102, 104, and 106.

[0029] Figure 3 is a schematic cross-sectional view of a processing chamber 300, according to one embodiment. Exemplary processing

chambers are available from Applied Materials, Inc. located in Santa Clara, Calif. It is to be understood that the chamber described below is an exemplary chamber and other chambers, including chambers from other manufacturers, may be used with or modified to accomplish aspects of the present disclosure.

[0030] The plasma processing chamber 300 includes a chamber body 302, a substrate support assembly 305, and a gas distribution assembly 304 positioned opposite the substrate support assembly 305 and defining a process volume 306 therebetween. The gas distribution assembly is configured to distribute gases uniformly into the process volume 306 of the plasma processing chamber 300 to facilitate deposition of a film onto a substrate 310 positioned on the substrate support 305. The gas distribution assembly 304 includes a gas inlet passage 317, which delivers gas from a gas flow controller 320 into a gas distribution manifold 318 suspended from a hanger plate 319. The gas distribution manifold 318 includes a plurality of holes or nozzles (not shown) through which gaseous mixtures are injected into the process volume 306 during processing. The gas distribution assembly 304 can be connected to an RF return 322 to allow RF energy applied to a substrate support 308 to generate an electric field within the process volume 306, which is used to generate the plasma for processing of the substrate 310. Power supply 320 may provide a DC energy source, while power supply 321 may provide an RF energy source to facilitate plasma generation and/or chucking of the substrate 310.

[0031] The substrate support assembly 305 includes the substrate support 308, a base 315, a stem 314 connecting the base 315 to the substrate support 108, and a drive system 303. The substrate support assembly 305 is disposed within the interior volume of the plasma processing chamber 300. The substrate support 308 has an upper surface 309 that supports the substrate 310 and a lower surface 311 for mounting the stem 314 to the substrate support 308. The substrate support 308 is movably disposed in the process volume 306 by the stem 314 that is coupled to the drive system 303

located external of the chamber body 302. The stem 314 and base 315 are connected to the drive system 303 and a bellows (not shown) to allow the substrate support 308 to be raised, lowered, and/or rotated.

[0032] During processing, process gases are provided to the process chamber 300 to deposit films in accordance with aspects described above.

[0033] The above-described methods, such as the pretreatment process and flowable silicon deposition, may be performed in a single chamber, such as a Producer® chamber available from Applied Materials, Inc. of Santa Clara, California, or the above-described processes may be performed in various chambers of a cluster tool comprising multiple chambers which perform various functions, such as the Centura® available from Applied Materials, Inc. of Santa Clara, California.

[0034] Examples of the present disclosure provide methods for gapfilling semiconductor device features, such as high aspect ratio trenches, with a-Si film that involves pretreating the surface of the substrate to modify the underlying Si-OH or Si-H surface to Si-ON or Si-N. The modification of the underlying surface of the substrate results in improved gapfilling, and more specifically semiconductor devices having seam-free and void-free a-Si gapfill without microporosity issues. More generally, the examples described herein result in semiconductor devices having increased silicon density and increased uniformity, which ultimately improves device functionality.

[0035] While the foregoing is directed to examples of the present disclosure, other and further examples of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method for manufacturing a semiconductor device, comprising:

positioning a substrate having at least one feature formed in a surface of the substrate, the at least one feature having sidewalls and a bottom surface;

exposing the at least one feature formed in the surface of the substrate to a pretreatment process, the pretreatment process comprising:

exposing the surface of the substrate to an inert gas; and

exposing the surface of the substrate to a reactive plasma; and

filling the at least one feature with a flowable silicon film.

2. The method of claim 1, wherein the inert gas comprises one or more of helium and argon.

3. The method of claim 1, wherein the reactive plasma comprises one or more of hydrogen gas and ammonia.

4. The method of claim 1, wherein the surface of the substrate prior to the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is hydroxy or hydrogen-terminated silicon.

5. The method of claim 4, wherein the surface of the substrate after the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is oxynitride-terminated silicon or nitrogen-terminated silicon.

6. The method of claim 1, wherein the exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a temperature between about 0 degrees Celsius and about 400 degrees Celsius.

7. The method of claim 1, wherein exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a pressure between about 1 Torr and about 50 Torr.

8. The method of claim 1, wherein exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a power between about 10 Watts and about 1000 Watts.

9. The method of claim 1, wherein exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a frequency of about 13.6 megahertz or about 2 megahertz.

10. A method for manufacturing a semiconductor device, comprising:

providing a substrate having at least one feature formed in a surface of the substrate, the at least one feature having sidewalls and a bottom surface;

exposing the at least one feature formed in the surface of the substrate to a pretreatment process, the pretreatment process comprising:

exposing the surface of the substrate to one or more reactive radicals; and

filling the at least one feature with a flowable silicon film.

11. The method of claim 10, wherein the one or more reactive radicals are selected from the group consisting of ammonia, hydrogen, oxygen, nitrous oxide, and nitrogen.

12. The method of claim 10, wherein the surface of the substrate prior to the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is hydroxy or hydrogen-terminated silicon.

13. The method of claim 12, wherein the surface of the substrate after the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is oxynitride-terminated silicon or nitrogen-terminated silicon.

14. A semiconductor device, comprising:

a substrate having at least one feature formed in a surface of the substrate, the at least one feature having sidewalls and a bottom surface;

an oxynitride-terminated silicon layer disposed over the surface of the substrate and the sidewalls and the bottom surface of the at least one feature; and

a flowable silicon film disposed over the oxynitride-terminated silicon layer.

15. The semiconductor device of claim 14, wherein the oxynitride-terminated silicon is disposed on and in contact with the surface of the substrate and the sidewalls and the bottom surface of the at least one feature.

AMENDED CLAIMS
received by the International Bureau on 14 September 2018

What is claimed is:

1. A method for manufacturing a semiconductor device, comprising:

positioning a substrate having at least one feature formed in a surface of the substrate, the at least one feature having sidewalls and a bottom surface;

exposing the at least one feature formed in the surface of the substrate to a pretreatment process, the pretreatment process comprising:

exposing the surface of the substrate to an inert gas; and

exposing the surface of the substrate to a reactive plasma; and

filling the at least one feature with a flowable silicon film.

2. The method of claim 1, wherein the inert gas comprises one or more of helium and argon.

3. The method of claim 1, wherein the reactive plasma comprises one or more of hydrogen gas and ammonia.

4. The method of claim 1, wherein the surface of the substrate prior to the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is hydroxy or hydrogen-terminated silicon.

5. The method of claim 4, wherein the surface of the substrate after the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is oxynitride-terminated silicon or nitrogen-terminated silicon.

6. The method of claim 1, wherein the exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a temperature between about 0 degrees Celsius and about 400 degrees Celsius.

7. The method of claim 1, wherein exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a pressure between about 1 Torr and about 50 Torr.

8. The method of claim 1, wherein exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a power between about 10 Watts and about 1000 Watts.

9. The method of claim 1, wherein exposing the at least one feature formed in the surface of the substrate to a pretreatment process occurs at a frequency of about 13.6 megahertz or about 2 megahertz.

10. A method for manufacturing a semiconductor device, comprising:

providing a substrate having at least one feature formed in a surface of the substrate, the at least one feature having sidewalls and a bottom surface;

exposing the at least one feature formed in the surface of the substrate to a pretreatment process, the pretreatment process comprising:

exposing the surface of the substrate to one or more reactive radicals; and

filling the at least one feature with a flowable silicon film.

11. The method of claim 10, wherein the one or more reactive radicals are selected from the group consisting of ammonia, hydrogen, oxygen, nitrous oxide, and nitrogen.

12. The method of claim 10, wherein the surface of the substrate prior to the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is hydroxy or hydrogen-terminated silicon.

13. The method of claim 12, wherein the surface of the substrate after the exposing the at least one feature formed in the surface of the substrate to the pretreatment process is oxynitride-terminated silicon or nitrogen-terminated silicon.

14. A semiconductor device, comprising:

a substrate having at least one feature formed in a surface of the substrate, the at least one feature having sidewalls and a bottom surface;

an oxynitride-terminated silicon layer disposed over the surface of the substrate and the sidewalls and the bottom surface of the at least one feature; and

a flowable silicon film disposed over the oxynitride-terminated silicon layer.

15. The semiconductor device of claim 14, wherein the oxynitride-terminated silicon layer is disposed on and in contact with the surface of the substrate and the sidewalls and the bottom surface of the at least one feature.

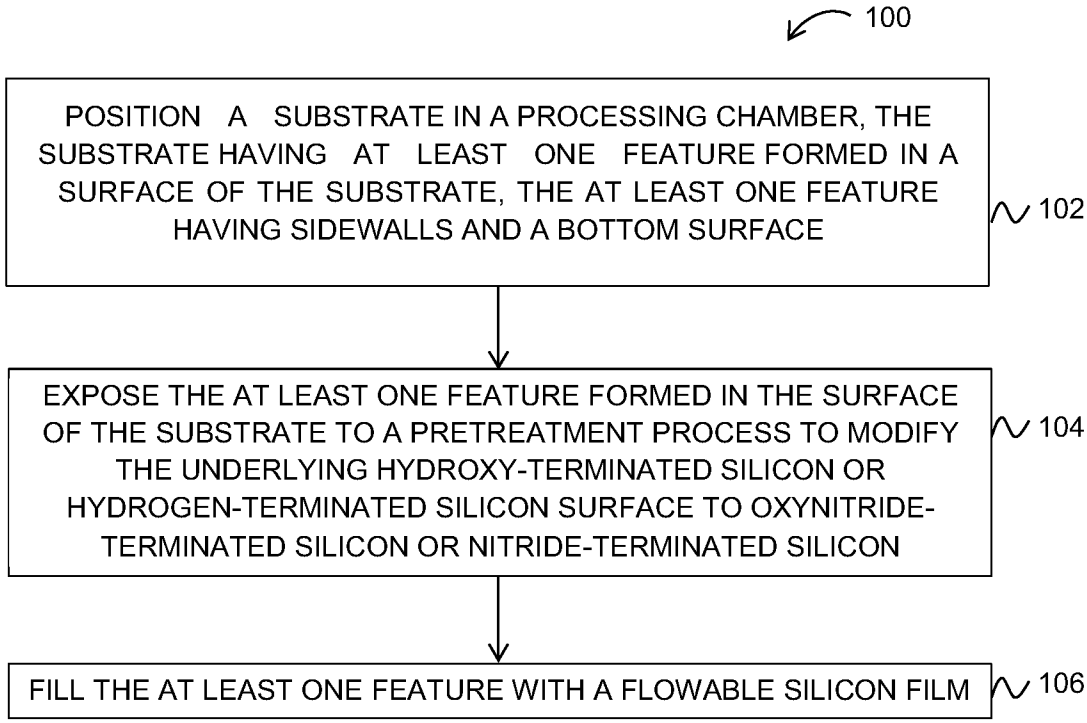
100
POSITION A SUBSTRATE IN A PROCESSING CHAMBER, THE SUBSTRATE HAVING AT LEAST ONE FEATURE FORMED IN A SURFACE OF THE SUBSTRATE, THE AT LEAST ONE FEATURE HAVING SIDEWALLS AND A BOTTOM SURFACE
102
EXPOSE THE AT LEAST ONE FEATURE FORMED IN THE SURFACE OF THE SUBSTRATE TO A PRETREATMENT PROCESS TO MODIFY THE UNDERLYING HYDROXY-TERMINATED SILICON OR HYDROGEN-TERMINATED SILICON SURFACE TO OXYNITRIDE-TERMINATED SILICON OR NITRIDE-TERMINATED SILICON
104
FILL THE AT LEAST ONE FEATURE WITH A FLOWABLE SILICON FILM
106

Figure 1

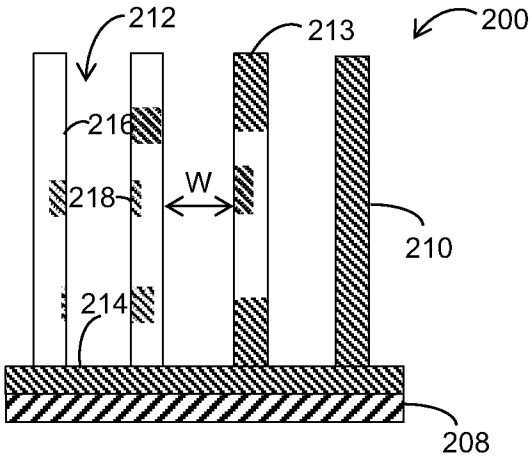

Figure 2A

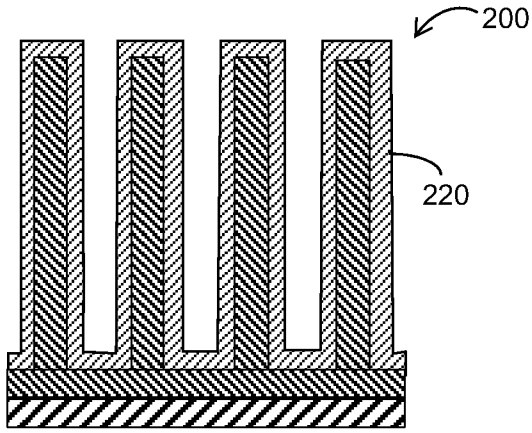

Figure 2B

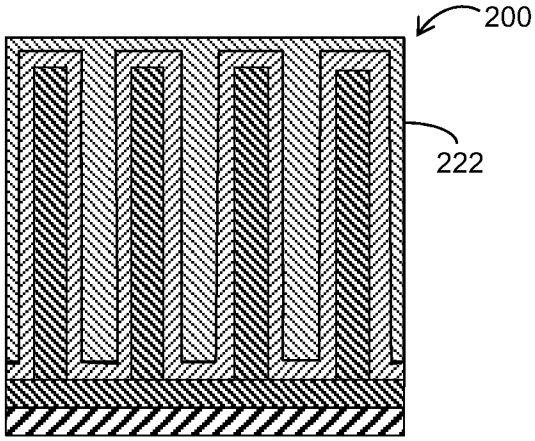

Figure 2C

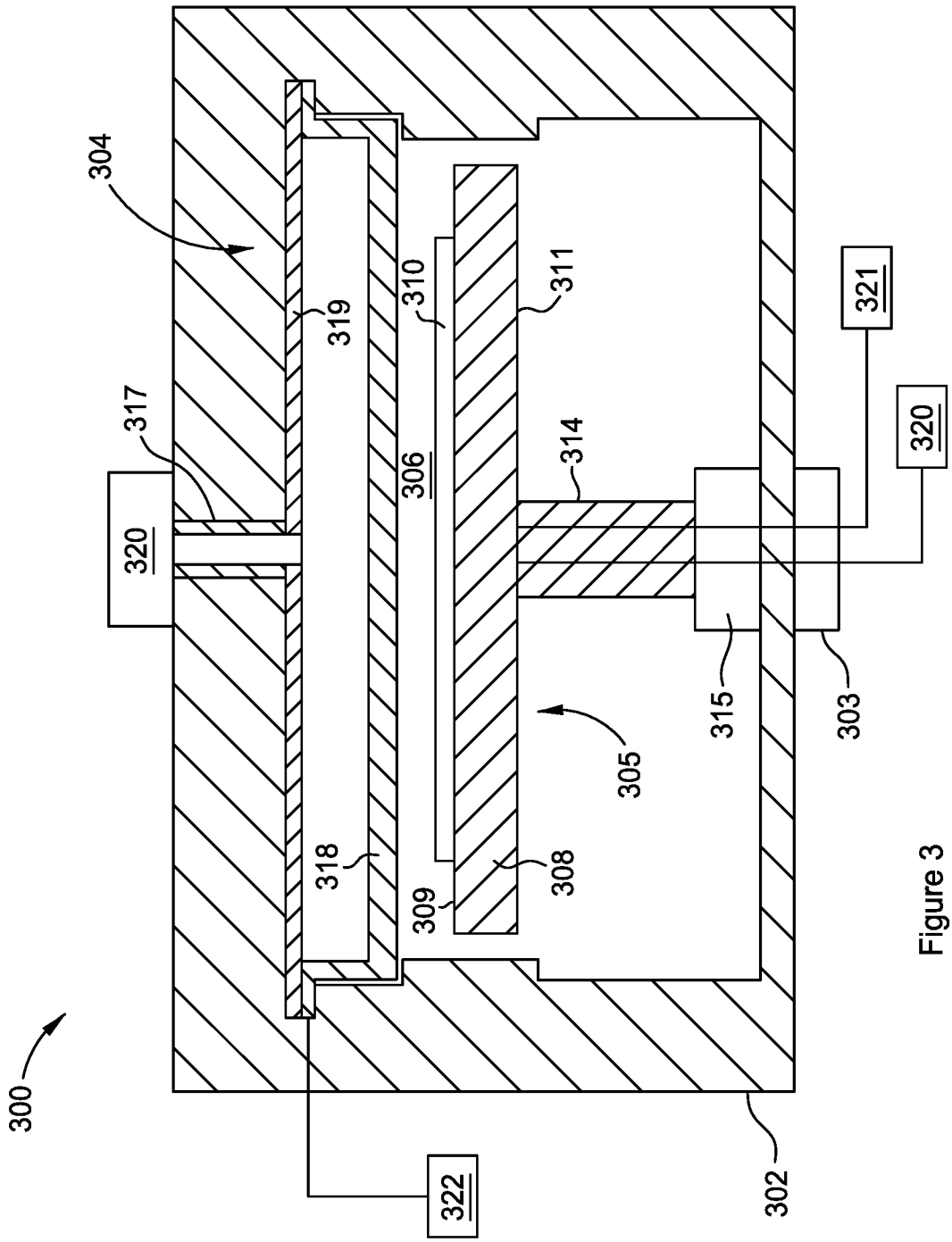
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Figure 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/024502

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H05H 1/24; H01L 21/312; H01L 21/02; H01L 21/8238; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: amorphous, gapfill, pretreatment, inert gas, reactive, plasma, flowable, oxynitride, terminated

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006-0045988 A1 (YOOU-BIN GUO et al.) 02 March 2006 See paragraphs 17-22, claims 1-22 and figures 1-4.	1-13
A		14-15
Y	US 7947551 B1 (SEN-HONG SYUE et al.) 24 May 2011 See column 1, line 58-column 4, line 3, claims 1-20 and figures 1-7.	1-15
Y	US 2002-0177270 A1 (KLAUS D. BEYER et al.) 28 November 2002 See paragraphs 28-48, claims 1-35 and figures 5-8.	5,13-15
A	US 2014-0193979 A1 (APPLIED MATERIALS, INC.) 10 July 2014 See the entire document.	1-15
A	US 8557712 B1 (GEORGE ANDREW ANTONELLI et al.) 15 October 2013 See the entire document.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 July 2018 (13.07.2018)	**13 July 2018 (13.07.2018)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2018/024502

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006-0045988 A1	02/03/2006	JP 11-282427 A	15/10/1999
		TW 200608487 A	01/03/2006
		TW 240328 A	21/09/2005
		TW I240328 B	21/09/2005
		US 6097616 A	01/08/2000
US 7947551 B1	24/05/2011	CN 102420164 A	18/04/2012
		CN 102420164 B	06/04/2016
US 2002-0177270 A1	28/11/2002	CN 1528015 A	08/09/2004
		CN 1528015 C	15/08/2007
		JP 2004-530304 A	30/09/2004
		KR 10-0564989 B1	28/03/2006
		KR 10-2003-0097835 A	31/12/2003
		TW 222698 A	21/10/2004
		TW I222698 B	21/10/2004
		US 2003-0015736 A1	23/01/2003
		US 2004-0106267 A1	03/06/2004
		US 6498383 B2	24/12/2002
		US 6709951 B2	23/03/2004
		US 6764922 B2	20/07/2004
		WO 02-095818 A1	28/11/2002
US 2014-0193979 A1	10/07/2014	CN 104813450 A	29/07/2015
		KR 10-2015-0060920 A	03/06/2015
		TW 201417183 A	01/05/2014
		US 2015-0072508 A1	12/03/2015
		US 2016-0247689 A1	25/08/2016
		US 9177780 B2	03/11/2015
		US 9245769 B2	26/01/2016
		US 9653318 B2	16/05/2017
		WO 2014-055235 A1	10/04/2014
US 8557712 B1	15/10/2013	JP 2010-153859 A	08/07/2010
		KR 10-1698595 B1	20/01/2017
		KR 10-2010-0069603 A	24/06/2010