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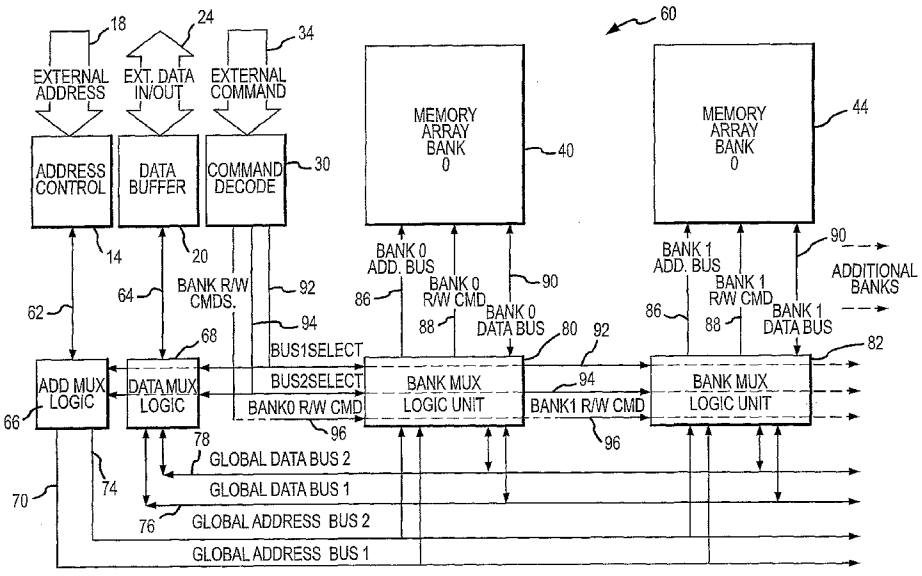
(54) **Title:** MEMORY DEVICE AND METHOD HAVING MULTIPLE ADDRESS, DATA AND COMMAND BUSES



(57) **Abstract:** A dynamic random access memory ("DRAM") device includes a pair of internal address buses that are selectively coupled to an external address bus by an address multiplexer, and a pair of internal data buses that are selectively coupled to an external data bus by a data multiplexer. The DRAM device also includes a bank multiplexer for each bank of memory cells that selectively couples one of the internal address buses and one of the internal data buses to the respective bank of memory cells. Select signals generated by a command decoder cause the multiplexers to select alternate internal address and data buses responsive to each memory command received by the command decoder.

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MEMORY DEVICE AND METHOD HAVING MULTIPLE ADDRESS, DATA AND COMMAND BUSES

TECHNICAL FIELD

[001] This invention relates to memory devices, and, more particularly, to a memory device and method that has multiple internal buses to provide increased performance.

BACKGROUND OF THE INVENTION

[002] Maximizing memory bandwidth, *i.e.*, the rate at which data can be written or read, is an important factor in memory device performance. Memory bandwidth has been increased to some extent by prefetching data so that the data will be available when it is called for by a received memory command. As memory bandwidth demands have increased, the amount of data that is prefetched for each read or applied to the memory device for each write has continued to increase as well. However, simply continuing to increase the amount of date prefetched results in a great deal of data being prefetched from a single location in memory. Taken to its extremes, data from an entire page of memory will be prefetched. Unfortunately, such a large amount of data from a single location is often not desired. It would be desirable to be able to prefetch smaller amounts of data from different banks at the same time. Yet the internal structure of memory devices, such as dynamic random access memory ("DRAM") devices precludes them from operating in a manner that provides more flexibility in data prefetch locations.

[003] A portion of a typical DRAM device 10 is shown in Figure 1. The DRAM device 10 includes an address buffer 14 that receives bank, row and column addresses through an external address bus 18. A bi-direction data buffer 20 receives write data through an external data bus 24, and outputs read data to the data bus 24.

Finally, a command decoder 30 receives and decodes memory commands, such as read command and write commands, through an external command bus 34. The DRAM device 10 also includes other circuitry as will be appreciated by one skilled in the art, but, in the interest of brevity, such circuitry has been omitted from Figure 1.

[004] The DRAM device 10 includes first and second memory array banks 40, 44, although additional banks (not shown) may be included. Each of the banks 40, 44 contains a large number of memory cells arranged in rows and columns. In response to read or write command signals received from the command decoder 30 through an internal command bus 50, data are coupled through an internal global data bus 52 to or from one of the banks 40, 44. The particular row to which the data are written or from which the data are read is designated by a row address received from the address buffer 14 through an internal global address bus 54. As is well known in the art, once a row of memory cells has been opened, the memory cells in the open row can be readily accessed. As a result, data in an open row can be easily prefetched. It requires substantially more time to open a different row in the same or a different one of the banks 40, 44. A particular column in an open row from which data are read or to which data are written is identified by a column address received from the address buffer 14.

[005] It can be seen from Figure 1 that the DRAM device 10 has a single internal command bus 50, a single internal data bus 52 and a single internal address bus 54. Although the internal data bus 52 may be divided into separate read data and write data paths, the data bus 52 can serve only one of the banks 40, 44 at a time. Similarly, the single internal command bus 50 and the single internal address bus 54 cannot simultaneously address and provide commands to both of the banks 40, 44. As a result, the DRAM device 10 is incapable of concurrently prefetching data from different rows of memory cells in the same or in different banks 40, 44.

[006] There is therefore a need for a method and system for concurrently accessing different rows of memory cells in the same or in different banks so that prefetches of smaller block of data in different locations can occur while still providing a high memory bandwidth.

SUMMARY OF THE INVENTION

[007] A memory device and method accesses data in a plurality of banks in a memory device through a plurality of internal address buses and a plurality of internal data buses. In response to receiving a first memory address, the memory device initiates a first memory access in a first bank of memory cells at the first memory address. While the first memory access is being processed, a second memory address is received by the memory device. A second memory access is then initiated in a second bank of memory cells in the memory device at the second memory address. This second memory access is initiated while the first memory access is being processed. In another aspect, the memory device initiates a first memory access in a first bank of memory cells responsive to a first memory command. While the first memory access is being processed, a second memory access is initiated in a second bank of memory cells in the memory device responsive to a second memory command. The memory device operating in this manner allows prefetching of data from the first bank of memory cells, and, while data are being transferred from the memory device responsive to the prefetch, a prefetch of data from a second bank of memory cells can be initiated.

BRIEF DESCRIPTION OF THE DRAWINGS

[008] Figure 1 is a block diagram of a portion of a conventional memory device having a single set of address, control and data buses.

[009] Figure 2 is a block diagram of a portion of a memory device according to one example of the present invention in which two sets of address, control and data buses are used.

[010] Figure 3 is a logic diagram of one example of a command decoder used in the memory device of Figure 2.

[011] Figure 4 is a logic diagram of one example of a bank multiplexer logic unit used in the memory device of Figure 2.

[012] Figure 5 is a logic diagram of one example of a address and data multiplexers used in the memory device of Figure 2.

[013] Figure 6 is a block diagram of a computer system according to one example of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[014] Figure 2 shows a DRAM device 60 according to one example of the invention. Like the DRAM device 10 of Figure 1, the DRAM device 60 includes several banks of memory cells, two of which 40, 44 are shown in Figure 2. The DRAM device 60 also includes the external address, data and command buses 18, 24, 34, respectively, that are used in the DRAM 10 as well as the address buffer 14, data buffer 20 and command decoder 30 used in the DRAM 10. A more specific example of the command decoder 30 is shown in Figure 3 and will be explained in connection with that figure.

[015] The DRAM 60 differs from the DRAM 10 primarily in its internal bus structure, which provides it with additional performance capabilities. The DRAM device 60 also includes other circuitry as will be appreciated by one skilled in the art. However, this other circuitry is not particularly germane to the various examples of the invention. Therefore, in the interest of brevity, such circuitry has been omitted from Figure 2.

[016] As shown in Figure 2, a single internal address bus 62 extends from the address buffer 14 to address multiplex logic 66. Similarly, a single internal data bus 64 extends from the data buffer 20 to data multiplex logic 68. The address multiplex logic 66 couples addresses from the address buffer 14 to either of two global address buses 70, 74. As explained in greater detail below, the global address buses 70, 74 allow two of the banks 40, 44 to be concurrently addressed. The data multiplex logic 68 couples data between from the data buffer 20 to either of two global data buses 76, 78. The global data buses 76, 78 allow write data to be coupled to or read data to be coupled from one of the banks 40, 44 at the same time write data are being coupled to or read data are being coupled from another of the banks 40, 44. More specific examples of the

address multiplexer logic 66 and the data multiplexer logic 68 will be explained in connection with Figure 5.

[017] The global address buses 70, 74 and the global data buses 76, 78 are coupled to bank multiplexer logic units 80, 82 associated with the memory array banks 40, 44, respectively. There are also additional bank logic units (not shown) for any additional memory array banks (not shown). Each of the bank multiplexer logic units 80, 82 communicates with its respective bank 40,44 through an address bus 86, and Read/Write ("R/W") Command ("Cmd") bus 88 and a Data bus 90. The bank multiplexer logic units 80, 82 are controlled by select signals applied through lines 92, 94. The units 80, 82 also receive respective R/W Cmd signals from the command decoder 30 through a R/W Cmd bus 96, and applies those signals to the banks 40, 44 through the R/W Cmd bus 88. A more specific example of the bank multiplexer logic units 80, 82 will be explained in connection with Figure 4.

[018] In operation, an external command applied to the DRAM device 60 on the external command bus 34. The command decoder decodes the command, and couples signals corresponding to the decoded command to the bank multiplex logic units 80, 82. The command decoder 30 determines which global address bus 70, 74 should receive an external address applied through the external address bus 18 to the address buffer 14, and generates corresponding select signals. These select signals are applied to the address multiplexer logic 66 so that the logic 66 couples the addresses to the corresponding one of the global address buses 70, 74. The select signals are also applied to the data multiplexer logic 68 to cause the logic 68 to couple the data buffer 20 to the corresponding one of the global data buses 76, 78. Finally, the select signals are applied to the bank multiplexer logic units 80, 82 to cause them to couple the corresponding one of the global address buses 70, 74 and the corresponding one of the global data buses 76, 78 to one of the memory array banks 40, 44.

[019] The external command preferably includes at least one bit identifying the bank 40, 44 to which the command is directed. In response to the external command, including the bank identifying bit(s), the command decoder 30 applies either Bank 0

R/W Cmd signals to the bank multiplexer logic unit 80 or Bank 1 R/W Cmd signals to the bank multiplexer logic unit 82. In response, the selected bank multiplexer logic unit 80 or 82 couples the R/W Cmd signals to the corresponding bank 40 or 44 through the R/W Cmd bus 88. In response to the bank identifying bit(s), the selected bank multiplexer logic unit 80 or 82 also couples an address from the selected global address bus 70 or 74 to the Add. Bus 86, and it couples the selected global data bus 76, 78 to the Data Bus 90. If the memory command is a read command, read data are coupled from a location in the bank 40 or 44 corresponding to the received address to the data buffer 20. If the memory command is a write command, write data from the data buffer 20 is coupled to a location in bank 40 or 44 corresponding to the received address.

[020] The use of two internal address buses 70, 74 and two internal data buses 76, 78 allows the banks 40, 44 to be concurrently accessed in an interleaved manner. As a result, the DRAM device 60 can prefetch data in one of the banks 40 at the same time that data are being prefetched from the other bank 44. While read data are actually being coupled from one of the banks 40, 44, the other of the banks 40, 44 is preferably being prepared to output read data, such as by being equilibrated, as is well known to one skilled in the art. As a result, it may be possible to continuously couple read data from the DRAM device 60. Other modes of operation are also possible.

[021] An example of a command decoder 100 that can be used as the command decoder 30 in the DRAM device 60 of Figure 2 is shown in Figure 3. The portion of the command decoder 100 that generates the Bus1 Select and Bus2 Select signals and that generates the R/W Cmd signals for Bank 0 is shown, it being understood that additional circuitry for generating R/W Cmd signals for other banks are also included. As shown in Figure 3, a Decoded Bank 0 Add bit is active high whenever a bank address for Bank 0 is decoded by an address decoder (not shown) in the DRAM device 60. The active high Bank 0 Add bit enables a plurality of AND gates 102 (only one of which is shown in Figure 3) to pass decoded R/W Cmd signals to the Bank Multiplexer Logic Unit 80 (Figure 2), as explained above. Other sets of the AND

gates 102 (not shown) are enabled by decoded bank bits to pass decoded R/W Cmd signals to the Bank Multiplexer Logic Units for the other banks.

[022] The command decoder 100 also includes a flip-flop 106 that receives at a CLK input One of the Decoded R/W Cmd signals. The data ("D") input of the flip-flop 106 receives the Y output of the flip-flop 106 through an inverter 108. The Y output of the flip-flop 106 therefore toggles with each rising edge of the Decoded R/W Cmd signal. When the Y output of the flip flop 106 is high, it enables an AND gate 110 to make the Bus1 Select signal active high. When the Y output of the flip flop 106 is low, it enables an AND gate 114 through an inverter 116 to make the Bus2 Select signal active high. The Bus1 and Bus2 Select signals are therefore alternately active high responsive to each set of decoded R/W Cmd signals. As a result, the Global Address Buses 70, 74 (Figure 2) and the Global Data Buses 76, 78 are alternately used to couple addresses to and data to and from the banks 40, 44 responsive to each memory command received from the external command bus 34.

[023] One example of a Bank Multiplexer Logic Unit 120 that can be used as the Bank Multiplexer Logic Units 80, 82 in the DRAM device 60 of Figure 2 is shown in Figure 4. The Bank Multiplexer Logic Unit 120 includes an Address Multiplexer 122 that has respective input ports coupled to the Global Address Buses 70, 74, and a single output port coupled to Memory Array Bank 0 (Figure 2). Similarly, a Data Multiplexer 124 has respective inputs coupled to the Global Data Buses 76, 78 and a single output port coupled to Memory Array Bank 0. The Multiplexers 122, 124 are controlled by common Sel1 and Sel2 signals. The Sel1 signal is generated by an AND gate 126, and the Sel2 signal is generated by an AND gate 128. The AND gates 126, 128 are enabled by one of the R/W Cmd signals for Bank 0 being active high. When the AND gates 126, 128 are enabled by a command directed to the respective bank, the AND gate 126 generates the Sel1 signal responsive to the Bus1 Select signal, and the AND gate 128 generates the Sel2 signal responsive to the Bus2 Select signal.

[024] One example of address multiplexer logic 140 and the data multiplexer logic 144 that can be used as the address multiplexer logic 66 and the data multiplexer

logic 68 in the DRAM device 60 of Figure 2 is shown in Figure 5. With reference to Figure 5, the address multiplexer logic 140 and the data multiplexer logic 144 include and address multiplexer 150 and a data multiplexer 154, respectively. The address multiplexer 150 has respective input ports coupled to the Global Address Buses 70, 74, and a single output port coupled to Memory Array Bank 0 (Figure 2). Similarly, the Data Multiplexer 1154 has respective inputs coupled to the Global Data Buses 76, 78 and a single output port coupled to Memory Array Bank 0. The Multiplexers 150, 154 are controlled by common Sel1 and Sel2 signals in the same way that the Address Multiplexer 122 (Figure 4) and Data Multiplexer 124 in the Bank Multiplexer Logic Unit 120 are controlled. As explained above, the Sel1 and Sel2 signals are generated by the Bank Multiplexer Logic Unit 120 shown in Figure 4.

[025] The DRAM device 60 or another example of a memory device according to the invention can be used in various electronic systems. For example, it may be used in a processor-based system, such as a computer system 200 shown in Figure 6. The computer system 200 includes a processor 202 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 202 includes a processor bus 204 that normally includes an address bus, a control bus, and a data bus. In addition, the computer system 200 includes one or more input devices 214, such as a keyboard or a mouse, coupled to the processor 202 to allow an operator to interface with the computer system 200. Typically, the computer system 200 also includes one or more output devices 216 coupled to the processor 202, such output devices typically being a printer or a video terminal. One or more data storage devices 218 are also typically coupled to the processor 202 to allow the processor 202 to store data in or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 218 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs). The processor 202 is also typically coupled to cache memory 226, which is usually static random access memory ("SRAM"), and to the DRAM 60 through a memory controller 230. The memory controller 230 normally includes a control bus 236 and an address bus 238 that are

coupled to the DRAM 60. A data bus 240 is coupled from the DRAM 60 to the processor bus 204 either directly (as shown), through the memory controller 230, or by some other means.

[026] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, it will be understood by one skilled in the art that various modifications may be made without deviating from the spirit and scope of the invention. For example, Figures 3 and 4 show various components implemented using specific logic elements, such as AND gates. However, it will be understood that these and other components can be implemented with other types of gates or logic elements or other circuitry. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

What is claimed is:

1. A memory device, comprising:

an external port coupling memory commands, memory addresses, and write data into the memory device, the external port further coupling read data from the memory device;

a plurality of internal address buses;

a plurality of internal data buses;

an address coupling circuit operable to couple memory address signals corresponding to the memory addresses from the external port to a selected one of the internal address buses;

a data coupling circuit operable to couple write data signals corresponding to the write data from the external port to a selected one of the internal data buses, the data coupling circuit further being operable to couple read data signals corresponding to the read data from a selected one of the internal data buses to the external port;

a plurality of banks of memory cells;

a bank coupling circuit for each of the banks of memory cells, the bank coupling circuit being operable to couple the memory address signals from a selected one of the internal address buses to the respective bank, the bank coupling circuit further being operable to couple the write data signals from a selected one of the internal data buses to the respective bank and to couple the read data signals from the respective bank to a selected one of the internal data buses; and

control circuitry coupled to control inputs of the address coupling circuit, the data coupling circuit, and the bank coupling circuit, the control circuitry being operable to apply signals to the address coupling circuit to cause the address coupling

circuit to select the internal address bus to which the address signals are coupled, to apply signals to the data coupling circuit to cause the data coupling circuit to select the internal data bus to which the write data signals are coupled and from which the read data signals are coupled, and to apply signals to the bank coupling circuit to cause the bank coupling circuit to select the internal address bus from which the address signals are coupled and to select the internal data bus to and from which write data and read data are coupled.

2. The memory device of claim 1 wherein the banks of memory cells comprise banks of dynamic random access memory cells.

3. The memory device of claim 1, further comprising a command decoder receiving the memory commands from the external port and decoding the received commands to output corresponding command signals.

4. The memory device of claim 3 wherein the command decoder comprise at least a portion of the control circuitry.

5. The memory device of claim 3, further comprising a command bus coupled to receive the command signals from the command decoder, and wherein each of the bank coupling circuits is further operable to couple the command signals from the command bus to the respective bank.

6. The memory device of claim 5 wherein each of the bank coupling circuit receives respective address signals indicative of an access to the respective bank, and wherein each of the bank coupling circuits is operable to couple the command signals from the command bus to the respective bank responsive to receiving the address signal indicative of an access to the respective bank.

7. The memory device of claim 1 wherein the external port comprises a command bus port receiving the memory commands, an address bus port receiving the memory addresses, and a data bus port receiving the write data and outputting the read data from.

8. The memory device of claim 1 wherein the address coupling circuit comprises an address multiplexer having an input bus port coupled to receive the memory addresses from the external port and a plurality of output bus ports coupled to respective ones of the plurality of internal address buses.

9. The memory device of claim 1 wherein the data coupling circuit comprises a data multiplexer having a first bus port coupled to the external port and a plurality of output bus ports coupled to respective ones of the plurality of internal data buses.

10. The memory device of claim 1 wherein the control circuitry comprises a logic circuit generating signals that are applied to the address coupling circuit, the data coupling circuit and the bank coupling circuit to sequentially each of the internal address buses and internal data buses in sequence, the logic circuit being triggered by the memory commands applied to the external port.

11. The memory device of claim 10 wherein the logic circuit comprises:

a toggling flip-flop having a clock input coupled to receive a signal that is generated each time one of the memory commands is applied to the external port; and

a plurality of logic gates coupled to the toggling flip-flop, each of the logic generating a respective signal that sequentially selects a respective one of the

internal address buses and a respective one of the internal data buses each time the flip-flop toggles.

12. The memory device of claim 1 wherein the bank coupling circuit comprises an address multiplexer having an output port coupled to the respective bank and a plurality of input bus ports coupled to respective ones of the plurality of internal address buses; and a data multiplexer having an output port coupled to the respective bank and a plurality of input bus ports coupled to respective ones of the plurality of internal data buses.

13. A processor-based system, comprising

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device comprising:

an external port coupled to the processor bus to receive memory commands, memory addresses, and write data from the processor and to couple read data to the processor;

a plurality of internal address buses;

a plurality of internal data buses;

an address coupling circuit operable to couple memory address signals corresponding to the memory addresses from the external port to a selected one of the internal address buses;

a data coupling circuit operable to couple write data signals corresponding to the write data from the external port to a selected one of the internal data buses, the data coupling circuit further being operable to couple

read data signals corresponding to the read data from a selected one of the internal data buses to the external port;

a plurality of banks of memory cells;

a bank coupling circuit for each of the banks of memory cells, the bank coupling circuit being operable to couple the memory address signals from a selected one of the internal address buses to the respective bank, the bank coupling circuit further being operable to couple the write data signals from a selected one of the internal data buses to the respective bank and to couple the read data signals from the respective bank to a selected one of the internal data buses; and

control circuitry coupled to control inputs of the address coupling circuit, the data coupling circuit, and the bank coupling circuit, the control circuitry being operable to apply signals to the address coupling circuit to cause the address coupling circuit to select the internal address bus to which the address signals are coupled, to apply signals to the data coupling circuit to cause the data coupling circuit to select the internal data bus to which the write data signals are coupled and from which the read data signals are coupled, and to apply signals to the bank coupling circuit to cause the bank coupling circuit to select the internal address bus from which the address signals are coupled and to select the internal data bus to and from which write data and read data are coupled.

14. The processor-based system of claim 13 wherein the banks of memory cells comprise banks of dynamic random access memory cells.

15. The processor-based system of claim 13, further comprising a command decoder receiving the memory commands from the external port and decoding the received commands to output corresponding command signals.

16. The processor-based system of claim 15 wherein the command decoder comprise at least a portion of the control circuitry.

17. The processor-based system of claim 15, further comprising a command bus coupled to receive the command signals from the command decoder, and wherein each of the bank coupling circuits is further operable to couple the command signals from the command bus to the respective bank.

18. The processor-based system of claim 17 wherein each of the bank coupling circuit receives respective address signals indicative of an access to the respective bank, and wherein each of the bank coupling circuits is operable to couple the command signals from the command bus to the respective bank responsive to receiving the address signal indicative of an access to the respective bank.

19. The processor-based system of claim 13 wherein the external port comprises a command bus port receiving the memory commands, an address bus port receiving the memory addresses, and a data bus port receiving the write data and outputting the read data from.

20. The processor-based system of claim 13 wherein the address coupling circuit comprises an address multiplexer having an input bus port coupled to receive the memory addresses from the external port and a plurality of output bus ports coupled to respective ones of the plurality of internal address buses.

21. The processor-based system of claim 13 wherein the data coupling circuit comprises a data multiplexer having a first bus port coupled to the external port and a plurality of output bus ports coupled to respective ones of the plurality of internal data buses.

22. The processor-based system of claim 13 wherein the control circuitry comprises a logic circuit generating signals that are applied to the address coupling circuit, the data coupling circuit and the bank coupling circuit to sequentially each of the internal address buses and internal data buses in sequence, the logic circuit being triggered by the memory commands applied to the external port.

23. The processor-based system of claim 22 wherein the logic circuit comprises:

a toggling flip-flop having a clock input coupled to receive a signal that is generated each time one of the memory commands is applied to the external port; and

a plurality of logic gates coupled to the toggling flip-flop, each of the logic generating a respective signal that sequentially selects a respective one of the internal address buses and a respective one of the internal data buses each time the flip-flop toggles.

24. The processor-based system of claim 13 wherein the bank coupling circuit comprises an address multiplexer having an output port coupled to the respective bank and a plurality of input bus ports coupled to respective ones of the plurality of internal address buses; and a data multiplexer having an output port coupled to the respective bank and a plurality of input bus ports coupled to respective ones of the plurality of internal data buses.

25. A method of accessing data in a memory device, comprising:

coupling a first memory address to the memory device;

initiating a first memory access in a first bank of memory cells in the memory device at the first memory address;

while the first memory access is being processed, coupling a second memory address to the memory device;

initiating a second memory access in a second bank of memory cells in the memory device at the second memory address while the first memory access is being processed, the second bank being different from the first bank.

26. The method of claim 25 further comprising:

coupling a first memory command to the memory device along with the first memory address; and

coupling a second memory command to the memory device along with the second memory address.

27. The method of claim 26 wherein the first memory command is different from the second memory command.

28. The method of claim 25, further comprising:

while the second memory access is being processed, coupling a third memory address to the memory device; and

initiating a third memory access in the first bank of memory cells in the memory device at the third memory address while the second memory access is being processed in the second bank of memory cells.

29. The method of claim 25 wherein the first and second banks of memory cells comprise dynamic random access memory cells.

30. A method of accessing data in a memory device, comprising:

coupling a first memory command to the memory device;

initiating a first memory access in a first bank of memory cells in the memory device responsive to the first memory command;

while the first memory access is being processed, coupling a second memory command to the memory device;

initiating a second memory access in a second bank of memory cells in the memory device responsive to the second memory command while the first memory access is being processed, the second bank being different from the first bank.

31. The method of claim 30 wherein the first memory command is different from the second memory command.

32. The method of claim 30, further comprising:

while the second memory access is being processed, coupling a third memory command to the memory device; and

initiating a third memory access in the first bank of memory cells in the memory device responsive to the third memory command while the second memory access is being processed in the second bank of memory cells.

33. The method of claim 30 wherein the first and second banks of memory cells comprise dynamic random access memory cells.

34. In a processor based system having a processor coupled to system memory having a plurality of banks of memory cells, a method of prefetching data in the system memory, comprising:

prefetching data from a first of the banks of memory cells in the system memory; and

while data are being transferred from the system memory to the processor responsive to the prefetching of data from the first bank of memory cells, initiating a prefetch of data from a second of the banks of memory cells in the system memory.

35. The method of claim 34 wherein the system memory comprises a dynamic random access memory device.

36. The method of claim 34 wherein the act of initiating a prefetch of data from a second of the banks of memory cells in the system memory comprises coupling a memory command and a memory address to the system memory.

37. The method of claim 34 wherein each of the banks have a plurality of pages of memory cells, and wherein the act of prefetching data from a first of the banks of memory cells comprises prefetching data from less than an entire page of memory cells in the first bank, and wherein the act of initiating a prefetch of data from a second of the banks of memory cells in the system memory comprises initiating a prefetch of data from less than an entire page of memory cells in the second bank.

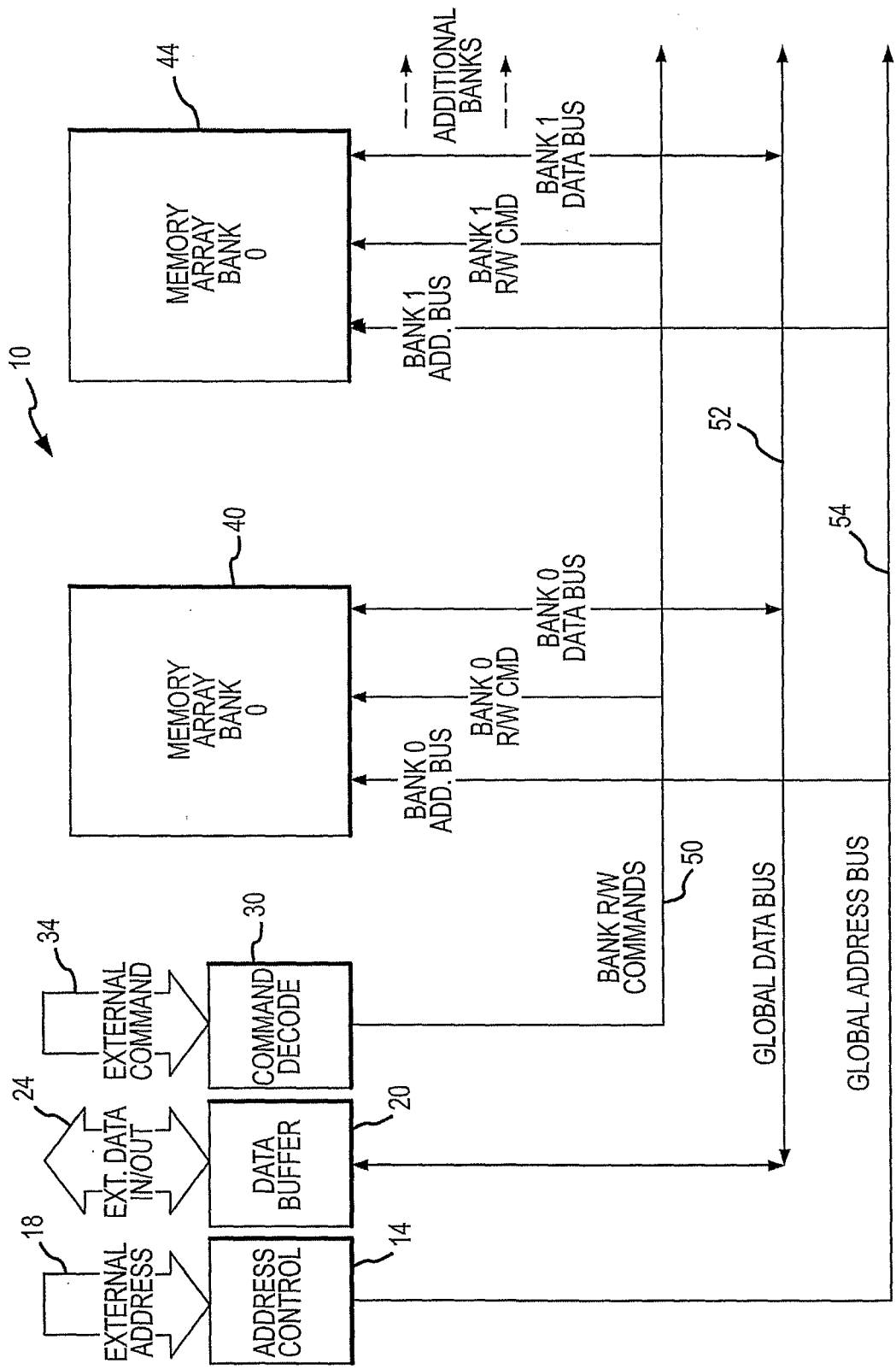

FIGURE 1
(PRIOR ART)

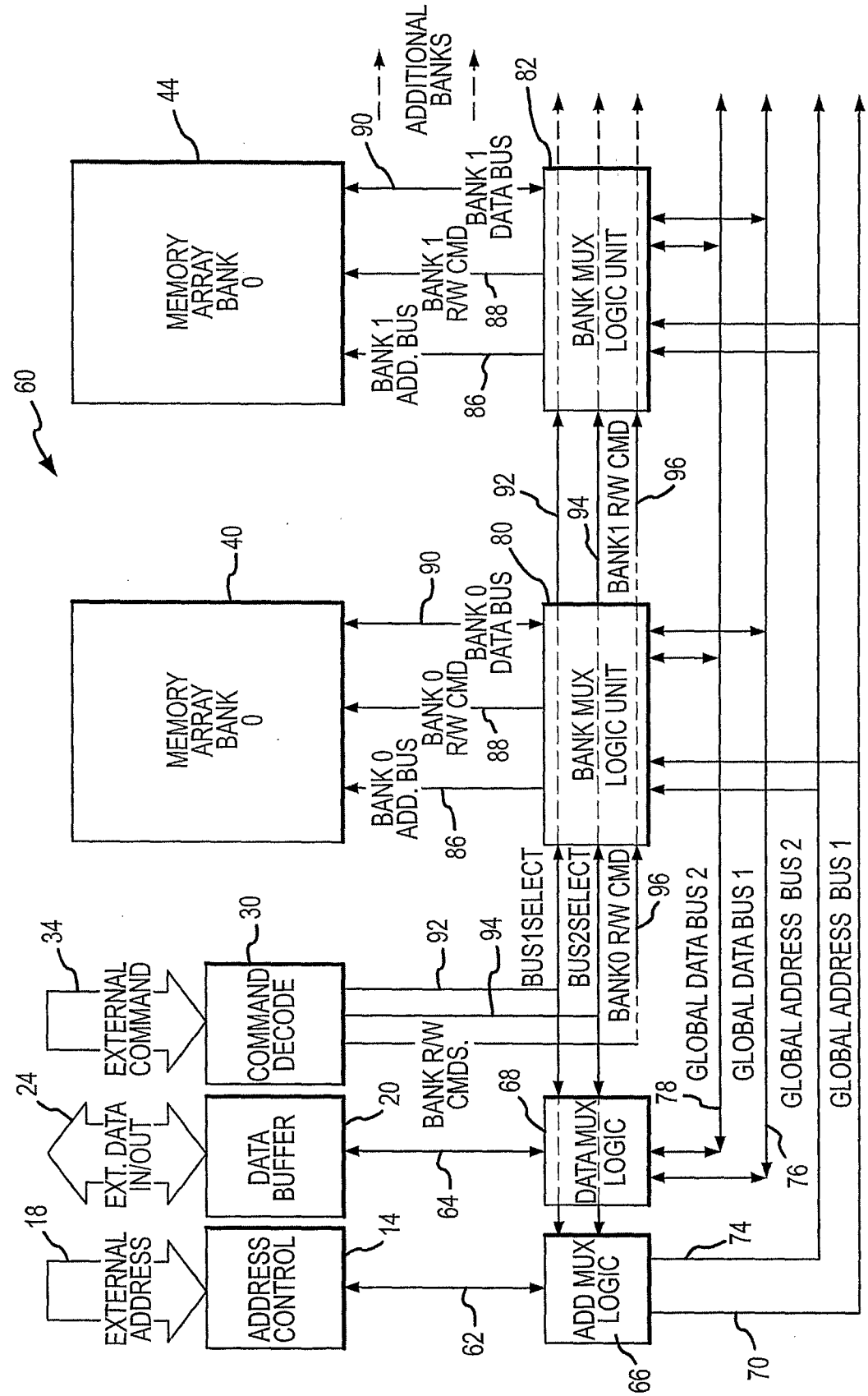
60
MEMORY ARRAY BANK 0
44
40
ADDITIONAL BANKS
90
82
80
92
94
96
86
88
BANK 1 ADD. BUS
BANK 1 R/W CMD
BANK 1 DATA BUS
BANK 0 ADD. BUS
BANK 0 R/W CMD
BANK 0 DATA BUS
BANK MUX LOGIC UNIT
BANK1 R/W CMD
BANK0 R/W CMD
BUS1SELECT
BUS2SELECT
GLOBAL DATA BUS 2
GLOBAL DATA BUS 1
GLOBAL ADDRESS BUS 2
GLOBAL ADDRESS BUS 1
EXTERNAL COMMAND
34
COMMAND DECODE
30
BANK R/W CMDS.
EXT. DATA IN/OUT
24
DATA BUFFER
20
68
64
78
76
EXTERNAL ADDRESS
18
ADDRESS CONTROL
14
62
DATA MUX LOGIC
ADD MUX LOGIC
74
66
70

FIGURE 2

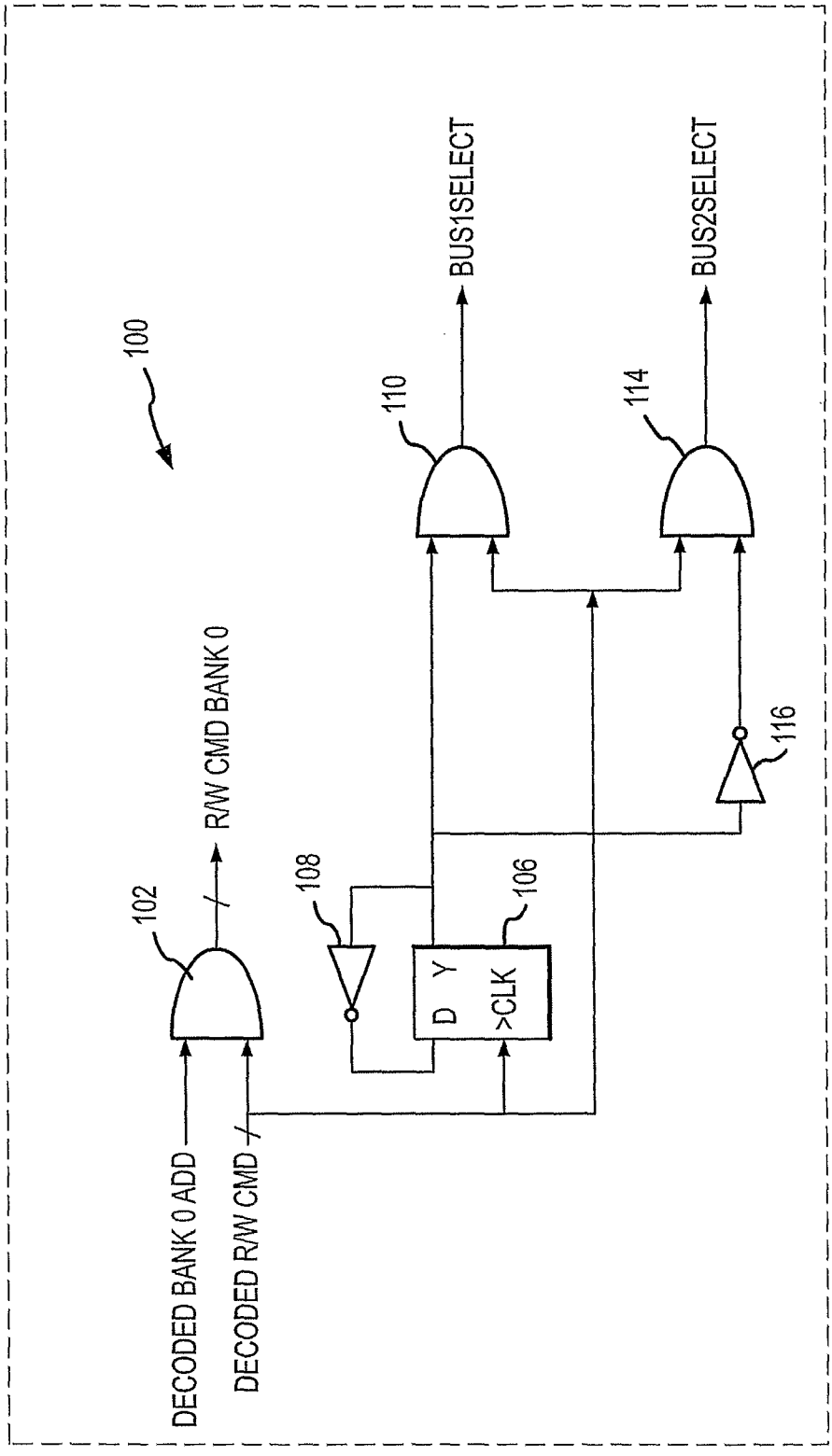
100
BUS1SELECT
BUS2SELECT
110
114
116
R/W CMD BANK 0
102
108
106
D Y
>CLK
DECODED BANK 0 ADD
DECODED R/W CMD

FIGURE 3

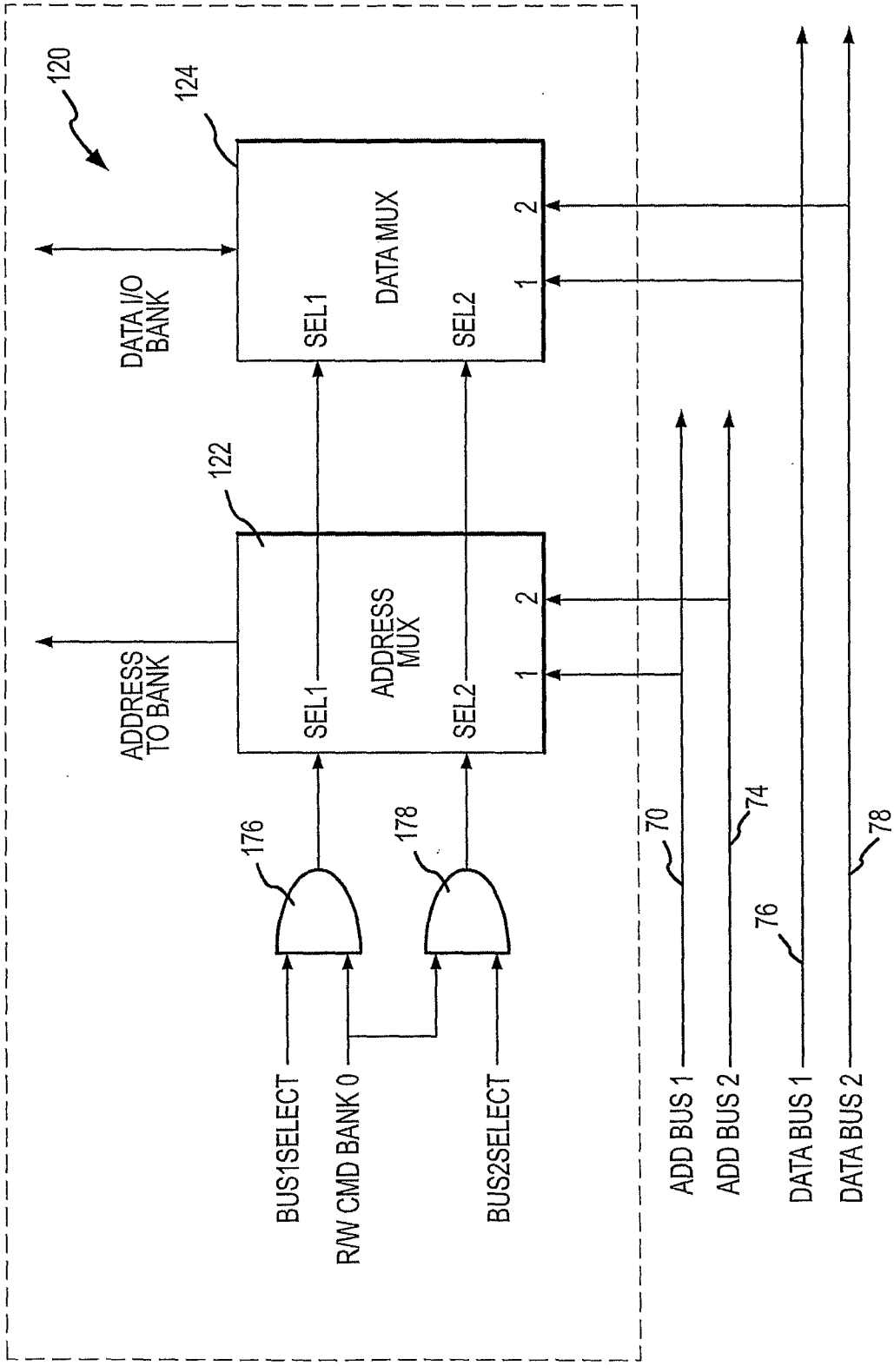
120
124
DATA I/O BANK
DATA MUX
SEL1
SEL2
2
1
122
ADDRESS TO BANK
ADDRESS MUX
SEL1
SEL2
2
1
176
178
BUS1SELECT
R/W CMD BANK 0
BUS2SELECT
70
74
76
78
ADD BUS 1
ADD BUS 2
DATA BUS 1
DATA BUS 2

FIGURE 4

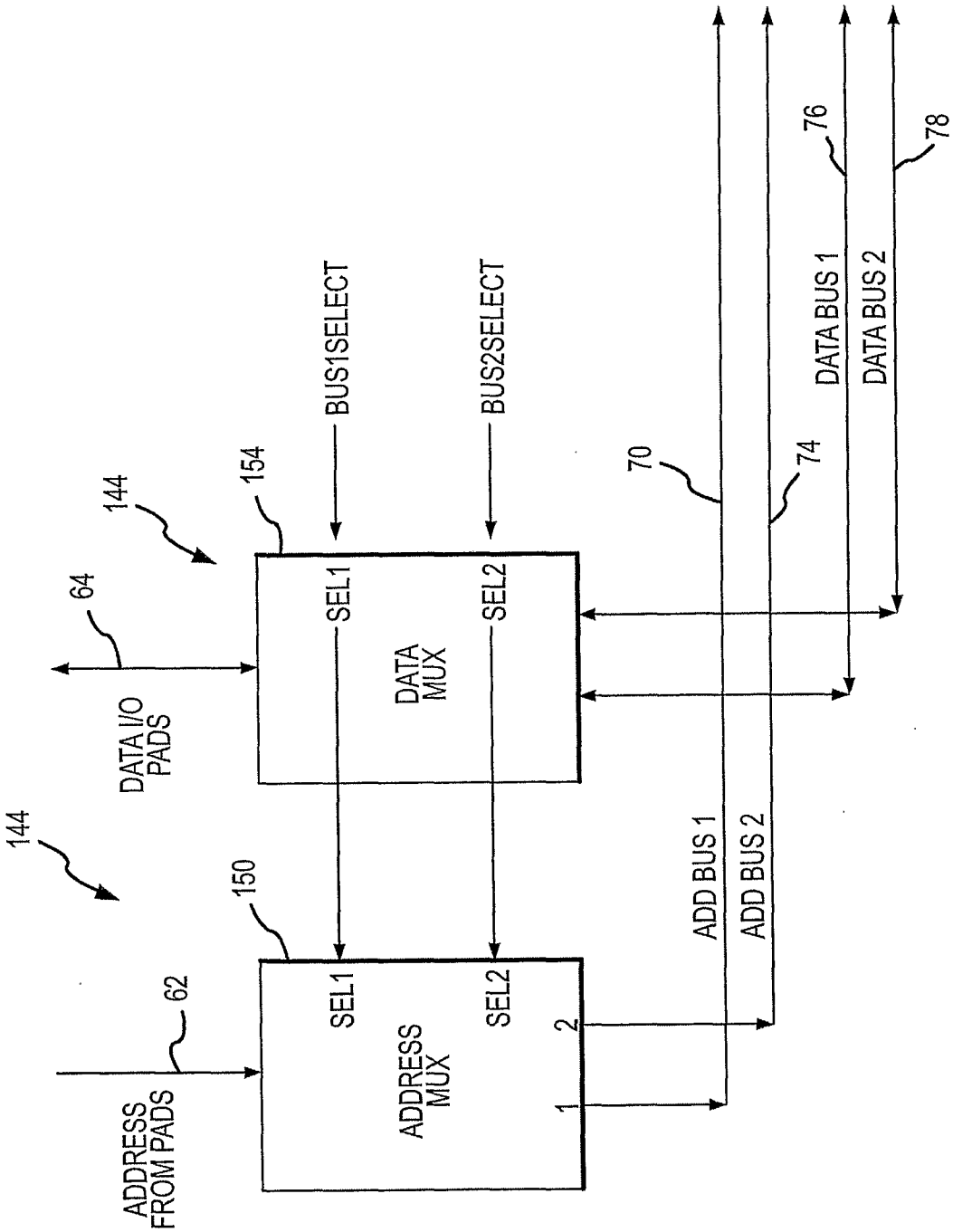
144
154
BUS1SELECT
BUS2SELECT
70
74
76
78
DATA BUS 1
DATA BUS 2
64
DATA I/O PADS
SEL1
DATA MUX
SEL2
144
150
ADD BUS 1
ADD BUS 2
62
ADDRESS FROM PADS
SEL1
ADDRESS MUX
SEL2
2
1

FIGURE 5

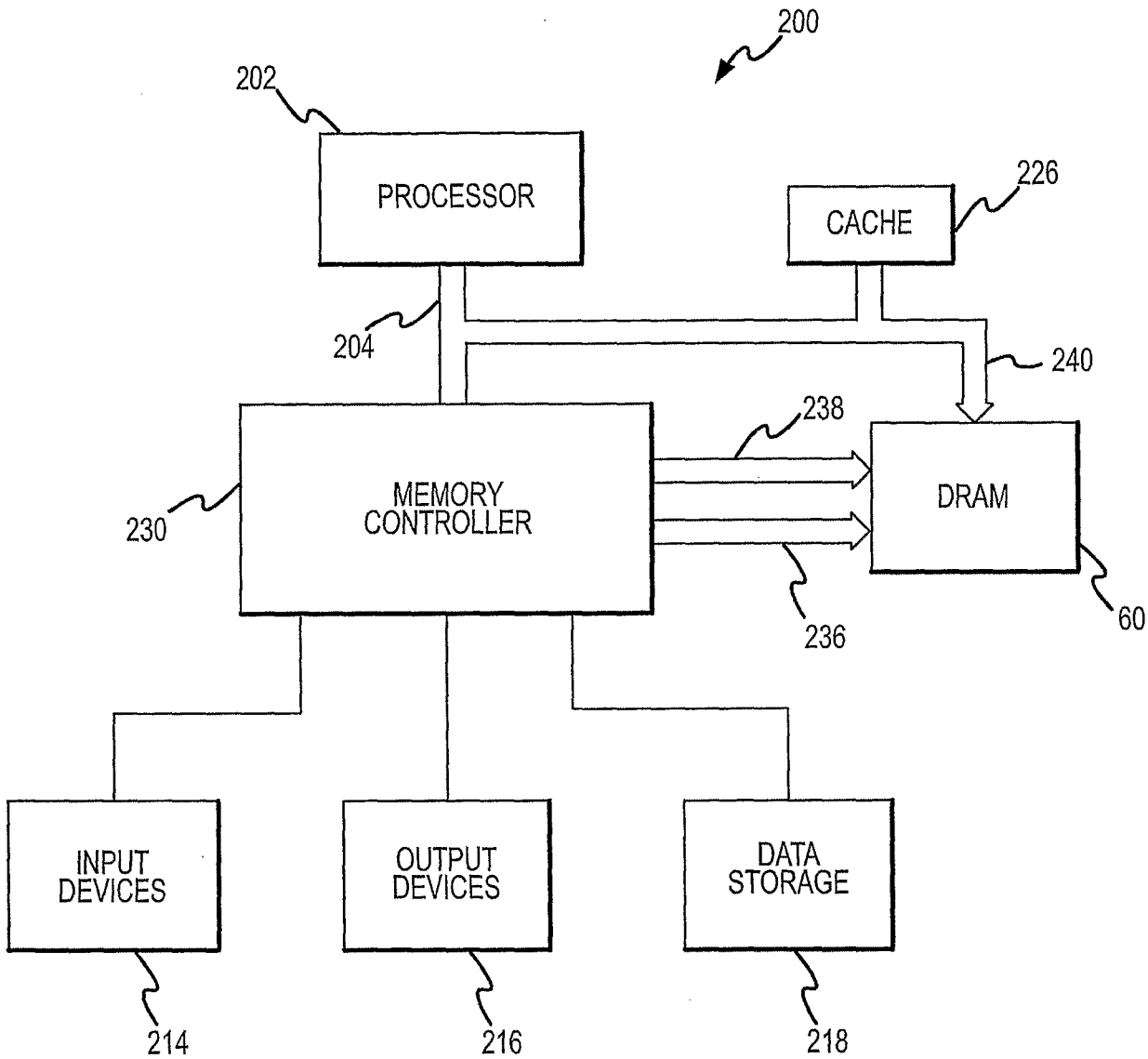
200
202
PROCESSOR
CACHE
226
204
240
238
MEMORY CONTROLLER
230
DRAM
60
236
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE
214
216
218

FIGURE 6