(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 July 2011 (14.07.2011)

PCT

(10) International Publication Number
WO 2011/084706 A2

(51) International Patent Classification:
H01L 23/48 (2006.01)

(21) International Application Number:
PCT/US2010/061143

(22) International Filing Date:
17 December 2010 (17.12.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/640,111 17 December 2009 (17.12.2009) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

[Continued on next page]

(54) Title: APPARATUS AND METHOD FOR CONTROLLING SEMICONDUCTOR DIE WARPAGE

(57) Abstract: A semiconductor die has through silicon vias arranged to reduce warpage. The through silicon vias adjust the coefficient of thermal expansion of the semiconductor die, permit substrate deformation, and also relieve residual stress. The through silicon vias may be located in the edges and/or corners of the semiconductor die. The through silicon vias are stress relief vias that can be supplemented with round corner vias to reducing warpage of the semiconductor die.

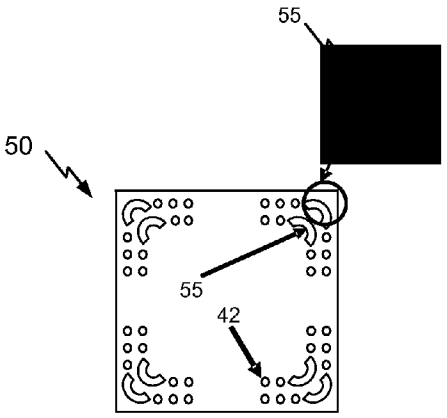


FIG. 5

WO 2011/084706 A2

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

APPARATUS AND METHOD FOR CONTROLLING SEMICONDUCTOR DIE WARPAGE

TECHNICAL FIELD

[0001] The present disclosure generally relates to semiconductor die manufacturing. More specifically, the present disclosure relates to controlling warpage while manufacturing semiconductor dies.

BACKGROUND

[0002] Residual stress in semiconductor wafers and dies causes warpage. For example, deposited materials (e.g., to create transistors) on the wafer can be engineered to have a different stress than the substrate resulting in unbalanced stress. In other cases, the stresses are not engineered but merely result from different materials. When the stress between the substrate and deposited materials is unbalanced, the substrate may warp or bend to reach an equilibrium stress.

[0003] In addition, change of temperature experienced by a packaged die can cause warpage. The coefficient of thermal expansion (CTE) of the package differs from the CTE of the die. Warpage occurs as a result of the CTE mismatch between the material sets of the package and die. The warpage is exacerbated when there is a substantial thickness difference between the package and the die.

[0004] One example of a product having a substantial thickness difference between the package and the die is a stacked IC. Thin wafers are conventionally used in stacked ICs to assist fabrication of through silicon vias. In some cases the die may be thinned to less than 50 microns without changing the thickness of a 1mm package. As a result of the substantial thickness difference, severe warpage may occur.

[0005] When the warping is severe, inadequate bonding of the die to the package occurs. In other words, the warpage prevents some bumps or pillars from attaching to the substrate during the package assembly process. If the warpage occurs after assembly, the bumps or pillars may de-attach when an end user device is with the consumer.

[0006] As seen in FIGURE 3, a warped package substrate 310 is not coupled to a warped die 320 in the center. That is, centrally located interconnects 330 do not contact the package substrate 310. Although not shown, the thermal mismatch can stress the interconnects 330 in the corner, disconnecting the package substrate 310 from the die 320.

[0007] In addition, interconnect fatigue life decreases when the coefficient of thermal expansion (CTE) between the die and package substrate are mismatched. When the temperature changes, the assembly bends to accommodate the mismatch in expansion. Based on measurements and mechanical models, warpage appears to occur at a periphery of the die, especially at the corners. The strain concentrated at the corner of chip results in a crack that propagates out from the corner. As the crack propagates, it opens up either the chip-underfill interface or another weak interface, causing either interconnect fatigue or electrical failure in the chip dielectric.

[0008] Although stress engineering solutions involving die dielectric interfaces exist, such solutions are relatively complex and expensive. Thus, a need exists for efficiently controlling warpage of a die.

BRIEF SUMMARY

[0009] According to an aspect of the present disclosure, a semiconductor die has through silicon vias located in a peripheral region. The through silicon vias reduce warpage of the semiconductor die.

[0010] In another aspect, a method for manufacturing a semiconductor die includes fabricating a plurality of non-signal carrying through silicon vias in a peripheral region of the semiconductor die to reduce warpage of the die.

[0011] In yet another aspect, a semiconductor die has means for increasing a coefficient of thermal expansion (CTE) of the semiconductor die located in a peripheral region of the semiconductor die. The CTE increasing means reduces warpage of the semiconductor die.

[0012] In still another aspect, a computerized method for designing a semiconductor die includes determining locations for stress relief through silicon vias in order to reduce die warpage.

[0013] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description that

follows may be better understood. Additional features and advantages will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the technology of the invention as set forth in the appended claims. The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] For a more complete understanding of the present invention, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0015] FIGURE 1 is a block diagram showing an exemplary wireless communication system in which an embodiment of the invention may be advantageously employed.

[0016] FIGURE 2 is a block diagram illustrating a design workstation for circuit and layout design of the disclosed semiconductor die.

[0017] FIGURE 3 is a block diagram illustrating a warped semiconductor die and packaging substrate.

[0018] FIGURE 4 is a block diagram illustrating a top view of a semiconductor die have stress relief vias.

[0019] FIGURE 5 is a block diagram illustrating a top view of a semiconductor die have stress relief vias and round corner vias.

DETAILED DESCRIPTION

[0020] FIGURE 1 is a block diagram showing an exemplary wireless communication system 100 in which an embodiment of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 1 shows three remote units 120, 130, and 150 and two base stations 140. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 120, 130, and 150 include IC devices 125A, 125B and 125C, that include the disclosed semiconductor die. It will be recognized that any device containing an IC may also include the die disclosed here, including the base stations, switching devices, and network equipment. FIGURE 1 shows forward link signals 180 from the base station 140 to the remote units 120, 130, and 150 and reverse link signals 190 from the remote units 120, 130, and 150 to base stations 140.

[0021] In FIGURE 1, the remote unit 120 is shown as a mobile telephone, the remote unit 130 is shown as a portable computer, and the remote unit 150 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be mobile phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, GPS enabled devices, navigation devices, set top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof. Although FIGURE 1 illustrates remote units according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. Embodiments of the disclosure may be suitably employed in any device which includes integrated circuitry.

[0022] FIGURE 2 is a block diagram illustrating a design workstation for circuit and layout design of the disclosed semiconductor integrated circuit. A design workstation 200 includes a hard disk 201 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 200 also includes a display to facilitate design of a circuit and layout 210. The circuit and layout 210 may include the via configuration, as disclosed below. A storage medium 204 is provided for tangibly storing the circuit and layout design 210. The circuit and layout design 210 may be stored on the storage medium 204 in a file format such as GDSII or GERBER. The storage medium 204 may be a CD-ROM, DVD, hard disk, flash

memory, or other appropriate device. Furthermore, the design workstation 200 includes a drive apparatus 203 for accepting input from or writing output to the storage medium 204.

[0023] Data recorded on the storage medium 204 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 204 facilitates the design of the circuit and layout 210 by decreasing the number of processes for designing semiconductor ICs.

[0024] According to the present disclosure, through silicon vias with conductive fill (e.g., metal) are manufactured within a semiconductor die (or wafer) to control warpage. The through silicon vias improve the die/substrate coefficient of thermal expansion (CTE) match. Thus, fatigue life and reliability of the interconnect is increased.

[0025] Moreover, the through silicon vias relieve residual stress and create more space for the substrate to deform, mitigating warpage. In one embodiment, the through silicon vias are stress relief vias and round corner vias provided in a periphery of the die.

[0026] As seen in FIGURE 4, a die 40 includes stress relief vias 42. The stress relief vias are through silicon vias disposed around the die corner to control the warpage and also release the residual stress. In addition, stress relief vias 44 can be disposed centrally to redistribute residual stress. The stress relief vias 44 can help to reduce or increase stress of critical functional blocks of the die 40 to meet design parameters.

[0027] In one embodiment, the stress relief vias 42 are filled with metal, helping improve the coefficient of thermal expansion (CTE) mismatch. Exemplary non-limiting fill materials include copper and tungsten. Selection of the appropriate fill material depends on desired package performance and cost. Tungsten has a larger modulus but smaller coefficient of thermal expansion (CTE). For example in a stacked die (two tier) package, a tungsten fill material results in lower stress in the vias and higher stress in die to die interconnects between tiers of the stack. Therefore, a

performance trade off exists between vias and interconnects when choosing the fill material.

[0028] In one embodiment, the stress relief vias 42, 44 do not carry signals. However, in another embodiment the stress relief vias 42, 44 do carry signals

[0029] The number and exact locations of the stress relief vias 42, 44 varies from die to die based on, *inter alia,* the die size, the via diameter and the fill material of the stress relief via. The desired number of stress relief vias 42, 44 and locations of the stress relief vias 44 can be computed during the semiconductor die design phase by analyzing a thermal mechanical model of the die 40. One advantage of locating the stress relief vias 42 in the corner of the die is that this area is often not used for functional vias of the die 40.

[0030] As seen in FIGURE 5, a die 50 includes round corner vias 55, in addition to stress relief vias 42. In one embodiment, the stress relief vias 42 are the primary mechanism for stress relief. If the stress relief vias are inadequate to relieve the stress by themselves, the round corner vias 55 are employed as a secondary mechanism. In another embodiment, the round corner vias 55 are the primary mechanism.

[0031] The round corner vias 55 can also be filled with metal to help increase the coefficient of thermal expansion of the die 50. By increasing the coefficient of thermal expansion of the die 50, the coefficient of thermal expansion of the die 50 will better match the coefficient of thermal expansion of the package (not shown), reducing the warpage. Moreover, the additional die cut out area creates more room for substrate deformation and relieves residual stress.

[0032] The format of the round corner via 55 can be varied. In one embodiment, as seen in the zoom view, the format is an array of through silicon vias.

[0033] The specific arrangement of round corner vias 55 and stress relief vias 42 can be determined based upon thermal mechanical modeling and the amount of expected warpage. If the warpage is more significant, round corner vias 55 can be provided because the round corner vias 55 remove more die material than the stress relief vias 42, giving the die 50 more space to deform. As a general rule of thumb, if the via area to die area ratio increases, then the warpage is more controlled. In other words, removing more die material better controls warpage.

[0034] In one embodiment, the area not used for the function of the die 50 influences the decision on where to locate the stress relief vias 42, 44 and the round

corner vias 55. Alternatively, when the warpage issue becomes more critical, the functional blocks of the die 50 are designed to accommodate the stress relief vias 42, 44 and the round corner vias 55

[0035] The stress relief vias 42, 44 and the round corner vias 55 can be manufactured during the conventional through silicon via formation process. Therefore, no additional manufacturing processes are needed. Moreover, because the stress relief vias 42, 44 and the round corner vias 55 are easily manufactured, little to no extra manufacturing costs are added. Finally, the stress relief vias 42, 44 and the round corner vias 55 enhance reliability of package substrate/die interconnects by reducing the CTE mismatch. That is, the interconnect fatigue life is increased.

[0036] Although the terminology "through silicon via" includes the word silicon, it is noted that through silicon vias are not necessarily constructed in silicon. Rather, the material can be any device substrate material.

[0037] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A semiconductor die comprising:

a plurality of through silicon vias located in a peripheral region of the semiconductor die, the through silicon vias reducing warpage of the semiconductor die.

2. The semiconductor die of claim 1, in which the through silicon vias are non-signal carrying through silicon vias.

3. The semiconductor die of claim 2, further comprising at least one additional non-signaling carrying through silicon via located in a central region proximate to a functional block of the semiconductor die.

4. The semiconductor die of claim 2, in which the through silicon vias comprise stress relief vias.

5. The semiconductor die of claim 4, in which the stress relief vias comprise round corner vias.

6. The semiconductor die of claim 5, in which each round corner via comprises an array of through silicon vias.

7. The semiconductor die of claim 2, in which the peripheral region comprises at least one corner of the semiconductor die.

8. The semiconductor die of claim 2, in which the peripheral region comprises at least one edge of the semiconductor die.

9. The semiconductor die of claim 1, integrated into an item selected from a group consisting of a handheld device and a personal computer.

10. The semiconductor die of claim 1, integrated into a stacked IC.

11. A method for manufacturing a semiconductor die comprising:

fabricating a plurality of non-signal carrying through silicon vias in a peripheral region of the semiconductor die to reduce warpage of the die.

12. The method of claim 11, further comprising fabricating signal carrying through silicon vias substantially concurrently with fabricating the non-signal carrying through silicon vias.

13. The method of claim 11, further comprising fabricating at least one additional non-signaling carrying through silicon via in a central region proximate to a functional block of the semiconductor die.

14. The method of claim 11, in which the fabricating comprises fabricating at least one array of non-signal carrying through silicon vias in a corner of the semiconductor die.

15. The method of claim 14, in which fabricating the at least one array comprises fabricating at least one round corner via.

16. The method of claim 11, further comprising integrating the semiconductor die into an item selected from a group consisting of a handheld device and a personal computer.

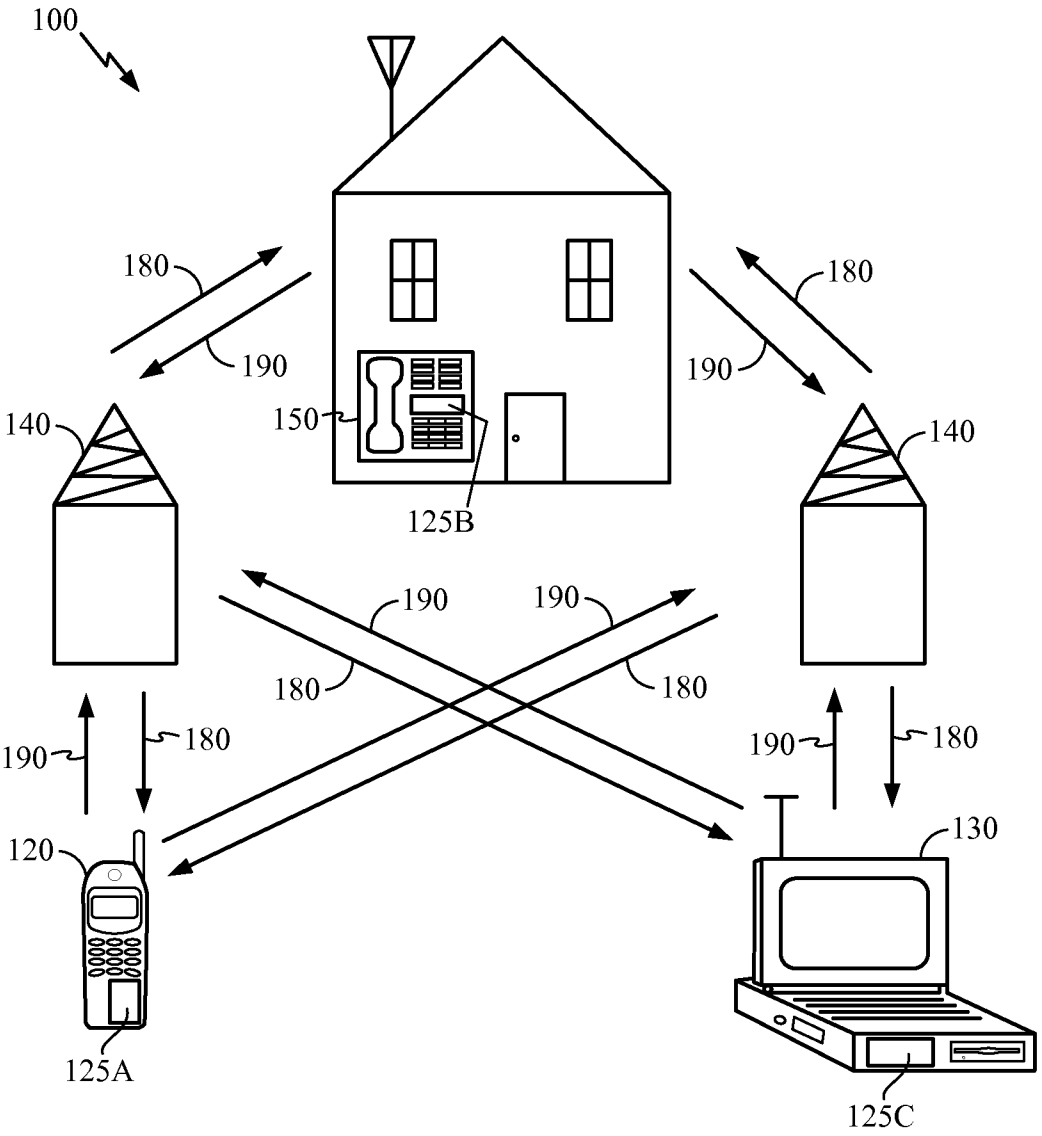
17. A semiconductor die comprising:

means for increasing a coefficient of thermal expansion (CTE) of the semiconductor die located in a peripheral region of the semiconductor die, the CTE increasing means reducing warpage of the semiconductor die.

18. A computerized method for designing a semiconductor die, comprising:

determining locations for stress relief through silicon vias in order to reduce die warpage.

19. The computerized method of claim 18, in which the determining comprises analyzing a coefficient of thermal expansion of the semiconductor die relative to a coefficient of thermal expansion of a package substrate.


100
180
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125B
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125A
125C

FIG. 1

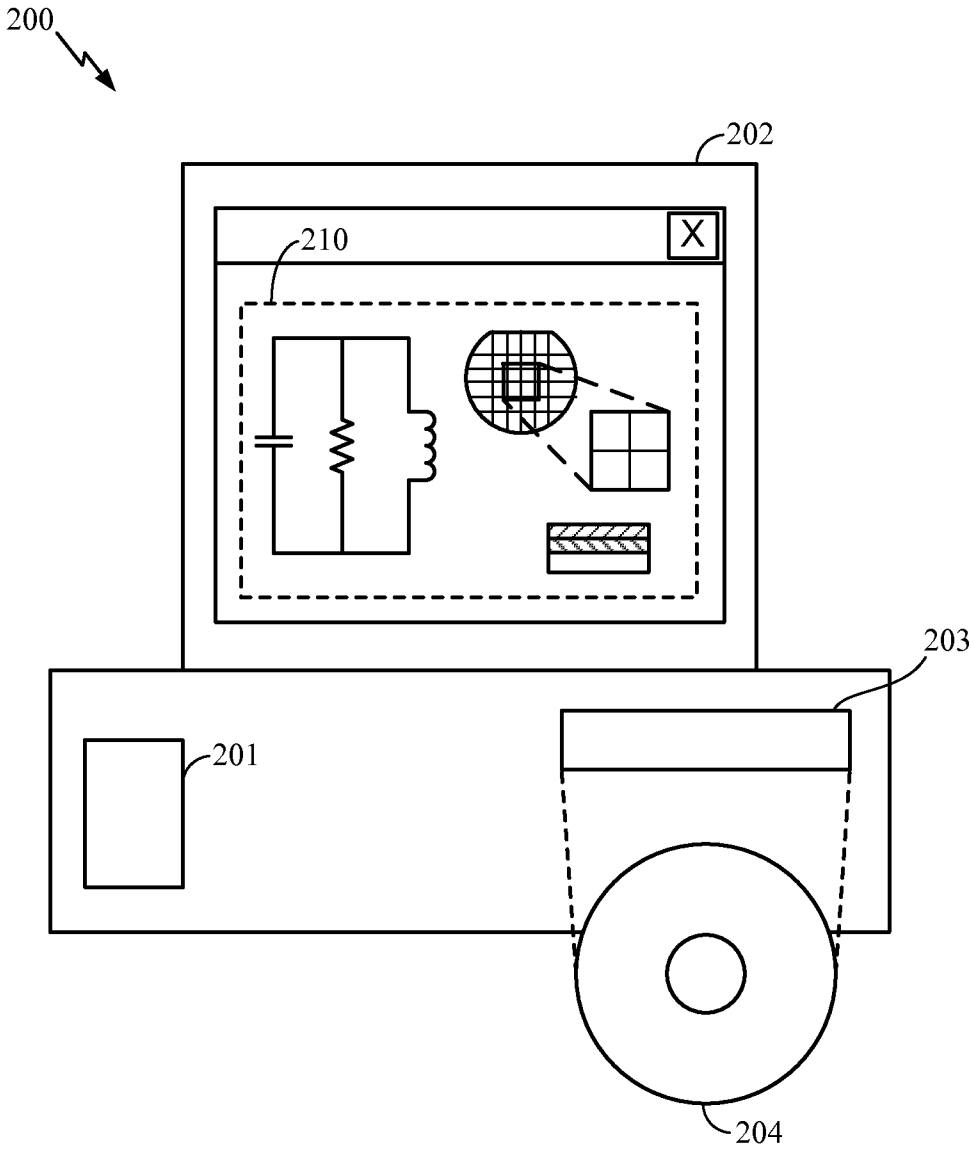

FIG. 2

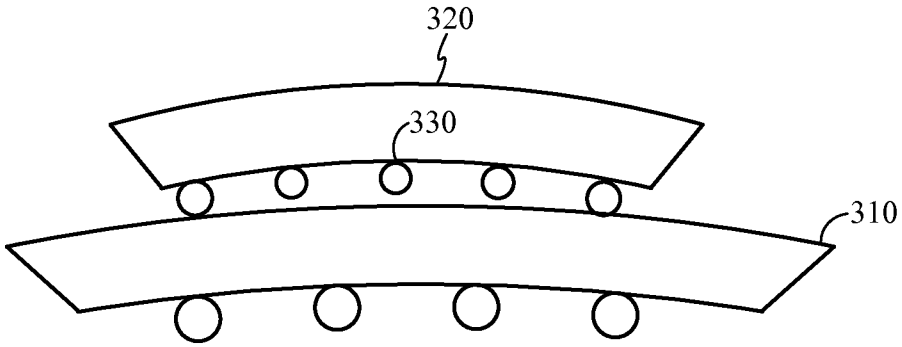

FIG. 3

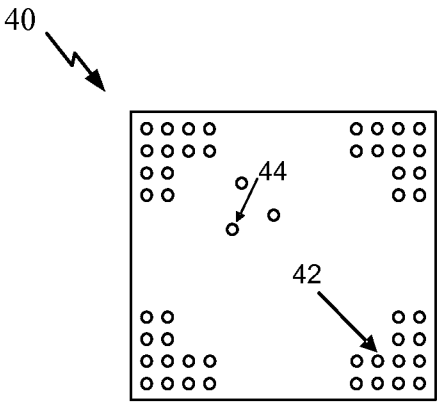

FIG. 4

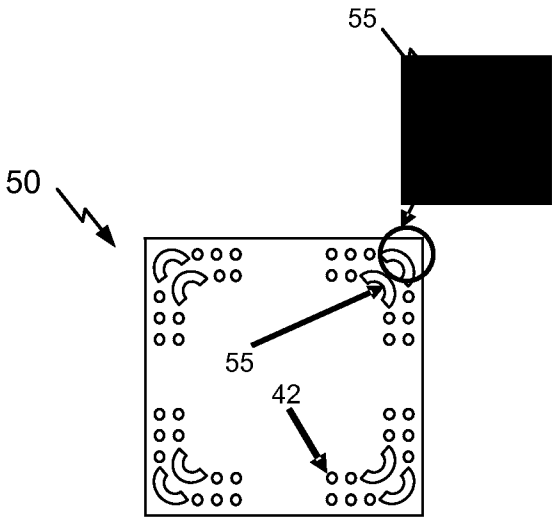

FIG. 5