United States Patent

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[33] **Germany**
[31] **P 17 66 415.2**

[54] **FREQUENCY DISCRIMINATOR TO ELIMINATE THE EFFECT OF NOISE PULSE WIDTH MODULATIONS**
3 Claims, 10 Drawing Figs.

[52] **U.S. Cl.** **329/103,** 307/234, 307/241, 307/280, 329/136
[51] **Int. Cl.** **H03d 3/00**
[50] **Field of Search** 329/101, 103, 107, 145, 136, 110; 307/280, 300, 238, 233, 244, 242, 234

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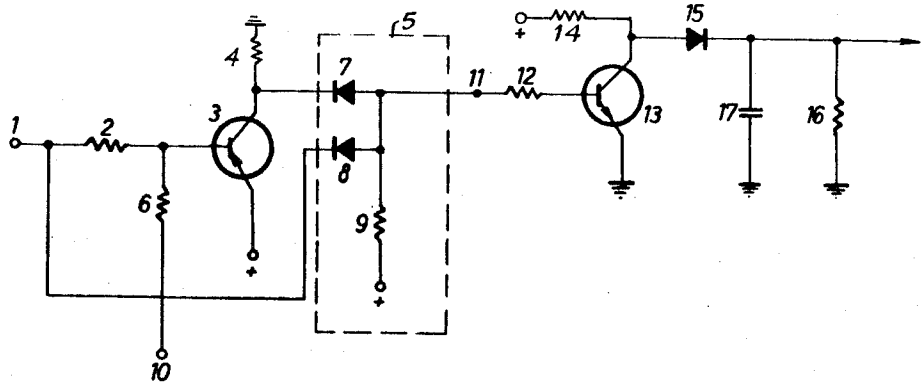
Attorneys—C. Cornell Remsen, Jr., Walter J. Baum, Paul W. Hemminger, Percy P Lantzy, Philip M. Bolton, Isidore Togut and Charles L. Johnson, Jr.

ABSTRACT: To eliminate the effects of noise width modulations, the input FM pulse signals are applied to a PNP transistor the duration of whose output pulses is each extended for a period equal to the "turnoff" time. These extended pulses are combined in an AND gate with the input pulse signals leaving pulses of a constant width equal to the "-turnoff" time. The latter pulses are applied to an NPN transistor whose "turnoff" time (storage time + fall time) after each pulse is such that the leading edge of the next pulse coincides with some point on the current fall time (voltage rise time) in the NPN-transistor which point varies with the pulse frequency. Frequency centering of the discriminator is accomplished by feeding back the integrated output voltage to the base of the second-mentioned transistor to control its "turnoff" time.



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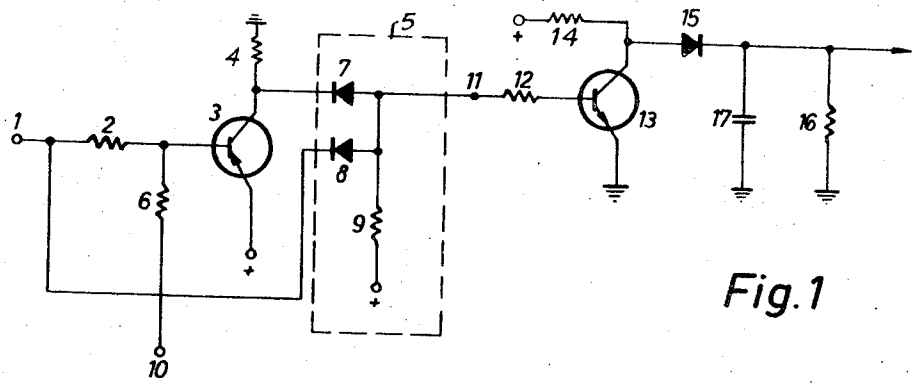

Fig.1

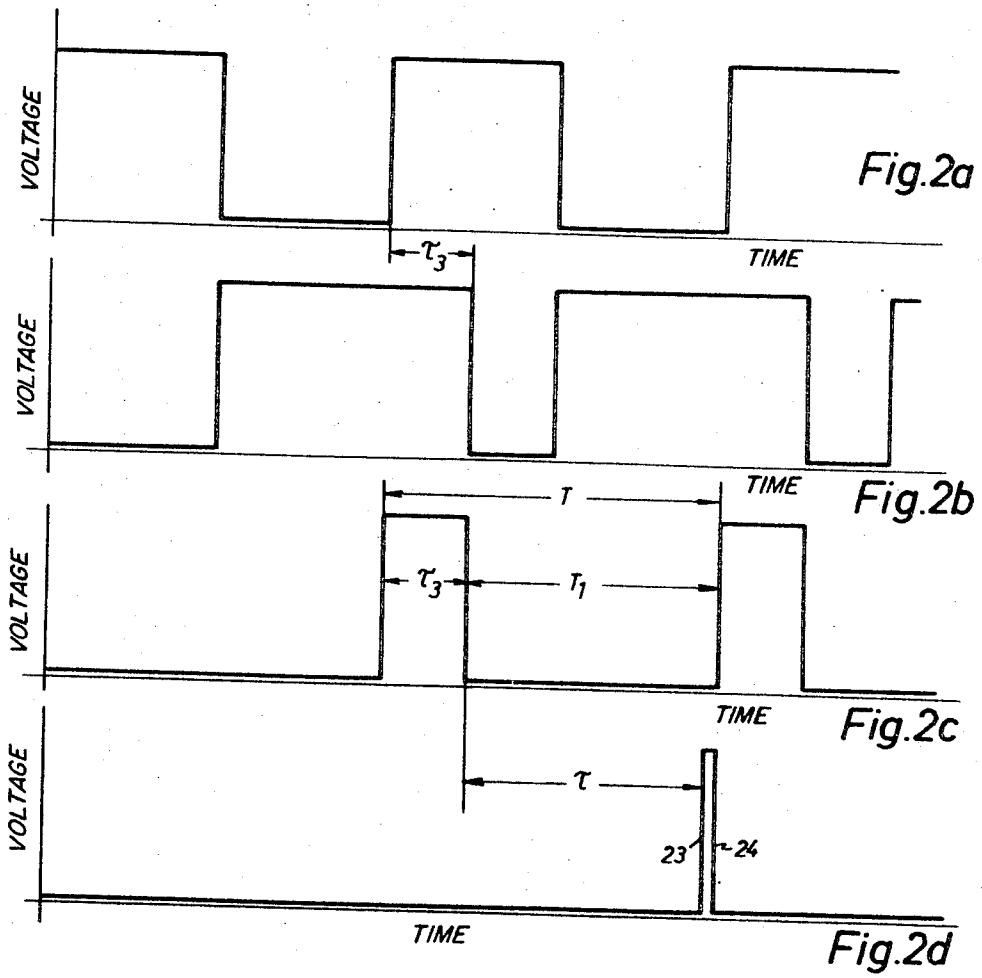

Fig.2a

Fig.2b

Fig.2c

Fig.2d

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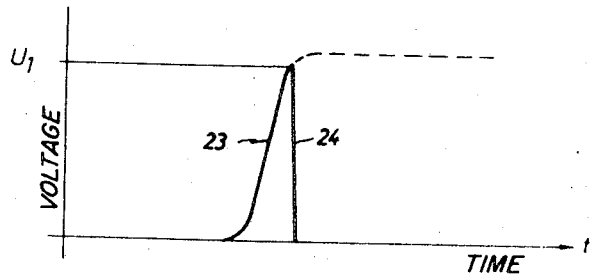

Fig.3a

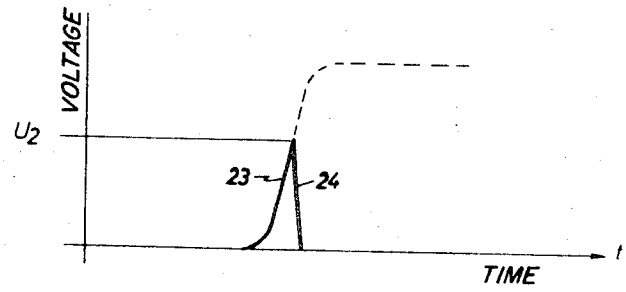

Fig.3b

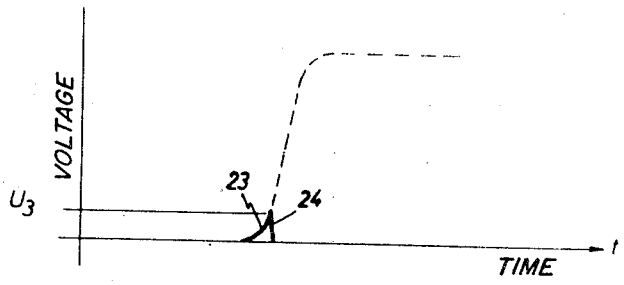

Fig.3c

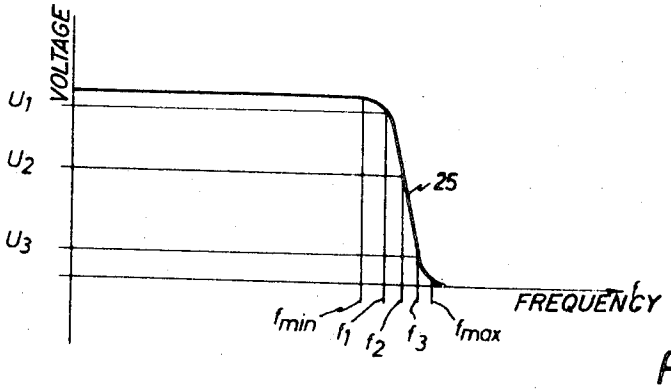

Fig.4

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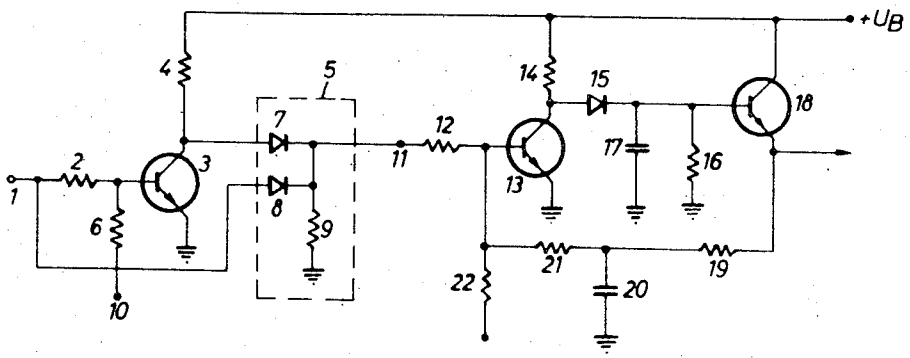

Fig. 5

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FREQUENCY DISCRIMINATOR TO ELIMINATE THE EFFECT OF NOISE PULSE WIDTH MODULATIONS

This invention relates to a frequency discriminator for pulse-shaped signals which is unresponsive to pulse width modulation.

My copending U. S. Application, Ser. No. 714,498, filed Mar. 20, 1968, now Pat. No. 3,519,943 for "Frequency Discriminator for Pulse-Shaped Signals," describes a frequency discriminator for pulse-shaped signals having a high steepness of edges of the discriminator characteristic lying between the frequency f_{min} and the frequency f_{max}, in which the pulse-shaped signals are fed to a semiconductor element (transistor or diode) whose storage time τ is approximately as long as the time spacing of the pulses at the frequency f_{max}. The pulses as produced by the semiconductor element are rectified, and the rectified voltage serves as the discriminator output voltage.

The frequency discriminator according to said copending application is particularly suitable for effecting the demodulation of pulse shaped, frequency-modulated signals in which, however, there does not appear a noise modulation of the pulse duration.

In some receivers a sinusoidal fm signal is clipped to convert it into pulse-shaped signals. Whenever there appears an unwarranted amplitude of the sine wave of sinusoidal signals it will appear in most cases, during the clipping, that the amplitude noise modulation is converted into a noise pulse width modulation of clipped pulses.

An object of the present invention is to provide a discriminator of the type mentioned in said copending application in which noise pulse width modulation appearing in addition to the frequency modulation is not demodulated.

In accordance with the present invention this is accomplished by providing a frequency discriminator comprising a source of input pulse signals, a semiconductor coupled to said source having a given delay in changing between its saturated and nonconductive states in response to input pulses, to thereby produce extended pulse signals, a first means coupled to said source and to the output of said semiconductor for producing output pulse signals each having a constant width equal to said given delay, and a second means responsive to the frequency of said constant width output pulse signals for producing an output that changes in amplitude with variations in said frequency.

Other and further objects of the present invention will become apparent from the following description of embodiments thereof, reference being had to the drawings, in which:

FIG. 1 is a schematic diagram of a frequency discriminator embodying the present invention;

FIGS. 2, 3, and 4 are waveforms and curves used in explaining the present invention; and

FIG. 5 is a schematic diagram of a modified embodiment of the present invention.

In FIG. 1 reference number 1 indicates the input terminal to which there are fed the frequency-modulated pulse-shaped signals which, at the same time, have a noise pulse width modulation, and which are supposed to be subjected to a frequency demodulation. From the terminal 1 this pulse-shaped signal, via coupling resistor 2 is applied to the base of the PNP-transistor 3 with the turnoff time τ_3. The reference numeral 4 indicates the collector resistor of this transistor. Both the input voltage as well as the output voltage as applied to the collector, are fed to an AND-circuit 5, which, in the present example, consists of the two diodes 7, 8 and of the resistor 9. By the auxiliary voltage which, in connection with the terminal 10, is applied to the resistor 6, and with this auxiliary voltage being connected to the base via the resistor 2, there is storage time and with the storage time the turnoff time τ_3 of the transistor 3.

The circuit consisting of the elements 1 to 11 serves to completely suppress the noise pulse width modulation by pulse width limitation. Accordingly, at the output 11 there will appear a pulse signal whose frequency is modulated, but whose pulse width τ_3 is constant; accordingly it is free from the original noise pulse width modulation. Following the terminal 11 is the discriminator according to said copending application. In this connection the reference numeral 12 indicates the coupling resistor to the base of transistor 13 (first semiconductor element).

The reference number 14 indicates the collector resistor of this transistor 13 whose storage time is τ. The reference numeral 15 indicates a rectifier diode; 16 and 17 indicate an RC-circuit with the aid of which, and in connection with the diode 15, there is achieved peak rectification. The demodulated modulation signal may be taken off at the RC-circuit 16, 17. Instead of using differently doped semiconductor elements, it is also possible to use semiconductors which are doped in the same way, provided that between the semiconductor element 3 and the semiconductor element 13, e.g. within the AND-circuit 5, and by using a transistor, there is effected a polarity reversal, with the turnoff time thereof being taken into consideration accordingly.

In explaining the mode of operation of the circuit according to FIG. 1, reference is made to FIGS. 2*a* to 2*d*. In FIG. 2*a* there are shown some periods of the pulse voltage as applied to the terminal 1. FIG. 2*b* shows the pulse voltage as generated at the collector of transistor 3. In this case τ_3 is the turnoff time of this particular transistor. FIG. 2*c* shows the output voltage of the AND-circuit 5 as appearing at the terminal 11 with the pulse duration (width) τ_3. In the case of variations of the pulse width of the input signal (FIG. 2*a*) the pulse width τ_3 of this particular signal no longer will vary. In cases where the frequency of the input signal varies, the pulse intervals T_1 will vary in the same sense as the frequency modulation. FIG. 2*d* shows the pulse voltage as appearing at the collector of transistor 13. In this case τ indicates the storage time of this particular transistor. In this drawing the pulses are shown in idealized fashion.

In FIG. 2*d* there is shown the voltage at the collector of transistor 13 with respect to a frequency which is smaller than f_{min}. Relative thereto, and in an idealized fashion, there is shown the edge steepness of the delayed disconnecting edge 23 and of the connecting edge 24. In the case of the frequency f_{max} the duration of period $T_{min}=1/f_{max}$ is so short that the pulses of FIG. 2*d* just disappear. In this particular case $T=T_{min}=\tau_3+\tau$. In FIGS. 3*a* to 3*c* the pulses appearing at the collector of transistor 13 are represented in a considerably expanded fashion and having the edge steepnesses as actually appearing. In this respect the edge 23, analogously to the edge 23 in FIG. 2*d*, corresponding by the current fall-time as transistor 13 is being turned off is the delayed leading edge. The reference numeral 24 indicates the trailing edge (switch-on edge) corresponding to the current rise-time as transistor 13 is being turned on. In FIG. 4 there is shown the discriminator curve as associated with the FIGS. 3*a* to 3*c*. FIG. 3*a* shows the pulses as appearing at the collector of transistor 13 at the frequency f_1 lying very close to the frequency f_{min} (see FIG. 4). By rectification of these pulses as shown in FIG. 3*a*, there will result DC voltage U_1. In the case of the higher frequency f_2 the distance between the delayed leading or switch-off edge 23 and the following trailing or switch-on edge 24 still becomes smaller, so that in accordance with FIG. 3*b*, and at the frequency f_2 there will result a voltage U_2. FIG. 3*c*, finally, shows the pulse waveform with respect to the frequency f_3, in which there results the DC voltage U_3. As may be recognized from the showing of FIGS. 3*a*, 3*b*, 3*c* and from FIG. 4, the form of the discriminator edge 25 which is a function of the frequency, is identical to the leading or switch-off edge 23 which is a function of time. The storage time τ is so large that it, with respect to the predetermined frequency f_{max} is equal to the time spacing of the pulses at the frequency f_{max}. In this case the beginning of the delayed leading edge 23 coincides with the beginning of the trailing edge 24, so that the output voltage of the discriminator will equal zero. The steepness of the delayed edge is so great that in the case of the predetermined frequency f_{min}, there is achieved the full amplitude of the delayed pul-

ses. With respect to the frequency f_{min} the trailing edge **24** only commences after the blocking delay edge **23** has reached its maximum possible value.

The slope of the delayed leading edge may be varied with the aid of means as known per se. A reduction of the slope or inclination is possible e.g. by increasing the capacitance between the collector potential of transistor **13** and mass (ground). A reduction of the slope can also be achieved e.g. by reducing the collector resistance **14**. Finally, and in the likewise known manner, it is possible to achieve extremely high edge steepnesses, by providing between the collector of transistor **13** and the rectifier **15** a further amplifying stage which increases the steepness of the leading edge.

In FIG. **5** there is shown a further example in which there is used a feedback towards the automatic tuning of the discriminator as already explained in said copending application. Identical parts are indicated by the same reference numerals as in FIG. **1**. Also the mode of operation of the elements **1** to **17** is the same. Reference numeral **18** indicates an emitter follower whose base is connected to the RC-circuit **16**, **17**, and whose collector is applied to the general supply voltage. At the emitter there is provided the demodulated signal. At the capacitor **20** the mean value of the demodulated modulation signal is generated. This mean value, via the resistor **21**, is fed to the base of transistor **13**. To achieve the desired operating point, a fixed biasing potential is applied, via the resistor **22**, likewise to the base of transistor **13**. If, for example owing to temperature variations, the storage time τ varies towards higher values, then the mean value of the output voltage of the discriminator will drop in the negative direction, and on account of this the filtered control voltage at the capacitor **20** will drop in the negative direction and, consequently, finally also the base biasing potential of transistor **13**. In this way the storage time τ is controlled back. In the case of variations of the center frequency of the input signal the discriminator will thus be automatically adjusted in such a way that the discriminator edge will lie at the frequency of the input signal. In a trial circuit the discriminator automatically followed the center frequency within a frequency variation range of about 1:10.

In special cases, in which a flat course of the discriminator characteristic is either desired or admissible, a linearization of the characteristic can be achieved in that a certain portion of the demodulated low frequency voltage is used and supplied to the base of transistor **13** for the purpose of controlling the storage time. This may be effected, for example, in that in the circuit of FIG. **5**, and in series with the capacitor **20**, there is arranged a resistor. In an advantageous manner, the low frequency voltage may be taken off the output of a subsequently following *lf* (low frequency) amplifier so that, in addition thereto, also this *lf*-amplifier is linearized, thus also reducing the distortion factor.

I claim:

1. A frequency discriminator comprising:

a source of input pulse signals;

a first transistor coupled to said source having a given delay in changing between its saturated and nonconductive states in response to input pulses, to thereby produce delayed pulse signals;

an AND gate coupled to said source and to the output of said first transistor for producing output pulse signals each having a constant width equal to said given delay; and

means responsive to the frequency of said constant width output pulse signals for producing an output that changes in amplitude with variations in said frequency, said means includes a second transistor also having a given delay in changes between its saturated and nonconductive states, the given delay of said second transistor being such that the application of a leading edge of each pulse to the second transistor occurs during the fall-time of the collector current of said first transistor and at a point during said current fall which varies with the frequency of said pulse signals.

2. A frequency discriminator according to claim **1**, wherein said transistors are of opposite conductivity type.

3. A frequency discriminator according to claim **1**, further including means coupled to the output of said second transistor for producing an output voltage; and

means for feeding back at least a portion of said output voltage to said second transistor to vary said given delay thereof and to thereby control the center frequency of its discriminating curve.