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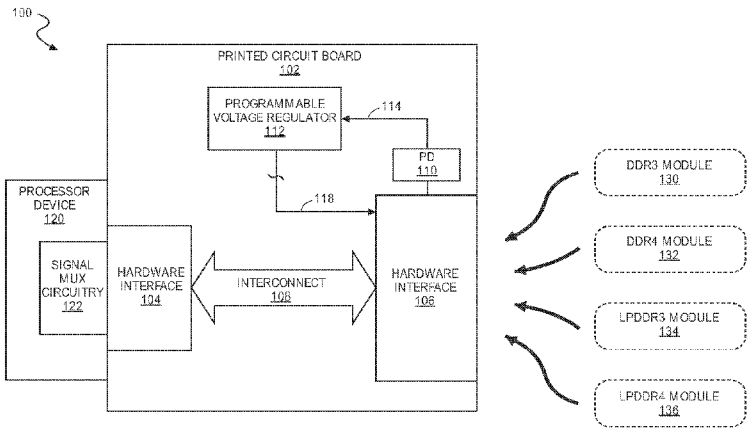

FIG. 1

(57) **Abstract**: Techniques and mechanisms to exchange communications via a printed circuit board (PCB) between a processor device and a memory device. In an embodiment, the processor device is configured based on a memory type of the memory device to an interface mode of multiple interface modes each corresponding to a different respective one of multiple memory standards. A voltage regulator (VR) is programmed, based on the memory type, to a VR mode to provide one or more voltages to the memory device via a hardware interface on the PCB. In another embodiment, x signal lines of an interconnect disposed in or on the PCB are each coupled between the processor device and the memory device to one another. The value x is an integer equal to a total number of signals of a superset of sets of signals each specified by a different respective one of the multiple memory standards.

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APPARATUS, SYSTEM AND METHOD TO PROVIDE PLATFORM SUPPORT FOR MULTIPLE MEMORY TECHNOLOGIES

RELATED APPLICATIONS

This application is a nonprovisional application based on U.S. Provisional Patent Application No. 61/941,687 filed February 19, 2014, and claims the benefit of priority of that provisional application. Provisional Application No. 61/941,687 is hereby incorporated by reference.

BACKGROUND

1. Technical Field

Embodiments discussed herein variously relate to computer platform design. More particularly, certain embodiments include, but are not limited to, a platform to accommodate any of multiple different memory technologies.

2. Background Art

Improvements to memory systems have taken, and continue to take, many forms including faster dynamic random access memory (DRAM), higher double data rate (DDR) bus frequencies, larger capacity dual inline memory modules (DIMMs), more DIMMs per channel and other increased capabilities. DDR standards defined by the Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association are some examples of memory technologies that variously implement memory functionality, and do so with different respective memory interface hardware.

Due to industry requirements regarding support for legacy memory systems, there is an increasing variety of memory interface hardware in the market as successive generations of memory device technologies are developed. To date, platform developers have relied upon the design of different printed circuit boards to support integration of different memory technologies each into a corresponding platform type.

Memory device testing and platform assembly are two areas of the industry that are impacted by the variety of previous, current and upcoming memory technologies to be tested

and/or marketed. One common problem faced in these areas is the limited applicability of a given printed circuit board design to support only one corresponding memory technology.

BRIEF DESCRIPTION OF THE DRAWINGS

The various embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which:

FIG. 1 is a high-level block diagram illustrating elements of a system to support any of multiple memory technologies according to an embodiment.

FIG. 2 illustrates elements of a system to support any of multiple memory technologies according to an embodiment.

FIG. 3 is a flow diagram illustrating elements of a method to access a memory device according to an embodiment.

FIG. 4 is a flow diagram illustrating elements of a method to configure a platform to accommodate a memory technology according to an embodiment.

FIG. 5 is a set of tables each describing signals of a corresponding memory technology supported by a platform according to a respective embodiment.

FIG. 6 is a set of tables variously listing signal types and voltages each specified by a respective memory technology supported by a platform according to an embodiment.

FIGs. 7A-7C is a set of tables each describing a mapping of signals across different interface modes of a platform according to an embodiment.

FIGs. 8A-8D is a set of tables each illustrating elements of a pinout for accommodating a respective memory technology according to a corresponding embodiment.

FIGs. 9A-9C is a set of tables each illustrating elements of a pinout for accommodating a respective memory technology according to a corresponding embodiment.

FIG. 10 is a high-level block diagram illustrating elements of a computer system to support any of multiple memory technologies according to an embodiment.

FIG. 11 is a high-level block diagram illustrating elements of a mobile device to support any of multiple memory technologies according to an embodiment.

DETAILED DESCRIPTION

Embodiments discussed herein variously provide techniques and/or mechanisms for a platform to support operation with a memory device that is based on any of multiple different memory technologies. In an embodiment, a printed circuit board (PCB) such as a motherboard has disposed therein and/or thereon circuitry to exchange one or more signals indicating connectivity of the PCB to a memory device via a hardware interface that is disposed in or on the PCB. Such circuitry may be configured to exchange one or more signals identifying a memory type of the memory device. In some embodiments, a voltage regulator (VR) is coupled to the PCB, wherein multiple programmable modes of the VR each correspond to a different respective one of the multiple memory technologies. Based on a memory type of the memory device – e.g., a particular memory technology on which the memory device is based – a mode of the VR may be programmed to provide to the hardware interface one or more voltages specified by the corresponding memory technology. The memory device may exchange signals with a processor device coupled to the PCB via another hardware interface disposed in or on the PCB. The interconnect may include signal lines configured to be able to accommodate any of multiple interface modes of the processor device – e.g., where the multiple interface modes each correspond to a different respective one of the multiple memory technologies.

As used herein, "hardware interface" refers to a set of input and/or output (I/O) contacts – such as pins, pads, balls or other conductive structures – by which one device may be coupled to another device. For example, a hardware interface may be disposed on a PCB to allow for coupling of a packaged integrated circuit (IC) device, a memory module and/or other device to the PCB. A hardware interface may include, for example, a mechanical connector capable of receiving a pluggable memory module. Alternatively, a hardware interface may include an array of pads available to be soldered to a ball grid array (BGA) of a device. A device to couple to a PCB via a hardware interface may comprise a processor (e.g., a central processing unit) including one or more processor cores. Alternatively, such a device may comprise a DIMM or other memory module including one or more packaged memory devices.

Certain illustrative embodiments are discussed herein with respect to various memory standards such as dual data rate (DDR) standards. Examples of such standards include, but are not limited to, the DDR3 Synchronous Dynamic Random-Access Memory (SDRAM) standard JESD79-3, published June 2007 by the JEDEC Solid State Technology Association, the DDR3L SDRAM standard JESD79-3-1, published July 26, 2010 by the JEDEC Solid State Technology Association and the DDR4 SDRAM standard JESD79-4, published September 25, 2012 by the

JEDEC Solid State Technology Association. Other examples include the LPDDR3 JESD209-3 LPDDR3 Low Power Memory Device Standard, published May 17, 2012 by the JEDEC Solid State Technology Association, the LPDDR4 Low Power Memory Device Standard JESD209-4, published August 2014 by the JEDEC Solid State Technology Association and the Graphics Double Data Rate (GDDR5) Synchronous Graphics Random-Access Memory (SGRAM) Standard JESD212B.01, published December 2013 by the JEDEC Solid State Technology Association. However, such discussion may be extended to additionally or alternatively apply to any of a variety of DDR and/or other memory standards. Unless otherwise indicated, "memory technology" and "memory type" are variously used herein to refer to particular set of signals and/or one or more voltages that are included in or otherwise used by a memory device. Such a set of signals and one or more voltages may be based on – e.g. specified by or otherwise compatible with – requirements of a particular memory standard, for example.

Certain embodiments discussed herein variously relate to a platform supporting operation of a processor device that is configurable to support multiple different modes each corresponding to a different respective memory technology. Such modes may each include a different respective pinout being configured for the processor device. Unless otherwise indicated, "interface mode" herein refers to a mode of a device – e.g., a processor device – that provides a particular pinout of the device. One interface mode of a device may be distinguished from one or more other interface modes of the device that each provide a different respective pinout of the device. At different times, a processor device may operate in different ones of the multiple interface modes – e.g., while the processor remains coupled to a PCB via the same hardware interface. A transition of a device to an interface mode – e.g., including a transition between different interface modes – is referred to herein as multiplexing (or MUXing) to the interface mode.

FIG. 1 illustrates elements of a system 100 according to an embodiment to facilitate operation of a processor with any of multiple memory devices each corresponding to a different respective set of signal – e.g., the sets of signals each based on a different respective memory standard. The technologies described herein may be implemented in one or more electronic devices. Non-limiting examples of electronic devices that may utilize the technologies described herein include any kind of mobile device and/or stationary device, such as cameras, cell phones, computer terminals, desktop computers, electronic readers, facsimile machines, kiosks, netbook computers, notebook computers, internet devices, payment terminals, personal digital assistants, media players and/or recorders, servers (e.g., blade server, rack mount server, combinations

thereof, etc.), set-top boxes, smart phones, tablet personal computers, ultra-mobile personal computers, wired telephones, combinations thereof, and the like. Such devices may be portable or stationary. In some embodiments the technologies described herein may be employed in a desktop computer, laptop computer, smart phone, tablet computer, netbook computer, notebook computer, personal digital assistant, server, combinations thereof, and the like. More generally, the technologies described herein may be employed in any electronic device to which one or both of a processor device and memory device may be coupled and/or installed.

In an embodiment, system 100 includes printed circuit board (PCB) 102 and components variously disposed therein or thereon, where such components are to facilitate communication between a processor device 120 and a memory device that are each to couple to PCB 102. Such components are represented as including the illustrative hardware (HW) interface 104, HW interface 106, interconnect 108, presence detector PD 110 and programmable voltage regulator (VR) 112. However, system 100 may include any of a variety of additional or alternative components to provide functionality such as that described herein. System 100 is shown as including PCB 102 coupled to processor device 120 via HW interface 104, where PCB 102 is available to be further coupled to any of multiple different memory devices via HW interface 106. However, some embodiments of system 100 merely include PCB 102 and components disposed therein and/or thereon – i.e., where the embodiment is available to be coupled to, but does not include, processor device 120. Examples of the different memory devices include memory modules each based on – e.g., conforming to or at least compatible in one or more respects with requirements of – a different respective memory standard such as the illustrative DDR3 module 130, DDR4 module 132, LPDDR3 module 134 and LPDDR4 module 136. However, system 100 may support fewer, more and/or different memory technologies, according to different embodiments.

Processor device may include one or more processor cores and, in an embodiment, memory controller logic to access a memory device on behalf of such one or more processor cores. Processor device 120 is one example of a pinout-configurable device – e.g., where processor device 120 includes signal MUX circuitry 122 to provide any of multiple different possible pinouts at the connection to HW interface 104. As used herein, "pinout" refers to a mapping of I/O contacts (e.g., pins, pads, balls or the like) each to a respective signal or voltage of an interface. Signal MUX circuitry 122 may be configured at different times to any of different interface modes each corresponding to a different respective memory technology, where an interface mode provides a respective pinout to accommodate the corresponding

memory technology. Some or all of signal MUX circuitry 122 may be adapted from conventional mechanisms to provide a configurable pinout. The particular details of such conventional mechanisms, which are not limiting on certain embodiments, are not detailed herein to avoid obscuring features of such embodiments.

To date, platform designers have relied upon one PCB design (or one class of PCB designs) for a given pinout-configurable processor device to operate with one memory technology, and a different PCB design (or class of PCB designs) for that pinout-configurable processor device to operate with a memory device of a different memory technology. Certain embodiments are a result of a realization that PCB design may be adapted to build on the capabilities of a pinout-configurable processor device, allowing for the device's operation – as part of one common platform – with any of multiple different possible memory technologies.

In an embodiment, printed circuit board 102 is to serve as a motherboard for a platform – e.g., where system 100 is the platform or a component of the platform. Hardware interfaces 104,106 may each include a respective plurality of I/O contacts – e.g., where interconnect 108 includes signal lines each coupling a respective I/O contact of HW interface 104 to a respective I/O contact of HW interface 106. By way of illustration and not limitation, such signal lines of interconnect 108 may variously support the communication of data signals, address signals, clock signals, on-die termination signals, clock enable signals, chip select signals and/or any of various other signals variously defined each by a respective memory standard.

Processor device 120 may comprise a packaged device including one or more processor cores to operate as a central processing unit (CPU) or other processor for system 100 – e.g., including processor device 120 executing a host operating system (OS), a Basic Input/Output System (BIOS) and/or one or more other software processes. Although certain embodiments are not limited in this regard, processor device 120 may include or otherwise have access to state machine logic (e.g., comprising hardware, firmware and/or executing software) to identify a particular memory technology type of a memory device coupled to HW interface 106. In some embodiments, system 100 is to couple to, but may not include, either or both of processor device 120 and a memory device to couple to HW interface 106.

System 100 may include presence detector circuitry PD 110 disposed in or on PCB 102, where circuitry of PD 110 is to detect connectivity of a memory device to HW interface 106. Such a memory device may include a memory module – e.g., a DIMM – comprising one or more packaged memory devices based on a particular memory standard. Although certain

embodiments are not limited in this regard, detection of such connectivity may include PD 110 performing one or more operations adapted from conventional presence detection techniques such as those based on a serial presence detect (SPD) standard. One example of such a standard is the SPD standard for DDR3 SDRAM Modules (Release 6), SPD4_01_02_11: SPD Annex K, of the JEDEC Solid State Technology Association, published February, 2014. The particulars of such conventional presence detect techniques are not detailed herein, and are not limiting on certain embodiments.

PD 110 may generate a signal 114 indicating the detected connectivity of a memory device to PCB 102 via HW interface 106. Signal 114 may specify a particular memory type of the memory device or, alternatively, may merely signal connectivity generically. Signal 114 may cause one or more other components of system 100 to determine and/or operate based on a specific one of multiple possible memory types of the memory device.

For example, a programmable voltage regulator (VR) 112 disposed in or on PCB 102 may be programmable to provide to HW interface 106 any of multiple sets of one or more signals that each correspond to a different respective memory technology. Based on signal 114, programmable VR 112 may be programmed to provide a particular set of one or more voltages – as represented by the illustrative one or more voltages 118 – that correspond to the memory type (in this case, memory technology) of the memory device coupled to HW interface 106. The one or more voltages 118 may be variously provided directly or indirectly by VR 112 each to a respective I/O contact of hardware interface 106 – e.g., where such I/O contacts are to be distinguished, for example, from I/O contacts of HW interface 106 that are coupled to interconnect 108. In another embodiment, the one or more voltages 118 may be provided by VR 112 to HW interface 106 via processor 120 and interconnect 108 and/or one or more other intermediary components of system 100. One or more voltages 118 may include, but are not limited to, a reference (e.g., ground) voltage, a supply (e.g., VDD) voltage and/or any of various other voltages.

Signal 114 is shown as being provided directly to programmable VR 112. However, in an alternate embodiment, signal 114 may be additionally or alternatively provided to other logic of 100 that is to identify a memory technology of the memory device coupled to HW interface 106. For example, signal 114 may instead be communicated to state machine logic of processor device 120, where in response to signal 114, such state machine logic may identify a memory type of the memory device. In turn, such state machine logic may communicate the memory

type to facilitate configuration of a corresponding interface mode of signal MUX circuitry 122 and/or to facilitate programming of programmable VR 112.

Referring now to FIG. 2, an assembly view of a system 200 according to one illustrative embodiment is shown. System 200 may include some or all of the features of system 100, for example. In an embodiment, system 200 includes a PCB 202 and components variously disposed therein or thereon to facilitate communication between a processor device 220 and a memory device 22 that are each to couple to PCB 202. Such components are represented as including the illustrative HW interfaces 204, 206, interconnect 208, detector 210 and VR 212.

In FIG. 2, PCB 202 is shown as being ready to be coupled to processor device 220 via HW interface 204, and further ready to be coupled to memory device 222 via HW interface 206. Some embodiments of system 200 merely include PCB 202 and components disposed therein and/or thereon – i.e., where the embodiment is available to be coupled to, but does not include, processor device 220 or memory device 222.

In the illustrative embodiment of system 200, HW interface 204 is an array of I/O pads to be variously soldered each to a corresponding ball of a ball grid array of processor device 220. By contrast, HW interface 206 may be a mechanical connector including I/O contacts to plug or otherwise connect with respective I/O contacts of memory device 222. By way of illustration and not limitation, HW interface 206 may comprise a memory module connector such as one that is compatible with a small outline DIMM (SO-DIMM) connector or any of various other conventional memory module connector types. HW interface 206 may facilitate a user switching or otherwise choosing between memory device 222 and at least one alternative memory device – e.g., where the two memory devices are based on different memory standards.

PCB 202 may facilitate communication by processor device 220 and memory device 222 as well as, at another time, an alternative memory device (not shown) that may be coupled to PCB 202 via HW interface 206. Interconnect 208 may include a plurality of signal lines each coupling an I/O contact of HW interface 204 to a respective I/O contact of HW interface 206. A total number of such a plurality of signal lines may correspond to a superset of multiple sets of signal lines variously defined each by a respective memory standard. By way of illustration and not limitation, the multiple sets of signal lines may include a first set including signals defined by a first memory standard and a second set including signals defined by a second memory standard. In such an embodiment, the plurality of signal lines of interconnect 208 may correspond to a superset due at least in part to the total number of the plurality of signal lines

being greater than a total number of first set, and less than a total number of signals of the first set and the second set.

As discussed herein, detector 210 may detect connectivity of memory device 222 to HW interface 206 and exchange via PCB 202 a signal indicating such connectivity. An indication of such connectivity may be communicated directly or indirectly to one or more components – e.g., including HW interface 204 and/or VR 212 – that are to determine a memory type of memory device 222 and/or be configured based on such a memory type. For example, processor device 220 may determine the memory type and configure a particular interface mode, of multiple possible interface modes of processor device 220, for an exchange of signals via HW interface 204 that is compatible with the memory type. The multiple possible interface modes of processor device 220 may each correspond to a different respective memory technology, where each interface mode is to provide a different respective pinout to accommodate the corresponding memory technology. Alternatively or in addition, VR 212 may configure a particular VR mode, of multiple possible VR modes of VR 212, for the providing of one or more voltages to memory device 222 via HW interface 204. The multiple possible VR modes may each correspond to a different respective memory device type, where each VR mode is to provide respective one or more voltages specified by the corresponding memory technology.

FIG. 3 illustrates elements of a method 300 for exchanging communications between a processor and a memory device according to an embodiment. Method 300 may be performed by a platform, system or other hardware including some or all of the features of system 100, for example. In an embodiment, method 300 includes, at 310, detecting connectivity of a memory device to a first hardware interface disposed in or on a printed circuit board. The detecting at 310 may be performed with detector logic disposed in or on the PCB, wherein the detector logic generates and send to a processor device a signal indicating the connectivity. Such detector logic may conform to or otherwise be based on a serial presence detect standard, for example.

In response to detecting at 310, method 300 may include, at 320, identifying a memory type of the memory device. The identifying at 320 may include identifying a memory standard on which the memory device is based and/or identifying a set of signals (e.g., a pinout) included in or otherwise corresponding to the memory device. Based on the memory type, a processor device may configure a first interface mode of multiple interface modes of the processor device. For example, the processor may be coupled to the PCB via a second hardware interface disposed in or on the PCB. State machine logic included in or otherwise accessible to the processor device may identify the memory type of the memory device, from among multiple possible

memory types, based on one or more exchanges with detector logic on the PCB and/or with the memory device itself. Such state machine logic may comprise, for example, state machine circuitry of the processor device or a Basic Input/Output System (BIOS) process executed by the processor device. The multiple interface modes of the processor device may each correspond to a different respective one of multiple sets of signals. Such sets of signals may include one or more sets each specified by a different respective memory standard.

Method 300 may further comprise, at 330, providing one or more voltages to the first interface based on the identified memory type. For example, the VR may generate or receive an indication of the memory type and, in response, program a first voltage regulator (VR) mode of multiple VR modes of a VR. The multiple VR modes may each correspond to a different respective one of multiple memory device types. The multiple memory types may each correspond to a respective memory standard – e.g., where one or more VR modes are each to provide respective one or more voltages specified by a corresponding memory standard. The VR may provide the one or more voltages at 330 based on the programmed first VR mode.

During operation of the memory device based on the one or more voltages, method 300 may, at 340, exchange signals between the memory device and the processor device. For example, such signals may be exchanged via x signal lines of an interconnect disposed in or on the PCB, wherein x is an integer equal to a total number of signals of a superset of sets of signals each corresponding to a different respective one of multiple memory types.

FIG. 4 illustrates elements of a method 400 for identifying a memory type of a memory device according to an embodiment. Method 400 may be performed by a component of system 100 or 200 to determine a pinout to be configured for communication with the memory device. For example, method 400 may be performed by a BIOS process of processor device 120 or processor device 200.

At 402, method 400 may begin operations to power on a system such as one of systems 100, 200. During or after such power on operations, one or more main rails of a PCB may be powered on – e.g., to power detector logic that is to detect connectivity of a memory device via a HW interface disposed in or on the PCB. By way of illustration and not limitation, at 406, serial presence detect (SPD) logic on the PCB may be polled by state machine logic to determine a memory type of any memory device coupled to the HW interface. After the polling at 406 indicates the presence of a memory device is detected, method 400 may determine, at 408, whether a processor coupled to the PCB supports a memory type of the memory device.

Where the memory type is not supported, method 400 may include an error message being generated, such as the illustrative BIOS power on, self-test (POST) code issued at 410, and a system boot failure at 412. However, where it is determined at 408 that the determined memory type is supported, method 400 may, at 414, program voltage regulator rails to provide respective voltage levels specified by a memory standard corresponding to the memory type. The voltage levels may be variously provided from the voltage regulator, via the PCB and the HW interface, to the memory device for operation of same.

Certain embodiments are not limited to the serial presence detection logic residing on the PCB to detect for connectivity of a memory device. For example, some embodiments may provide for a BIOS process, executing with the processor device, to provide a presence detection functionality. In such an embodiment, method 400 may include one or more additional operations (not shown) to determine which presence detection mechanism is available for use. The processor device may perform such operations to determine whether SPD logic on the PCB is accessible or whether, for example, a virtual SPD process of the BIOS is to be used instead. Such determining may be performed prior to the polling at 406 to determine a target of such polling.

Referring now to FIG. 5, the various tables shown each list and describe at least some signals identified by a corresponding memory standard. More particularly, table 500 describes signal to be exchanged by a memory device that is based on a DDR4 standard, table 510 describes signal to be exchanged by a memory device that is based on a LPDDR3 standard, and table 520 describes signal to be exchanged by a memory device that is based on a LPDDR4 standard. The particular details of such memory standards, and signals thereof, are not described herein to avoid obscuring features of certain embodiments.

As described in more detail herein, an interconnect such as one of interconnects 108, 208 may include at least some plurality of signal lines to exchange signals between hardware interfaces disposed on a PCB. The plurality of signal lines may serve as a superset that can accommodate any of multiple sets of signals each specified by a different respective memory standard. Tables 500, 510, 520 represent one example of such different memory standards, and respective signals thereof. However, the interconnect may support fewer, additional and/or other memory standards. Additionally or alternatively, the superset may support fewer, additional and/or other signals specified by some or all such memory standards.

Referring now to FIG. 6, various tables shown each describe a respective set of signals defined by a corresponding memory technology. More particularly, table 600 describes a set of signals identified by a DDR4 standard, table 610 describes a set of signals identified by a LPDDR3 standard, and table 620 describes a set of signals identified by a LPDDR4 standard. Tables 610, 620, 630 are variously organized by signal type – e.g., data (DQ), data mask (DM*), differential data strobe (DQS), etc. – and list a number of signals of the signal type that are identified by the corresponding memory standard. As mentioned with respect to FIG. 5, the DDR4 standard, LPDDR3 standard and LPDDR4 standard are merely one example of different memory standards accommodated according to an embodiment. Other embodiments may accommodate fewer, more and/or other memory standards.

Table 630 illustrates a superset of signals represented by tables 600, 610, 620, where the superset may be accommodated according to an embodiment by signal lines of an interconnect such as one of interconnects 108, 208. The row-wise arrangement of tables 600, 610, 620, 630 illustrate a breakdown of the superset by signal type – e.g., where for a given signal type, the memory standard identifying a largest number of signals of that signal type determines the number of signal lines in the superset that are to support the signal type.

Table 640 illustrates a table of voltages that may be supported according to an embodiment by a voltage regulator such as one of programmable VR 112 and VR 212. Table 640 lists voltages variously specified by a DDR4 standard, a LPDDR3 standard and a LPDDR4 standard, and a superset of such voltages. A VR according to an embodiment may be programmable to provide to a memory device, via a HW interface on a PCB, any of a superset of the voltages specified in table 640.

Referring now to FIGs. 7A-7C, tables 700a, 700b, 700c variously list a mapping of signals to be exchanged between a CPU and any of multiple memory devices each based on a different respective memory standard. Such a CPU may include or operate with pinout-configurable interface circuitry that may implement any of multiple different interface modes each corresponding to a respective one of such memory standards. Tables 700a, 700b, 700c each provide a respective column-wise list of signals that the CPU is capable of exchanging. For memory devices of different memory standards – in this example, DDR3, DDR4, LPDDR3 (including two different configurations thereof) and LPDDR4 – tables 700a, 700b, 700c variously map CPU-side signal identifiers each to respective signal identifiers of the memory standards shown. In table 700c, "NC" stands for "not connected". It is appreciated that a

particular CPU-side signal identifiers may be associated with different I/O contacts of the CPU at different times depending upon a particular input mode of the CPU.

Referring now to FIGs. 8A-8D, tables 810, 820, 830, 840 each list a respective pinout of a corresponding memory device to communicate with a pinout-configurable processor device via a PCB according to an embodiment. More particularly, table 800 lists a pinout of a DDR3L device to couple to a 260-pin connector on the PCB, and table 810 lists a pinout of a DDR4 device to couple to such 260-pin connector. Table 820 lists a pinout of a LPDDR3 device to couple to such a 260-pin connector, and table 830 lists a pinout of a LPDDR4 device to couple to such a 260-pin connector.

Certain embodiments variously identify a memory type of a memory device coupled to a PCB – e.g., including identifying a particular one of the pinouts variously represented in tables 800, 810, 820, 830. In response, an interface mode of a processor device may be configured and a VR mode of a voltage regulator may be programmed to accommodate both the pinout and voltage levels that are specified by the corresponding memory standard.

Referring now to FIGs. 9A-9C, tables 900, 910, 920 each list a respective pinout of a corresponding memory device to communicate with a pinout-configurable processor device via a PCB according to another embodiment. More particularly, table 900 lists a pinout of a DDR4 memory device to couple to a 242-pin connector on the PCB, table 910 lists a pinout of a LPDDR3 memory device to couple to such 242-pin connector, and table 920 lists a pinout of a LPDDR4 memory device to couple to such a 242-pin connector. Certain embodiments variously identify a particular one of the pinouts variously represented in tables 900, 910, 920 as corresponding to a memory device coupled to a PCB. In response, an interface mode of a processor device may be configured, and a VR mode of a voltage regulator may be programmed, to accommodate both the pinout and voltage levels that are specified by the corresponding memory standard.

FIG. 10 is a block diagram of an embodiment of a computing system in which access to a memory device may be implemented. System 1000 represents a computing device in accordance with any embodiment described herein, and may be a laptop computer, a desktop computer, a server, a gaming or entertainment control system, a scanner, copier, printer, or other electronic device. System 1000 may include processor 1020, which provides processing, operation management, and execution of instructions for system 1000. Processor 1020 may include any type of microprocessor, central processing unit (CPU), processing core, or other processing

hardware to provide processing for system 1000. Processor 1020 controls the overall operation of system 1000, and may be or include, one or more programmable general-purpose or special-purpose microprocessors, digital signal processors (DSPs), programmable controllers, application specific integrated circuits (ASICs), programmable logic devices (PLDs), or the like, or a combination of such devices.

Memory subsystem 1030 represents the main memory of system 1000, and provides temporary storage for code to be executed by processor 1020, or data values to be used in executing a routine. Memory subsystem 1030 may include one or more memory devices such as read-only memory (ROM), flash memory, one or more varieties of random access memory (RAM), or other memory devices, or a combination of such devices. Memory subsystem 1030 stores and hosts, among other things, operating system (OS) 1036 to provide a software platform for execution of instructions in system 1000. Additionally, other instructions 1038 are stored and executed from memory subsystem 1030 to provide the logic and the processing of system 1000. OS 1036 and instructions 1038 are executed by processor 1020.

Memory subsystem 1030 may include memory device 1032 where it stores data, instructions, programs, or other items. In one embodiment, memory subsystem includes memory controller 1034, which accesses memory 1032 – e.g., on behalf of processor 1020. Memory controller 1034 may be incorporated into a packaged device including processor 1020 – e.g., where processor 1020 accesses memory 1032 via a PCB (not shown) having disposed therein or thereon components providing functionality such as that discussed herein.

Processor 1020 and memory subsystem 1030 may be coupled to bus/bus system 1010. Bus 1010 is an abstraction that represents any one or more separate physical buses, communication lines/interfaces, and/or point-to-point connections, connected by appropriate bridges, adapters, and/or controllers. Therefore, bus 1010 may include, for example, one or more of a system bus, a Peripheral Component Interconnect (PCI) bus, a HyperTransport or industry standard architecture (ISA) bus, a small computer system interface (SCSI) bus, a universal serial bus (USB), or an Institute of Electrical and Electronics Engineers (IEEE) standard 1394 bus (commonly referred to as "Firewire"). The buses of bus 1010 may also correspond to interfaces in network interface 1050.

System 1000 may also include one or more input/output (I/O) interface(s) 1040, network interface 1050, one or more internal mass storage device(s) 1060, and peripheral interface 1070 coupled to bus 1010. I/O interface 1040 may include one or more interface components through

which a user interacts with system 1000 (e.g., video, audio, and/or alphanumeric interfacing). Network interface 1050 provides system 1000 the ability to communicate with remote devices (e.g., servers, other computing devices) over one or more networks. Network interface 1050 may include an Ethernet adapter, wireless interconnection components, USB (universal serial bus), or other wired or wireless standards-based or proprietary interfaces.

Storage 1060 may be or include any conventional medium for storing large amounts of data in a nonvolatile manner, such as one or more magnetic, solid state, or optical based disks, or a combination. Storage 1060 holds code or instructions and data 1062 in a persistent state (i.e., the value is retained despite interruption of power to system 1000). Storage 1060 may be generically considered to be a "memory," although memory 1030 is the executing or operating memory to provide instructions to processor 1020. Whereas storage 1060 is nonvolatile, memory 1030 may include volatile memory (i.e., the value or state of the data is indeterminate if power is interrupted to system 1000).

Peripheral interface 1070 may include any hardware interface not specifically mentioned above. Peripherals refer generally to devices that connect dependently to system 1000. A dependent connection is one where system 1000 provides the software and/or hardware platform on which operation executes, and with which a user interacts.

FIG. 11 is a block diagram of an embodiment of a mobile device in which access to a memory device may be implemented. Device 1100 represents a mobile computing device, such as a computing tablet, a mobile phone or smartphone, a wireless-enabled e-reader, or other mobile device. It will be understood that certain of the components are shown generally, and not all components of such a device are shown in device 1100. Device 1100 may include processor 1110, which performs the primary processing operations of device 1100. Processor 1110 may include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1110 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting device 1100 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

In one embodiment, device 1100 includes audio subsystem 1120, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions may include speaker and/or headphone output, as well as microphone input. Devices for such functions may be integrated into device 1100, or connected to device 1100. In one embodiment, a user interacts with device 1100 by providing audio commands that are received and processed by processor 1110.

Display subsystem 1130 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device. Display subsystem 1130 may include display interface 1132, which may include the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1132 includes logic separate from processor 1110 to perform at least some processing related to the display. In one embodiment, display subsystem 1130 includes a touchscreen device that provides both output and input to a user.

I/O controller 1140 represents hardware devices and software components related to interaction with a user. I/O controller 1140 may operate to manage hardware that is part of audio subsystem 1120 and/or display subsystem 1130. Additionally, I/O controller 1140 illustrates a connection point for additional devices that connect to device 1100 through which a user might interact with the system. For example, devices that may be attached to device 1100 might include microphone devices, speaker or stereo systems, video systems or other display device, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

As mentioned above, I/O controller 1140 may interact with audio subsystem 1120 and/or display subsystem 1130. For example, input through a microphone or other audio device may provide input or commands for one or more applications or functions of device 1100. Additionally, audio output may be provided instead of or in addition to display output. In another example, if display subsystem includes a touchscreen, the display device also acts as an input device, which may be at least partially managed by I/O controller 1140. There may also be additional buttons or switches on device 1100 to provide I/O functions managed by I/O controller 1140.

In one embodiment, I/O controller 1140 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, gyroscopes, global positioning system

(GPS), or other hardware that may be included in device 1100. The input may be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

In one embodiment, device 1100 includes power management 1150 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1160 may include memory device(s) 1162 for storing information in device 1100. Memory subsystem 1160 may include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory 1160 may store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of system 1100.

In one embodiment, memory subsystem 1160 includes memory controller 1164 (which could also be considered part of the control of system 1100, and could potentially be considered part of processor 1110). Memory controller 1164 may communicate signaling to provide access to memory 1162 – e.g., on behalf of processor 1110. Memory controller 1164 may be incorporated into a packaged device including processor 1110 – e.g., where processor 1110 accesses memory 1162 via a PCB (not shown) having disposed therein or thereon components providing functionality such as that discussed herein.

Connectivity 1170 may include hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable device 1100 to communicate with external devices. The device could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

Connectivity 1170 may include multiple different types of connectivity. To generalize, device 1100 is illustrated with cellular connectivity 1172 and wireless connectivity 1174. Cellular connectivity 1172 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, LTE (long term evolution – also referred to as "4G"), or other cellular service standards. Wireless connectivity 1174 refers to wireless connectivity that is not cellular, and may include personal area networks (such as Bluetooth),

local area networks (such as WiFi), and/or wide area networks (such as WiMax), or other wireless communication. Wireless communication refers to transfer of data through the use of modulated electromagnetic radiation through a non-solid medium. Wired communication occurs through a solid communication medium.

Peripheral connections 1180 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that device 1100 could both be a peripheral device ("to" 1182) to other computing devices, as well as have peripheral devices ("from" 1184) connected to it. Device 1100 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on device 1100. Additionally, a docking connector may allow device 1100 to connect to certain peripherals that allow device 1100 to control content output, for example, to audiovisual or other systems.

In addition to a proprietary docking connector or other proprietary connection hardware, device 1100 may make peripheral connections 1180 via common or standards-based connectors. Common types may include a Universal Serial Bus (USB) connector (which may include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other type.

In one implementation, a device comprises a first hardware (HW) interface to couple a printed circuit board (PCB) to any of memory devices each corresponding to a different respective set of signals of multiple sets of signals, and a second HW interface to couple the PCB to a processor device, wherein the processor device detects connectivity of a memory device to the first HW interface and configures, based on a memory type of the memory device, a first interface mode of interface modes each corresponding to a different respective one of the multiple sets of signals. The device further comprises a voltage regulator (VR) coupled to the first HW interface, the VR to be programmed, based on the memory type, to a first VR mode of VR modes each corresponding to a different respective one of the memory devices, and to provide one or more voltages to the first interface based on the first VR mode, and an interconnect, disposed in or on the PCB, including x signal lines each coupling a respective input/output (I/O) contact of the first HW interface to a respective I/O contact of the second HW interface, wherein x is an integer equal to a total number of signals of a superset of the multiple sets of signals.

In an embodiment, the multiple sets of signals are each specified by a different respective one of multiple memory standards. In another embodiment, the multiple memory standards include one or more dual data rate memory standards. In another embodiment, the one or more dual data rate memory standards include a DDR3 standard or a DDR4 standard. In another embodiment, the one or more dual data rate memory standards include a low power dual data rate memory standard. In another embodiment, the one or more dual data rate memory standards include a LPDDR3 standard or a LPDDR4 standard.

In another embodiment, the device further comprises detector logic disposed in or on the PCB, the detector logic to generate and send to the processor device a signal indicating the connectivity of the memory device to the first HW interface. In another embodiment, the detector logic is based on a serial presence detect standard. In another embodiment, state machine logic identifies the memory type of the memory device in response to the signal indicating the connectivity of the memory device to the first HW interface. In another embodiment, the state machine logic comprises state machine circuitry of the processor device. In another embodiment, the processor device executes a Basic Input/Output System (BIOS) process including the state machine logic. In another embodiment, the first HW interface includes a mechanical connector. In another embodiment, the second HW interface includes a pad array. In another embodiment, the multiple memory devices include one or more dual in-line memory modules.

In another implementation, a system comprises a printed circuit board (PCB), a first hardware (HW) interface disposed in or on the PCB, the first HW interface to couple to any of memory devices each corresponding to a different respective set of signals of multiple sets of signals, a second HW interface disposed in or on the PCB and a processor device coupled to the PCB via the second HW interface, the processor device the processor device to detect connectivity of a memory device to the first HW interface and to configure, based on a memory type of the memory device, a first interface mode of interface modes each corresponding to a different respective one of the multiple sets of signals. The system further comprises a voltage regulator (VR) coupled to the first HW interface, the VR to be programmed, based on the memory type, to a first VR mode of VR modes each corresponding to a different respective one of the memory devices, and to provide one or more voltages to the first interface based on the first VR mode, and an interconnect, disposed in or on the PCB, including x signal lines each coupling a respective input/output (I/O) contact of the first HW interface to a respective I/O

contact of the second HW interface, wherein x is an integer equal to a total number of signals of a superset of the multiple sets of signals.

In an embodiment, the multiple sets of signals are each specified by a different respective one of multiple memory standards. In another embodiment, the multiple memory standards include one or more dual data rate memory standards. In another embodiment, the one or more dual data rate memory standards include a DDR3 standard or a DDR4 standard. In another embodiment, the one or more dual data rate memory standards include a low power dual data rate memory standard. In another embodiment, the one or more dual data rate memory standards include a LPDDR3 standard or a LPDDR4 standard.

In another embodiment, the system further comprises detector logic disposed in or on the PCB, the detector logic to generate and send to the processor device a signal indicating the connectivity of the memory device to the first HW interface. In another embodiment, the detector logic is based on a serial presence detect standard. In another embodiment, state machine logic identifies the memory type of the memory device in response to the signal indicating the connectivity of the memory device to the first HW interface. In another embodiment, the state machine logic comprises state machine circuitry of the processor device. In another embodiment, the processor device executes a Basic Input/Output System (BIOS) process including the state machine logic. In another embodiment, the first HW interface includes a mechanical connector. In another embodiment, the second HW interface includes a pad array. In another embodiment, the multiple memory devices include one or more dual in-line memory modules.

In another implementation, a method comprises detecting connectivity of a memory device to a first hardware interface disposed in or on a printed circuit board (PCB), and in response to detecting the connectivity, identifying a memory type of the memory device, wherein, based on the memory type, a processor device configures a first interface mode of multiple interface modes of the processor device, the multiple interface modes each corresponding to a different respective set of signals of multiple sets of signals, the processor device coupled to the PCB via a second hardware interface disposed in or on the PCB. The method further comprises, based on the memory type, programming a first voltage regulator (VR) mode of multiple VR modes of a VR, the multiple VR modes each corresponding to a different respective one of multiple memory types, wherein the VR provides one or more voltages to the first interface based on the first VR mode, and during operation of the memory device based on the one or more voltages, exchanging signals between the memory device and

the processor device via x signal lines of an interconnect disposed in or on the PCB, wherein x is an integer equal to a total number of signals of a superset of the multiple sets of signals.

In an embodiment, the multiple sets of signals are each specified by a different respective one of multiple memory standards. In another embodiment, the multiple memory standards include one or more dual data rate memory standards. In another embodiment, the one or more dual data rate memory standards include a DDR3 standard or a DDR4 standard. In another embodiment, the one or more dual data rate memory standards include a low power dual data rate memory standard. In another embodiment, the one or more dual data rate memory standards include a LPDDR3 standard or a LPDDR4 standard.

In another embodiment, the method further comprises with detector logic disposed in or on the PCB, generating and sending to the processor device a signal indicating the connectivity of the memory device to the first hardware interface. In another embodiment, the detector logic is based on a serial presence detect standard. In another embodiment, state machine logic identifies the memory type of the memory device in response to the signal indicating the connectivity of the memory device to the first hardware interface. In another embodiment, the state machine logic comprises state machine circuitry of the processor device. In another embodiment, the processor device executes a Basic Input/Output System (BIOS) process including the state machine logic. In another embodiment, the first hardware interface includes a mechanical connector. In another embodiment, the second hardware interface includes a pad array. In another embodiment, the multiple memory devices include one or more dual in-line memory modules.

In another implementation, a computer-readable storage medium has stored thereon instructions which, when executed by one or more processing units, cause the one or more processing units to perform a method comprising detecting connectivity of a memory device to a first hardware interface disposed in or on a printed circuit board (PCB), and in response to detecting the connectivity, identifying a memory type of the memory device, wherein, based on the memory type, a processor device configures a first interface mode of multiple interface modes of the processor device, the multiple interface modes each corresponding to a different respective set of signals of multiple sets of signals, the processor device coupled to the PCB via a second hardware interface disposed in or on the PCB. The method further comprises based on the memory type, programming a first voltage regulator (VR) mode of multiple VR modes of a VR, the multiple VR modes each corresponding to a different respective one of multiple memory types, wherein the VR provides one or more voltages to the first interface based on the first VR

mode, and during operation of the memory device based on the one or more voltages, exchanging signals between the memory device and the processor device via x signal lines of an interconnect disposed in or on the PCB, wherein x is an integer equal to a total number of signals of a superset of the multiple sets of signals.

In an embodiment, the multiple sets of signals are each specified by a different respective one of multiple memory standards. In another embodiment, the multiple memory standards include one or more dual data rate memory standards. In another embodiment, the one or more dual data rate memory standards include a DDR3 standard or a DDR4 standard. In another embodiment, the one or more dual data rate memory standards include a low power dual data rate memory standard. In another embodiment, the one or more dual data rate memory standards include a LPDDR3 standard or a LPDDR4 standard.

In another embodiment, the method further comprises, with detector logic disposed in or on the PCB, generating and sending to the processor device a signal indicating the connectivity of the memory device to the first hardware interface. In another embodiment, the detector logic is based on a serial presence detect standard. In another embodiment, state machine logic identifies the memory type of the memory device in response to the signal indicating the connectivity of the memory device to the first hardware interface. In another embodiment, the state machine logic comprises state machine circuitry of the processor device. In another embodiment, the processor device executes a Basic Input/Output System (BIOS) process including the state machine logic. In another embodiment, the first hardware interface includes a mechanical connector. In another embodiment, the second hardware interface includes a pad array. In another embodiment, the multiple memory devices include one or more dual in-line memory modules.

Techniques and architectures for operating a memory device are described herein. In the above description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of certain embodiments. It will be apparent, however, to one skilled in the art that certain embodiments can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the description.

Reference in the specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase “in one

embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

Some portions of the detailed description herein are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the computing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here, and generally, conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the discussion herein, it is appreciated that throughout the description, discussions utilizing terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

Certain embodiments also relate to apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs) such as dynamic RAM (DRAM), EPROMs, EEPROMs, magnetic or optical cards, or any type of media suitable for storing electronic instructions, and coupled to a computer system bus.

The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general purpose systems may be used with programs in

accordance with the teachings herein, or it may prove convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these systems will appear from the description herein. In addition, certain embodiments are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of such embodiments as described herein.

Besides what is described herein, various modifications may be made to the disclosed embodiments and implementations thereof without departing from their scope. Therefore, the illustrations and examples herein should be construed in an illustrative, and not a restrictive sense. The scope of the invention should be measured solely by reference to the claims that follow.

CLAIMS

What is claimed is:

1. A device comprising:

a first hardware (HW) interface to couple a printed circuit board (PCB) to any of memory devices each corresponding to a different respective set of signals of multiple sets of signals;

a second HW interface to couple the PCB to a processor device, wherein the processor device detects connectivity of a memory device to the first HW interface and configures, based on a memory type of the memory device, a first interface mode of interface modes each corresponding to a different respective one of the multiple sets of signals;

a voltage regulator (VR) coupled to the first HW interface, the VR to be programmed, based on the memory type, to a first VR mode of VR modes each corresponding to a different respective one of the memory devices, and to provide one or more voltages to the first interface based on the first VR mode; and

an interconnect, disposed in or on the PCB, including x signal lines each coupling a respective input/output (I/O) contact of the first HW interface to a respective I/O contact of the second HW interface, wherein x is an integer equal to a total number of signals of a superset of the multiple sets of signals.

2. The device of claim 1, wherein the multiple sets of signals are each specified by a different respective one of multiple memory standards.

3. The device of claim 2, wherein the multiple memory standards include one or more dual data rate memory standards.

4. The device of claim 1, further comprising detector logic disposed in or on the PCB, the detector logic to generate and send to the processor device a signal indicating the connectivity of the memory device to the first HW interface.

5. The device of claim 4, wherein the detector logic is based on a serial presence detect standard.

6. The device of claim 4, wherein state machine logic identifies the memory type of the memory device in response to the signal indicating the connectivity of the memory device to the first HW interface.

7. The device of claim 6, wherein the state machine logic comprises state machine circuitry of the processor device.

8. The device of claim 6, wherein the processor device executes a Basic Input/Output System (BIOS) process including the state machine logic.

9. The device of claim 1, wherein the multiple memory devices include one or more dual in-line memory modules.

10. A system comprising:

a printed circuit board (PCB);

a first hardware (HW) interface disposed in or on the PCB, the first HW interface to couple to any of memory devices each corresponding to a different respective set of signals of multiple sets of signals;

a second HW interface disposed in or on the PCB;

a processor device coupled to the PCB via the second HW interface, the processor device the processor device to detect connectivity of a memory device to the first HW interface and to configure, based on a memory type of the memory device, a first interface mode of interface modes each corresponding to a different respective one of the multiple sets of signals;

a voltage regulator (VR) coupled to the first HW interface, the VR to be programmed, based on the memory type, to a first VR mode of VR modes each corresponding to a different respective one of the memory devices, and to provide one or more voltages to the first interface based on the first VR mode; and

an interconnect, disposed in or on the PCB, including x signal lines each coupling a respective input/output (I/O) contact of the first HW interface to a respective I/O contact of the second HW interface, wherein x is an integer equal to a total number of signals of a superset of the multiple sets of signals.

11. The system of claim 10, wherein the multiple sets of signals are each specified by a different respective one of multiple memory standards.

12. The system of claim 11, wherein the multiple memory standards include one or more dual data rate memory standards.

13. The system of claim 10, further comprising detector logic disposed in or on the PCB, the detector logic to generate and send to the processor device a signal indicating the connectivity of the memory device to the first HW interface.

14. The system of claim 13, wherein the detector logic is based on a serial presence detect standard.

15. The system of claim 13, wherein state machine logic identifies the memory type of the memory device in response to the signal indicating the connectivity of the memory device to the first HW interface.

16. The system of claim 15, wherein the state machine logic comprises state machine circuitry of the processor device.

17. The system of claim 10, wherein the multiple memory devices include one or more dual in-line memory modules.

18. A method comprising:

detecting connectivity of a memory device to a first hardware interface disposed in or on a printed circuit board (PCB);

in response to detecting the connectivity, identifying a memory type of the memory device, wherein, based on the memory type, a processor device configures a first interface mode of multiple interface modes of the processor device, the multiple interface modes each corresponding to a different respective set of signals of multiple sets of signals, the processor device coupled to the PCB via a second hardware interface disposed in or on the PCB;

based on the memory type, programming a first voltage regulator (VR) mode of multiple VR modes of a VR, the multiple VR modes each corresponding to a different respective one of multiple memory types, wherein the VR provides one or more voltages to the first interface based on the first VR mode; and

during operation of the memory device based on the one or more voltages, exchanging signals between the memory device and the processor device via x signal lines of an interconnect disposed in or on the PCB, wherein x is an integer equal to a total number of signals of a superset of the multiple sets of signals.

19. The method of claim 18, wherein the multiple sets of signals are each specified by a different respective one of multiple memory standards.

20. The method of claim 19, wherein the multiple memory standards include one or more dual data rate memory standards.

21. The method of claim 18, wherein the multiple memory devices include one or more dual in-line memory modules.

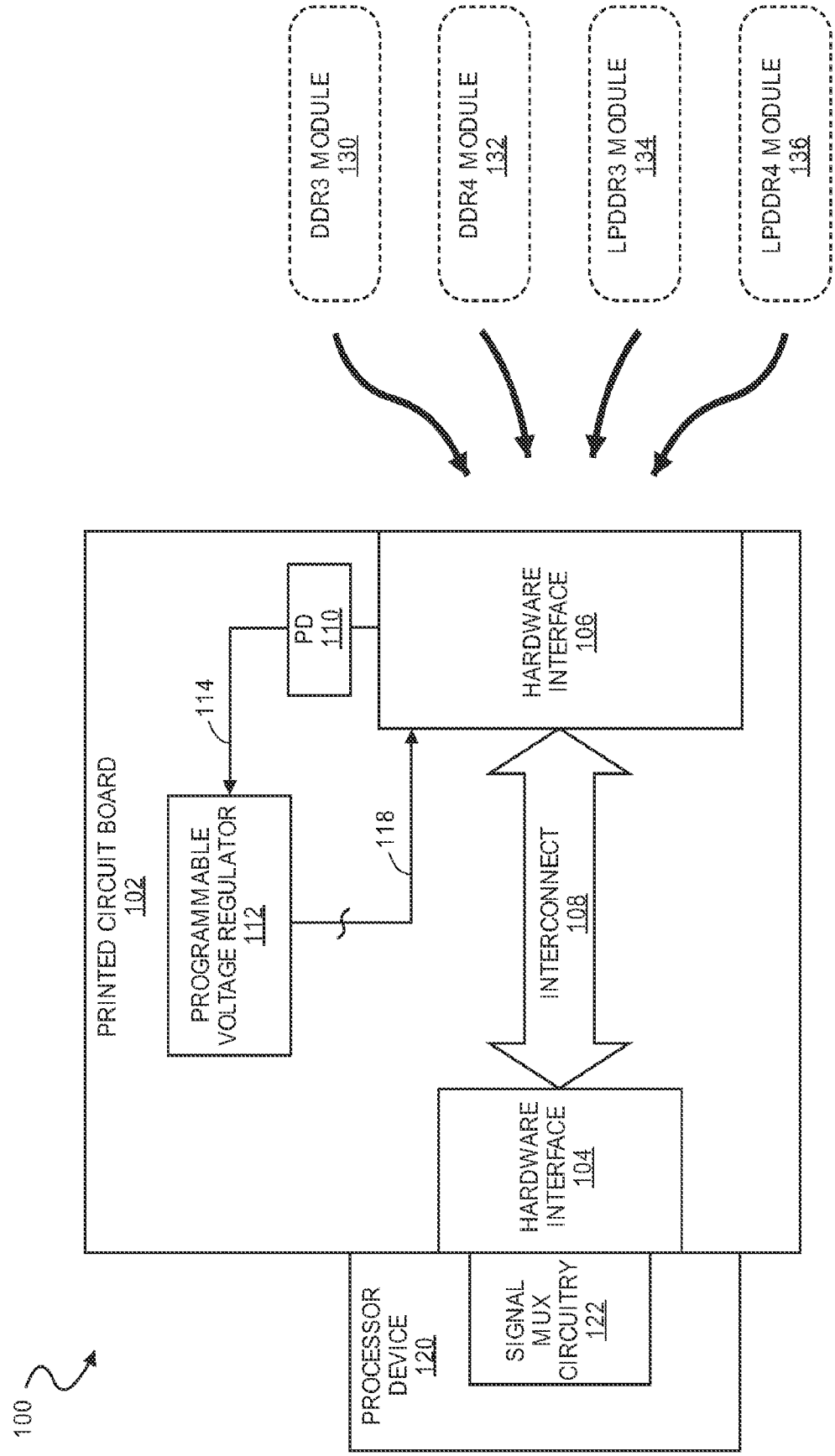

DDR3 MODULE
130
DDR4 MODULE
132
LPDDR3 MODULE
134
LPDDR4 MODULE
136
PRINTED CIRCUIT BOARD
102
PD
110
HARDWARE
INTERFACE
106
114
PROGRAMMABLE
VOLTAGE REGULATOR
112
118
INTERCONNECT
108
HARDWARE
INTERFACE
104
PROCESSOR
DEVICE
120
SIGNAL
MUX
CIRCUITRY
122
100

FIG. 1

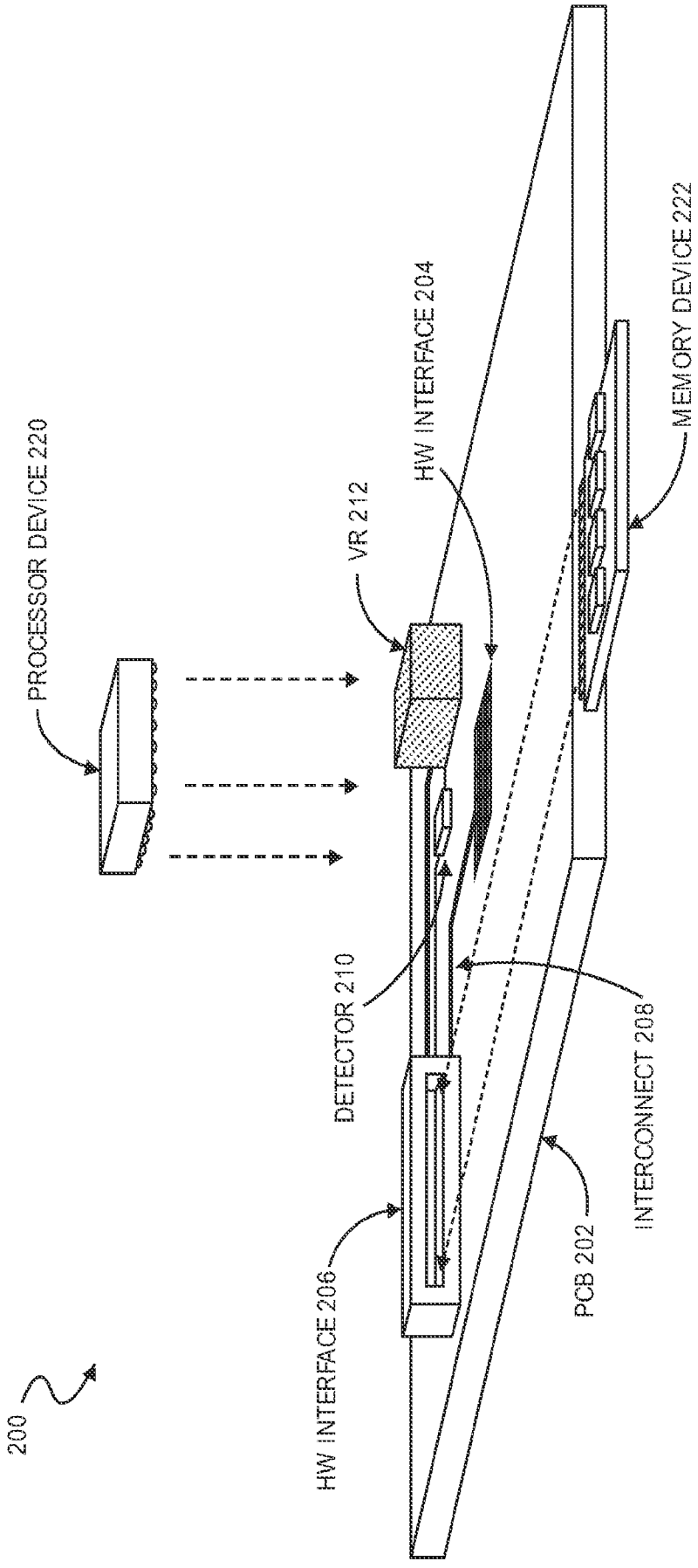

200
PROCESSOR DEVICE 220
VR 212
HW INTERFACE 204
MEMORY DEVICE 222
DETECTOR 210
INTERCONNECT 208
HW INTERFACE 206
PCB 202

FIG. 2

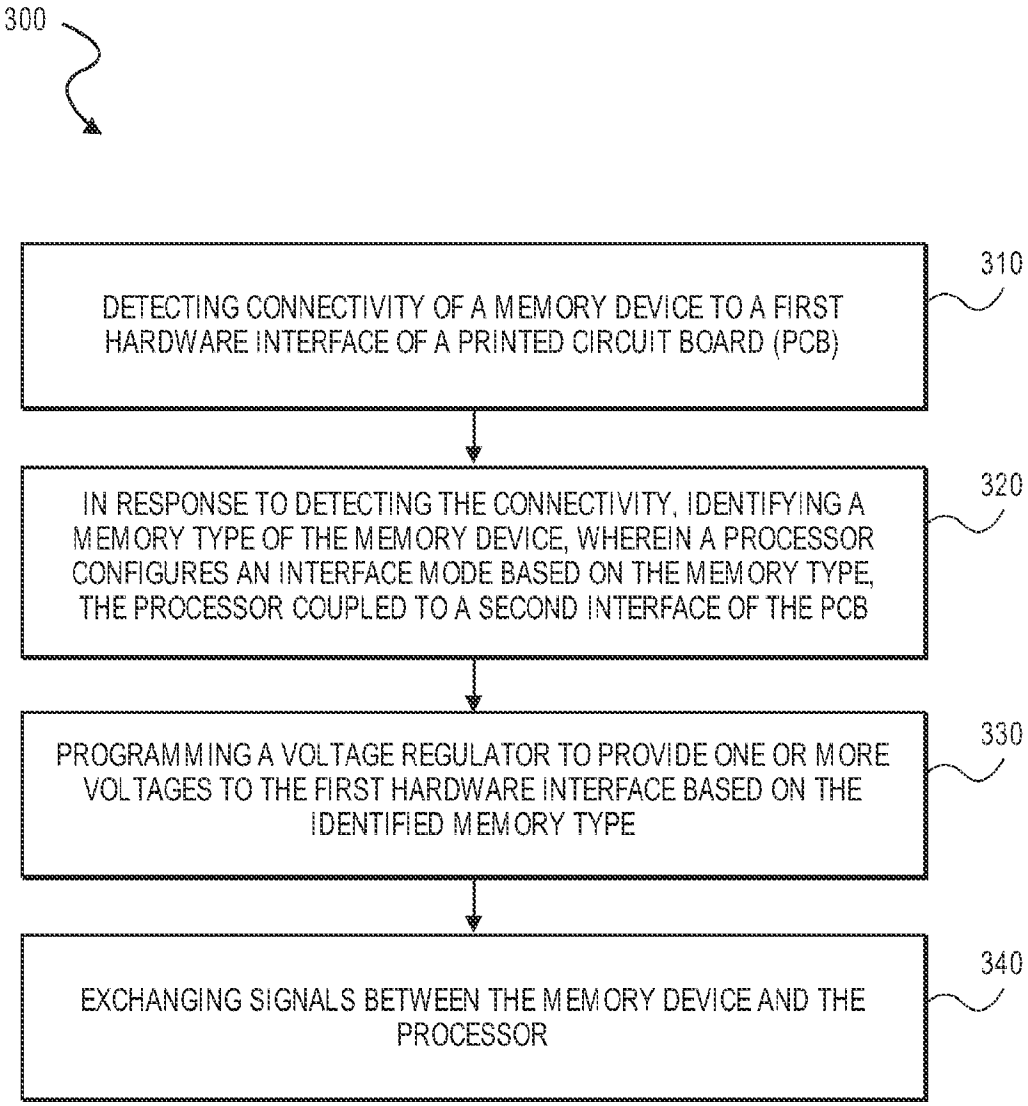

300
DETECTING CONNECTIVITY OF A MEMORY DEVICE TO A FIRST HARDWARE INTERFACE OF A PRINTED CIRCUIT BOARD (PCB)
310
IN RESPONSE TO DETECTING THE CONNECTIVITY, IDENTIFYING A MEMORY TYPE OF THE MEMORY DEVICE, WHEREIN A PROCESSOR CONFIGURES AN INTERFACE MODE BASED ON THE MEMORY TYPE, THE PROCESSOR COUPLED TO A SECOND INTERFACE OF THE PCB
320
PROGRAMMING A VOLTAGE REGULATOR TO PROVIDE ONE OR MORE VOLTAGES TO THE FIRST HARDWARE INTERFACE BASED ON THE IDENTIFIED MEMORY TYPE
330
EXCHANGING SIGNALS BETWEEN THE MEMORY DEVICE AND THE PROCESSOR
340

FIG. 3

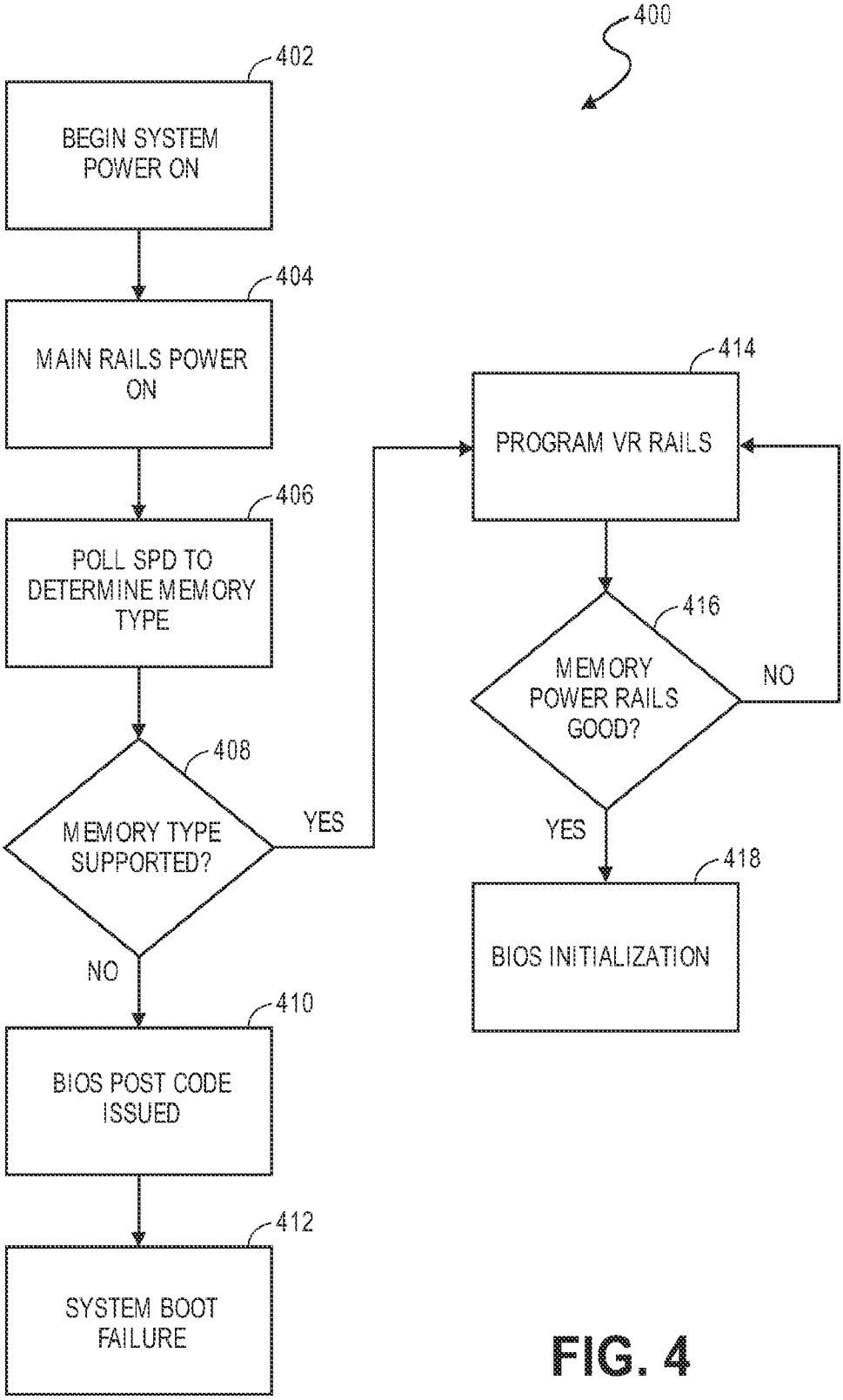

400
402
BEGIN SYSTEM POWER ON
404
MAIN RAILS POWER ON
406
POLL SPD TO DETERMINE MEMORY TYPE
408
MEMORY TYPE SUPPORTED?
YES
NO
410
BIOS POST CODE ISSUED
412
SYSTEM BOOT FAILURE
414
PROGRAM VR RAILS
416
MEMORY POWER RAILS GOOD?
NO
YES
418
BIOS INITIALIZATION

FIG. 4

DDR4 Signal Descriptions 500

Signal Pin (DDR4)	Description
CK_t, CK_c	Clock
CKE, (CKE1)	Clock Enable
CS_n, (CS1_n)	Chip Select
C0,C1,C2	Chip ID
ODT, (ODT1)	On Die Termination
ACT_n	Activation Command Input
RAS_n/A16, CAS_n/	RAS: Row Address/CAS: Column Add
DM_n/DBI_n	Input Data Mask and Data Bus Inversion
BG0 - BG1	Bank Group Inputs
BA0 - BA1	Bank Address Inputs
A0 - A17	Address Inputs
A10 / AP	Auto-precharge
A12 / BC_n	Burst Chop
RESET_n	Reset
PAR	Command and Address Parity

LPDDR3 Signal Descriptions 510

Signal Pin (LPDDR3)	Description
CK_t, CK_c	Clock
CKE	Clock Enable
CS_n	Chip Select
CA0-CA9	Command/Address Inputs
DQ	Data Input/Output
DM	Input Data Mask
ODT	On Die Termination

LPDDR4 Signal Descriptions 520

Signal Pin (LPDDR4)	Description
CK_t_A	Clock
CK_c_A	
CK_t_B	
CK_c_B	
CKE_A	Clock Enable
CKE_B	
CS_A/CS_B	Chip Select
CAA/CAB	Command/Address Inputs
ODT	On Die Termination
DQ	Data Input/Output
DQS	Data Strobe
DMI[1:0]_A/DMI[1:0]_B	Data Mask Inversion
RESET_n	Reset

FIG. 5

DDR4 set 600

DDR4	# of Signals
DQ	64
DM'	8
DQS'	18
CKE'	2
CS'	2
CK0'	2
CK1'	2
A'	19
B'	4
VDD_SPD	1
VPP	2
VTT	1
VREFDQ	0
Vref_CA	0
RESET_n	1
ALERT_n	1
Parity	1
SDA	1
SA0	1
SA1	1
SCL	1
Total	**132**

LPDDR3 set 610

LPDDR3	# of Signals
DQ	64
DM'	8
DQS'	16
CKE'	4
CS'	4
CK0'	2
CK1'	2
'CAA'	10
'CAB'	10
VDD_SPD	0
VPP	0
VTT	0
VREFDQ	1
Vref_CA	1
RESET_n	0
ALERT_n	0
Parity	0
SDA	1
SA0	1
SA1	1
SCL	1
Total	**126**

LPDDR4 set 620

LPDDR4	# of Signals
DQ	64
DM'	8
DQS'	16
CKE'	4
CS'	4
CK0'	2
CK1'	2
'CAA'	6
'CAB'	6
VDD_SPD	0
VPP	0
VTT	0
VREFDQ	0
Vref_CA	0
RESET_n	1
ALERT_n	0
Parity	0
SDA	1
SA0	1
SA1	1
SCL	1
Total	**117**

Superset 630

Super Set	# of Signals
DQ	64
DM'	8
DQS'	18
CKE'	4
CS'	4
CK0'	2
CK1'	2
'CAA'	19
'CAB'	1
VDD_SPD	1
VPP	2
VTT	1
VREFDQ	1
Vref_CA	1
RESET_n	1
ALERT_n	1
Parity	1
SDA	1
SA0	1
SA1	1
SCL	1
Total	**144**

FIG. 6

Voltage Table 640

Voltage	DDR4	LP3	LP4	Super set
VDD_SPD	1.7-3.3V	1.7-3.3V	1.7-3.3V	1.7-3.3V
VDD	1.2V	1.2V	1.1V	1.1 and 1.2
VDDQ	1.2V	1.2V	1.1V	1.1 and 1.2
VPP	2.5V	1.8V	1.8V	2.5 and 1.8

FIG. 6 (CONT.)

Signal Mapping 700a

CPU (1 DPC)	DDR3 (Slot 0)	DDR4 (Slot 0)	LP3 (2Rx64) (1DPC Only)	LP3 (2x2Rx32) (1DPC Only)	LP4 (2x2Rx32) (1DPC Only)
CLK_P[0]	CLK_P[0]	CLK_P[0]	CKA_P[0]	CKA_P[0]	CKA_P[0]
CLK_N[0]	CLK_N[0]	CLK_N[0]	CKA_N[0]	CKA_N[0]	CKA_N[0]
CLK_P[1]	CLK_P[1]	CLK_P[1]	CKB_P[0]	CKB_P[0]	CKB_P[0]
CLK_N[1]	CLK_N[1]	CLK_N[1]	CKB_N[0]	CKB_N[0]	CKB_N[0]
CS_N[0]	CS_N[0]	CS_N[0]	CS_N[0]	CS_A_N[0]	CS_A[0]
CS_N[1]	CS_N[1]	CS_N[1]	CS_N[1]	CS_B_N[1]	CS_B[1]
CS_N[2]		CS_N[0]		CS_A_N[1]	
CS_N[3]		CS_N[1]		CS_B_N[0]	
CS/ODT[0]	ODT[0]	ODT[0]	ODT[0]	ODT_A[0]	CS_A[1]
CS/ODT[1]	ODT[1]	ODT[1]		ODT_B[0]	CS_B[0]
CKE[0]	CKE[0]	CKE[0]	CKE_A[0]	CKE_A[0]	CKE_A[0]
CKE[1]	CKE[1]	CKE[1]	CKE_A[1]	CKE_A[1]	CKE_A[1]
CKE[2]			CKE_B[0]	CKE_B[0]	CKE_B[0]
CKE[3]	CKE[1]'	CKE[1]'	CKE_B[1]	CKE_B[1]	CKE_B[1]
CKE[4]					
CKE[5]					
CKE[6]					
CKE[7]					

FIG. 7A

MA[0]	MA[0]	MA[0]	CAB[9]	CAB[9]	
MA[1]	MA[1]	MA[1]	CAB[8]	CAB[8]	
MA[2]	MA[2]	MA[2]	CAB[5]	CAB[5]	CAB[5]
MA[3]	MA[3]	MA[3]			X
MA[4]	MA[4]	MA[4]			X
MA[5]	MA[5]	MA[5]	CAA[0]	CAA[0]	CAA[0]
MA[6]	MA[6]	MA[6]	CAA[2]	CAA[2]	CAA[2]
MA[7]	MA[7]	MA[7]	CAA[4]	CAA[4]	CAA[4]
MA[8]	MA[8]	MA[8]	CAA[3]	CAA[3]	CAA[2]
MA[9]	MA[9]	MA[9]	CAA[1]	CAA[1]	CAA[1]
MA[10]	MA[10]	MA[10]	CAB[7]	CAB[7]	
MA[11]	MA[11]	MA[11]	CAA[7]	CAA[7]	
MA[12]	MA[12]	MA[12]	CAA[6]	CAA[6]	
MA[13]	MA[13]	MA[13]	CAB[0]	CAB[0]	CAB[0]
MA[14]	MA[14]	BG[1]	CAA[9]	CAA[9]	
MA[15]	MA[15]	ACT_N	CAA[8]	CAA[8]	
RAS_N	RAS_N	A16/RAS_n	CAB[3]	CAB[3]	CAB[3]
CAS_N	CAS_N	A15/CAS_n	CAB[1]	CAB[1]	CAB[1]
WE_N	WE_N	A14/WE_n	CAB[2]	CAB[2]	CAB[2]
BA[0]	BA[0]	BA[0]	CAB[4]	CAB[4]	CAB[4]
BA[1]	BA[1]	BA[1]	CAB[6]	CAB[6]	
BA[2]	BA[2]	BG[0]	CAA[5]	CAA[5]	CAA[5]
New		C0			
New		C1			
PARITY		PARITY			
ALERT		ALERT			

FIG. 7A (CONT.)

Signal Mapping (cont'd) 700b

CPU (1 DPC)	DDR3 (Slot 0)	DDR4 (Slot 0)	LP3 (2Rx64) (1DPC Only)	LP3 (2x2Rx32) (1DPC Only)	LP4 (2x2Rx32) (1DPC Only)
DQ[0]	DQ[0]	DQ[0]	DQ[0]	DQ[0]	DQA[0]
DQ[1]	DQ[1]	DQ[1]	DQ[1]	DQ[1]	DQA[1]
DQ[2]	DQ[2]	DQ[2]	DQ[2]	DQ[2]	DQA[2]
DQ[3]	DQ[3]	DQ[3]	DQ[3]	DQ[3]	DQA[3]
DQ[4]	DQ[4]	DQ[4]	DQ[4]	DQ[4]	DQA[4]
DQ[5]	DQ[5]	DQ[5]	DQ[5]	DQ[5]	DQA[5]
DQ[6]	DQ[6]	DQ[6]	DQ[6]	DQ[6]	DQA[6]
DQ[7]	DQ[7]	DQ[7]	DQ[7]	DQ[7]	DQA[7]
DQ[8]	DQ[8]	DQ[8]	DQ[8]	DQ[8]	DQA[8]
DQ[9]	DQ[9]	DQ[9]	DQ[9]	DQ[9]	DQA[9]
DQ[10]	DQ[10]	DQ[10]	DQ[10]	DQ[10]	DQA[10]
DQ[11]	DQ[11]	DQ[11]	DQ[11]	DQ[11]	DQA[11]
DQ[12]	DQ[12]	DQ[12]	DQ[12]	DQ[12]	DQA[12]
DQ[13]	DQ[13]	DQ[13]	DQ[13]	DQ[13]	DQA[13]
DQ[14]	DQ[14]	DQ[14]	DQ[14]	DQ[14]	DQA[14]
DQ[15]	DQ[15]	DQ[15]	DQ[15]	DQ[15]	DQA[15]
DQ[16]	DQ[16]	DQ[16]	DQ[16]	DQ[16]	DQA[16]
DQ[17]	DQ[17]	DQ[17]	DQ[17]	DQ[17]	DQA[17]
DQ[18]	DQ[18]	DQ[18]	DQ[18]	DQ[18]	DQA[18]
DQ[19]	DQ[19]	DQ[19]	DQ[19]	DQ[19]	DQA[19]
DQ[20]	DQ[20]	DQ[20]	DQ[20]	DQ[20]	DQA[20]

FIG. 7B

DQ[21]	DQ[21]	DQ[21]	DQ[21]	DQ[21]	DQA[21]
DQ[22]	DQ[22]	DQ[22]	DQ[22]	DQ[22]	DQA[22]
DQ[23]	DQ[23]	DQ[23]	DQ[23]	DQ[23]	DQA[23]
DQ[24]	DQ[24]	DQ[24]	DQ[24]	DQ[24]	DQA[24]
DQ[25]	DQ[25]	DQ[25]	DQ[25]	DQ[25]	DQA[25]
DQ[26]	DQ[26]	DQ[26]	DQ[26]	DQ[26]	DQA[26]
DQ[27]	DQ[27]	DQ[27]	DQ[27]	DQ[27]	DQA[27]
DQ[28]	DQ[28]	DQ[28]	DQ[28]	DQ[28]	DQA[28]
DQ[29]	DQ[29]	DQ[29]	DQ[29]	DQ[29]	DQA[29]
DQ[30]	DQ[30]	DQ[30]	DQ[30]	DQ[30]	DQA[30]
DQ[31]	DQ[31]	DQ[31]	DQ[31]	DQ[31]	DQA[31]
DQ[32]	DQ[32]	DQ[32]	DQ[32]	DQ[32]	DQB[0]
DQ[33]	DQ[33]	DQ[33]	DQ[33]	DQ[33]	DQB[1]
DQ[34]	DQ[34]	DQ[34]	DQ[34]	DQ[34]	DQB[2]
DQ[35]	DQ[35]	DQ[35]	DQ[35]	DQ[35]	DQB[3]
DQ[36]	DQ[36]	DQ[36]	DQ[36]	DQ[36]	DQB[4]
DQ[37]	DQ[37]	DQ[37]	DQ[37]	DQ[37]	DQB[5]
DQ[38]	DQ[38]	DQ[38]	DQ[38]	DQ[38]	DQB[6]
DQ[39]	DQ[39]	DQ[39]	DQ[39]	DQ[39]	DQB[7]
DQ[40]	DQ[40]	DQ[40]	DQ[40]	DQ[40]	DQB[8]

FIG. 7B (CONT.)

Signal Mapping (cont'd) 700c

CPU (1 DPC)	DDR3 (Slot 0)	DDR4 (Slot 0)	LP3 (2Rx64) (1DPC Only)	LP3 (2x2Rx32) (1DPC Only)	LP4 (2x2Rx32) (1DPC Only)
DQ[41]	DQ[41]	DQ[41]	DQ[41]	DQ[41]	DQB[9]
DQ[42]	DQ[42]	DQ[42]	DQ[42]	DQ[42]	DQB[10]
DQ[43]	DQ[43]	DQ[43]	DQ[43]	DQ[43]	DQB[11]
DQ[44]	DQ[44]	DQ[44]	DQ[44]	DQ[44]	DQB[12]
DQ[45]	DQ[45]	DQ[45]	DQ[45]	DQ[45]	DQB[13]
DQ[46]	DQ[46]	DQ[46]	DQ[46]	DQ[46]	DQB[14]
DQ[47]	DQ[47]	DQ[47]	DQ[47]	DQ[47]	DQB[15]
DQ[48]	DQ[48]	DQ[48]	DQ[48]	DQ[48]	DQB[16]
DQ[29]	DQ[29]	DQ[29]	DQ[29]	DQ[29]	DQB[17]
DQ[50]	DQ[50]	DQ[50]	DQ[50]	DQ[50]	DQB[18]
DQ[51]	DQ[51]	DQ[51]	DQ[51]	DQ[51]	DQB[19]
DQ[52]	DQ[52]	DQ[52]	DQ[52]	DQ[52]	DQB[20]
DQ[53]	DQ[53]	DQ[53]	DQ[53]	DQ[53]	DQB[21]
DQ[54]	DQ[54]	DQ[54]	DQ[54]	DQ[54]	DQB[22]
DQ[35]	DQ[35]	DQ[35]	DQ[35]	DQ[35]	DQB[23]
DQ[56]	DQ[56]	DQ[56]	DQ[56]	DQ[56]	DQB[24]
DQ[57]	DQ[57]	DQ[57]	DQ[57]	DQ[57]	DQB[25]
DQ[58]	DQ[58]	DQ[58]	DQ[58]	DQ[58]	DQB[26]
DQ[59]	DQ[59]	DQ[59]	DQ[59]	DQ[59]	DQB[27]
DQ[60]	DQ[60]	DQ[60]	DQ[60]	DQ[60]	DQB[28]
DQ[61]	DQ[61]	DQ[61]	DQ[61]	DQ[61]	DQB[29]
DQ[62]	DQ[62]	DQ[62]	DQ[62]	DQ[62]	DQB[30]
DQ[63]	DQ[63]	DQ[63]	DQ[63]	DQ[63]	DQB[31]
NC	DM/DBI[0]	DM/DBI[0]	DM/DBI[0]	DM/DBI[0]	DM/DBIA[0]
NC	DM/DBI[1]	DM/DBI[1]	DM/DBI[1]	DM/DBI[1]	DM/DBIA[1]
NC	DM/DBI[2]	DM/DBI[2]	DM/DBI[2]	DM/DBI[2]	DM/DBIA[2]
NC	DM/DBI[3]	DM/DBI[3]	DM/DBI[3]	DM/DBI[3]	DM/DBIA[3]
NC	DM/DBI[4]	DM/DBI[4]	DM/DBI[4]	DM/DBI[4]	DM/DBIB[0]
NC	DM/DBI[5]	DM/DBI[5]	DM/DBI[5]	DM/DBI[5]	DM/DBIB[1]
NC	DM/DBI[6]	DM/DBI[6]	DM/DBI[6]	DM/DBI[6]	DM/DBIB[2]
NC	DM/DBI[7]	DM/DBI[7]	DM/DBI[7]	DM/DBI[7]	DM/DBIB[3]

FIG. 7C

DQS_P[0]	DQS_P[0]	DQS_P[0]	DQS_P[0]	DQS_P[0]	DQSA_P[0]
DQS_N[0]	DQS_N[0]	DQS_N[0]	DQS_N[0]	DQS_N[0]	DQSA_N[0]
DQS_P[1]	DQS_P[1]	DQS_P[1]	DQS_P[1]	DQS_P[1]	DQSA_P[1]
DQS_N[1]	DQS_N[1]	DQS_N[1]	DQS_N[1]	DQS_N[1]	DQSA_N[1]
DQS_P[2]	DQS_P[2]	DQS_P[2]	DQS_P[2]	DQS_P[2]	DQSA_P[2]
DQS_N[2]	DQS_N[2]	DQS_N[2]	DQS_N[2]	DQS_N[2]	DQSA_N[2]
DQS_P[3]	DQS_P[3]	DQS_P[3]	DQS_P[3]	DQS_P[3]	DQSA_P[3]
DQS_N[3]	DQS_N[3]	DQS_N[3]	DQS_N[3]	DQS_N[3]	DQSA_N[3]
DQS_P[4]	DQS_P[4]	DQS_P[4]	DQS_P[4]	DQS_P[4]	DQSB_P[0]
DQS_N[4]	DQS_N[4]	DQS_N[4]	DQS_N[4]	DQS_N[4]	DQSB_N[0]
DQS_P[5]	DQS_P[5]	DQS_P[5]	DQS_P[5]	DQS_P[5]	DQSB_P[1]
DQS_N[5]	DQS_N[5]	DQS_N[5]	DQS_N[5]	DQS_N[5]	DQSB_N[1]
DQS_P[6]	DQS_P[6]	DQS_P[6]	DQS_P[6]	DQS_P[6]	DQSB_P[2]
DQS_N[6]	DQS_N[6]	DQS_N[6]	DQS_N[6]	DQS_N[6]	DQSB_N[2]
DQS_P[7]	DQS_P[7]	DQS_P[7]	DQS_P[7]	DQS_P[7]	DQSB_P[3]
DQS_N[7]	DQS_N[7]	DQS_N[7]	DQS_N[7]	DQS_N[7]	DQSB_N[3]

FIG. 7C (CONT.)

DDR3L Mode Pinout (260-pin connector) 800

Pin #	Front side	Pin #	Back side
1	RSVD	2	RSVD
3	RSVD	4	RSVD
5	VSS	6	VSS
7	DQ0	8	DQ4
9	DQ1	10	DQ5
11	VSS	12	VSS
13	DQS0_c	14	DM0/DBI0
15	DQS0_t	16	VSS
17	VSS	18	DQ6
19	DQ2	20	DQ7
21	DQ3	22	VSS
23	VSS	24	DQ12
25	DQ8	26	DQ13
27	DQ9	28	VSS
29	VSS	30	DQS1_c
31	DM1/DBI1	32	DQS1_t
33	VSS	34	VSS
35	DQ10	36	DQ14
37	DQ11	38	DQ15
39	VSS	40	VSS
41	DQ16	42	DQ20
43	DQ17	44	DQ21
45	VSS	46	VSS
47	DQS2_c	48	DM2/DBI2
49	DQS2_t	50	VSS
51	VSS	52	DQ22
53	DQ18	54	DQ23
55	DQ19	56	VSS
57	VSS	5	DQ28
59	DQ24	60	DQ29
61	DQ25	62	VSS
63	VSS	64	DQS3_c
65	DM3/DBI3	66	DQS3_t
67	VSS	68	VSS
69	DQ26	70	DQ30

Pin #	Front side	Pin #	Back side
127	A6	128	A4
129	VSS	130	VSS
131	A3	132	A2
133	A1	134	EVENT_n
135	VSS	136	VSS
137	CLK0_t	138	CLK1_t
139	CLK0_c	140	CLK1_c
141	VSS	142	VSS
143	Not Used	144	A0
145	BA1	146	A10
147	VSS	148	VSS
149	RFU	150	BA0
151	WE_n	52	RAS_n
153	VSS	154	VSS
155	RFU	156	A13
157	CS0_n	158	CAS_n
159	VSS	160	VSS
161	ODT0	162	CS1_n
163	CS2_n	164	ODT1
165	VSS	166	VSS
167	CS3_n	168	VREF_CA
169	VSS	170	VSS
171	VDD	172	VDD
173	VDD	174	VDD
175	VDD	176	VDD
177	VDD	178	VDD
179	VDD	180	VDD
181	VSS	182	VSS
183	DQ32	184	DQ36
185	DQ33	186	DQ37
187	VSS	188	VSS
189	DQS3_c	190	DM4/DBI4
191	DQS3_t	192	VSS
193	VSS	194	DQ38
195	DQ34	196	DQ39

FIG. 8A

71	DQ27	72	DQ31
73	VSS	74	VSS
75	CB0	76	CB4
77	CB1	78	CB5
79	VSS	80	VSS
81	DQS8_c	82	DM8/DBI8
83	DQS8_t	84	VSS
85	VSS	86	CB6
87	CB2	88	CB7
89	CB3	90	VSS
91	VSS	92	VREF_DQ
93	VDD	94	VDD
95	VDD	96	VDD
97	VDD	98	VDD
99	VDD	100	VDD
101	VSS	102	RESET_n
Key		Key	
103	CKE0	104	CKE1
105	VSS	106	VSS
107	CKE2	108	CKE3
109	Not Used	110	Not Used
111	VSS	112	VSS
113	A14	114	A15
115	BA2	116	Not Used
117	VSS	118	VSS
119	A12	120	A11
121	A9	122	A7
123	VSS	124	VSS
125	A8	126	A5

197	DQ35	198	VSS
199	VSS	200	DQ44
201	DQ40	202	DQ45
203	DQ41	204	VSS
205	VSS	206	DQS5_c
207	DM5/DBI5	208	DQS5_t
209	VSS	210	VSS
211	DQ42	212	DQ46
213	DQ43	214	DQ47
215	VSS	216	VSS
217	DQ48	218	DQ52
219	DQ49	220	DQ53
221	VSS	222	VSS
223	DQS6_c	224	DM6/DBI6
225	DQS6_t	226	VSS
227	VSS	228	DQ54
229	DQ50	230	DQ55
231	DQ51	232	VSS
233	VSS	234	DQ60
235	DQ56	236	DQ61
237	DQ57	238	VSS
239	VSS	240	DQS7_c
241	DM7/DBI7	242	DQS7_t
243	VSS	244	VSS
245	DQ58	246	DQ62
247	DQ59	248	DQ63
249	VSS	250	VSS
251	SCL	252	SDA
253	VDD_SPD	254	SA0
255	SA2	256	SA1
257	VPP	258	VTT
259	VPP	260	VTT

FIG. 8A (CONT.)

DDR4 Mode Pinout (260-pin connector) 810

Pin #	Front side	Pin #	Back side
1	VSS	2	VSS
3	DQ5	4	DQ4
5	VSS	6	VSS
7	DQ1	8	DQ0
9	VSS	10	VSS
11	DQS0_C	12	DM0_n/DBIO_n
13	DQS0_t	14	VSS
15	VSS	16	DQ6
17	DQ7	18	VSS
19	VSS	20	DQ2
21	DQ3	22	VSS
23	VSS	24	DQ12
25	DQ13	26	VSS
27	VSS	28	DQ8
29	DQ9	30	VSS
31	VSS	32	DQS1_c
33	D,1_n/DBI1_n	34	DQS1_t
35	VSS	36	VSS
37	DQ15	38	DQ14
39	VSS	40	VSS
41	DQ10	42	DQ11
43	VSS	44	VSS
45	DQ21	46	DQ20
47	VSS	48	VSS
49	DQ17	50	DQ16
51	VSS	52	VSS
53	DQS2_c	54	DM2_n/DBI2_n
55	DQS2_t	56	VSS
57	VSS	5	DQ22
59	DQ23	60	VSS
61	VSS	62	DQ18
63	DQ19	64	VSS
65	VSS	66	DQ28
67	DQ29	68	VSS
69	VSS	70	DQ24

Pin #	Front side	Pin #	Back side
135	VDD	136	VDD
137	CK0_t	138	CD1_t
139	CK0_c	140	CK1_c
141	VDD	142	VDD
143	Parity	144	A0
KEY		KEY	
145	BA1	146	A10/AP
147	VDD	148	VDD
149	CS0_n	150	BA0
151	A14/WE_n	152	A16/RAS_n
153	VDD	154	VDD
155	ODT0	156	A15/CAS_n
157	CS1_n	158	A13
159	VDD	160	VDD
161	ODT1	162	C0, CS2_n
163	VDD	164	VREFCA
165	C1, CS3_n	166	SA2
167	VSS	168	VSS
169	DQ37	170	DQ36
171	VSS	172	VSS
173	DQ33	174	DQ32
175	VSS	176	VSS
177	DQS4_c	178	DM4_n/DBI4_n
179	DQS4_t	180	VSS
181	VSS	182	DQ39
183	DQ38	184	VSS
185	VSS	186	DQ35
187	DQ34	188	VSS
189	VSS	190	DQ45
191	DQ44	192	VSS
193	VSS	194	DQ41
195	DQ40	196	VSS

FIG. 8B

71	DQ25	72	VSS
73	VSS	74	DQS3_c
75	DM3_n/DBI3_n	76	DQS3_t
77	VSS	78	VSS
79	DQ30	80	DQ31
81	VSS	82	VSS
83	DQ26	84	DQ27
85	VSS	86	VSS
87	CB5, NC	88	CB4, NC
89	VSS	90	VSS
91	CB1, NC	92	CB0, NC
93	VSS	94	VSS
95	DQS8_c	96	DBI8_n
97	DQS8_t	98	VSS
99	VSS	100	CB6, NC
101	CB2, NC	102	VSS
103	VSS	104	CB7, NC
105	CB3, NC	106	VSS
107	VSS	108	RESET_n
109	CKE0	110	CKE1
111	VDD	112	VDD
113	BG1	114	ACT_n
115	BG0	116	ALERT_n
117	VDD	118	VDD
119	A12	120	A11
121	A9	122	A7
123	VDD	124	VDD
125	A8	126	A5
127	A6	128	A4
129	VDD	130	VDD
131	A3	132	A2
133	A1	134	EVENT_n

197	VSS	198	DQS5_C
199	DM5_n/DBI5_n	200	DQS5_t
201	VSS	202	VSS
203	DQ46	204	DQ47
205	VSS	206	VSS
207	DQ42	208	DQ43
209	VSS	210	VSS
211	DQ52	212	DQ53
213	VSS	214	VSS
215	DG49	216	DQ48
217	VSS	218	VSS
219	DQS6_c	220	DM6_n/DBI6_n
221	DQS6_t	222	VSS
223	VSS	224	DQ54
225	DQ55	226	VSS
227	VSS	228	DQ50
229	DQ51	230	VSS
231	VSS	232	DQ60
233	DQ61	234	VSS
235	VSS	236	DQ57
237	DQ58	238	VSS
239	VSS	240	DQS7_c
241	DM7_n/DBI7_n	242	DQS7_t
243	VSS	244	VSS
245	DQ62	246	DQ63
247	VSS	248	VSS
249	DQ58	250	DQ59
251	VSS	252	VSS
253	SCL	254	SDA
255	VDD SPD	256	SA0
257	VPP	258	VTT
259	VPP	260	SA1

FIG. 8B (CONT.)

LPDDR3 Mode Pinout (260-pin connector) 820

Pin #	Front side	Pin #	Back side
1	RSVD	2	RSVD
3	RSVD	4	RSVD
5	VSS	6	VSS
7	DQ0	8	DQ4
9	DQ1	10	DQ5
11	VSS	12	VSS
13	DQS0_c	14	DM0/DBI0
15	DQS0_t	16	VSS
17	VSS	18	DQ6
19	DQ2	20	DQ7
21	DQ3	22	VSS
23	VSS	24	DQ12
25	DQ8	26	DQ13
27	DQ9	28	VSS
29	VSS	30	DQS1_c
31	DM1/DBI1	32	DQS1_t
33	VSS	34	VSS
35	DQ10	36	DQ14
37	DQ11	38	DQ15
39	VSS	40	VSS
41	DQ16	42	DQ20
43	DQ17	44	DQ21
45	VSS	46	VSS
47	DQS2_c	48	DM2/DBI2
49	DQS2_t	50	VSS
51	VSS	52	DQ22
53	DQ18	54	DQ23
55	DQ19	56	VSS
57	VSS	5	DQ28
59	DQ24	60	DQ29
61	DQ25	62	VSS
63	VSS	64	DQS3_c
65	DM3/DBI3	66	DQS3_t
67	VSS	68	VSS
69	DQ26	70	DQ30

Pin #	Front side	Pin #	Back side
127	CAA_02	128	Not Used
129	VSS	130	VSS
131	Not Used	132	CAB_05
133	CAB_08	134	EVENT_n
135	VSS	136	VSS
137	CLKA_t	138	CLKB_t
139	CLKA_c	140	CLKB_c
141	VSS	142	VSS
143	Not Used	144	CAB_09
145	CAB_06	146	CAB_07
147	VSS	148	VSS
149	RFU	150	CAB_04
151	CAB_02	52	CAB_03
153	VSS	154	VSS
155	RFU	156	CAB_00
157	CSA0_n	158	CAB_01
159	VSS	160	VSS
161	ODTA0	162	CSB1_n
163	CSA1_n	164	ODTB0
165	VSS	166	VSS
167	CSB0_n	168	VREF_CA
169	VSS	170	VSS
171	VDD	172	VDD
173	VDD	174	VDD
175	VDD	176	VDD
177	VDD	178	VDD
179	VDD	180	VDD
181	VSS	182	VSS
183	DQ32	184	DQ36
185	DQ33	186	DQ37
187	VSS	188	VSS
189	DQS4_c	190	DM4/DBI4
191	DQS4_t	192	VSS
193	VSS	194	DQ38
195	DQ34	196	DQ39

FIG. 8C

71	DQ27	72	DQ31
73	VSS	74	VSS
75	Not Used	76	Not Used
77	Not Used	78	Not Used
79	VSS	80	VSS
81	Not Used	82	Not Used
83	Not Used	84	VSS
85	VSS	86	Not Used
87	Not Used	88	Not Used
89	Not Used	90	VSS
91	VSS	92	VREF_DQ
93	VDD	94	VDD
95	VDD	96	VDD
97	VDD	98	VDD
99	VDD	100	VDD
101	VSS	102	RESET_n
Key		Key	
103	CKEA0	104	CKEA1
105	VSS	106	VSS
107	CKEB0	108	CKEB1
109	Not Used	110	Not Used
111	VSS	112	VSS
113	CAA_09	114	CAA_08
115	CAA_05	116	Not Used
117	VSS	118	VSS
119	CAA_06	120	CAA_07
121	CAA_01	122	CAA_04
123	VSS	124	VSS
125	CAA_03	126	CAA_00

197	DQ35	198	VSS
199	VSS	200	DQ44
201	DQ40	202	DQ45
203	DQ41	204	VSS
205	VSS	206	DQS5_c
207	DM5/DBI5	208	DQS5_t
209	VSS	210	VSS
211	DQ42	212	DQ46
213	DQ43	214	DQ47
215	VSS	216	VSS
217	DQ48	218	DQ52
219	DQ49	220	DQ53
221	VSS	222	VSS
223	DQS6_c	224	DM6/DBI6
225	DQS6_t	226	VSS
227	VSS	228	DQ54
229	DQ50	230	DQ55
231	DQ51	232	VSS
233	VSS	234	DQ60
235	DQ56	236	DQ61
237	DQ57	238	VSS
239	VSS	240	DQS7_c
241	DM7/DBI7	242	DQS7_t
243	VSS	244	VSS
245	DQ58	246	DQ62
247	DQ59	248	DQ63
249	VSS	250	VSS
251	SCL	252	SDA
253	VDD_SPD	254	SA0
255	SA2	256	SA1
257	VPP	258	VTT
259	VPP	260	VTT

FIG. 8C (CONT.)

LPDDR4 Mode Pinout (260-pin connector) 830

Pin #	Front side	Pin #	Back side
1	RSVD	2	RSVD
3	RSVD	4	RSVD
5	VSS	6	VSS
7	DQ0	8	DQ4
9	DQ1	10	DQ5
11	VSS	12	VSS
13	DQS0_c	14	DM0/DBI0
15	DQS0_t	16	VSS
17	VSS	18	DQ6
19	DQ2	20	DQ7
21	DQ3	22	VSS
23	VSS	24	DQ12
25	DQ8	26	DQ13
27	DQ9	28	VSS
29	VSS	30	DQS1_c
31	DM1/DBI1	32	DQS1_t
33	VSS	34	VSS
35	DQ10	36	DQ14
37	DQ11	38	DQ15
39	VSS	40	VSS
41	DQ16	42	DQ20
43	DQ17	44	DQ21
45	VSS	46	VSS
47	DQS2_c	48	DM2/DBI2
49	DQS2_t	50	VSS
51	VSS	52	DQ22
53	DQ18	54	DQ23
55	DQ19	56	VSS
57	VSS	5	DQ28
59	DQ24	60	DQ29
61	DQ25	62	VSS
63	VSS	64	DQS3_c
65	DM3/DBI3	66	DQS3_t
67	VSS	68	VSS
69	DQ26	70	DQ30

Pin #	Front side	Pin #	Back side
127	CAA_02	128	Not Used
129	VSS	130	VSS
131	Not Used	132	CAB_05
133	Not Used	134	EVENT_n
135	VSS	136	VSS
137	CLKA_t	138	CLKB_t
139	CLKA_c	140	CLKB_c
141	VSS	142	VSS
143	Not Used	144	Not Used
145	Not Used	146	Not Used
147	VSS	148	VSS
149	RFU	150	CAB_04
151	CAB_02	52	CAB_03
153	VSS	154	VSS
155	RFU	156	CAB_00
157	CSA0	158	CAB_01
159	VSS	160	VSS
161	CSA2	162	CSB1
163	CSA1	164	CSB2
165	VSS	166	VSS
167	CSB0	168	VREF_CA
169	VSS	170	VSS
171	VDD	172	VDD
173	VDD	174	VDD
175	VDD	176	VDD
177	VDD	178	VDD
179	VDD	180	VDD
181	VSS	182	VSS
183	DQ32	184	DQ36
185	DQ33	186	DQ37
187	VSS	188	VSS
189	DQS4_c	190	DM4/DBI4
191	DQS4_t	192	VSS
193	VSS	194	DQ38
195	DQ34	196	DQ39

FIG. 8D

71	DQ27	72	DQ31
73	VSS	74	VSS
75	Not Used	76	Not Used
77	Not Used	78	Not Used
79	VSS	80	VSS
81	Not Used	82	Not Used
83	Not Used	84	VSS
85	VSS	86	Not Used
87	Not Used	88	Not Used
89	Not Used	90	VSS
91	VSS	92	VREF_DQ
93	VDD	94	VDD
95	VDD	96	VDD
97	VDD	98	VDD
99	VDD	100	VDD
101	VSS	102	RESET_n
Key		Key	
103	CKEA0	104	CKEA1
105	VSS	106	VSS
107	CKEB0	108	CKEB1
109	CKEA2	110	CKEB2
111	VSS	112	VSS
113	Not Used	114	Not Used
115	CAA_05	116	Not Used
117	VSS	118	VSS
119	Not Used	120	Not Used
121	CAA_01	122	CAA_04
123	VSS	124	VSS
125	CAA_03	126	CAA_00

197	DQ35	198	VSS
199	VSS	200	DQ44
201	DQ40	202	DQ45
203	DQ41	204	VSS
205	VSS	206	DQS5_c
207	DM5/DBI5	208	DQS5_t
209	VSS	210	VSS
211	DQ42	212	DQ46
213	DQ43	214	DQ47
215	VSS	216	VSS
217	DQ48	218	DQ52
219	DQ49	220	DQ53
221	VSS	222	VSS
223	DQS6_c	224	DM6/DBI6
225	DQS6_t	226	VSS
227	VSS	228	DQ54
229	DQ50	230	DQ55
231	DQ51	232	VSS
233	VSS	234	DQ60
235	DQ56	236	DQ61
237	DQ57	238	VSS
239	VSS	240	DQS7_c
241	DM7/DBI7	242	DQS7_t
243	VSS	244	VSS
245	DQ58	246	DQ62
247	DQ59	248	DQ63
249	VSS	250	VSS
251	SCL	252	SDA
253	VDD_SPD	254	SA0
255	SA2	256	SA1
257	VPP	258	VTT
259	VPP	260	VTT

FIG. 8D (CONT.)

DDR4 Mode Pinout (242-pin connector) 900

Pin #	Front side	Pin #	Back side
1	RSVD	2	RSVD
3	RSVD	4	RSVD
5	VSS	6	VSS
7	DQ0	8	DQ4
9	DQ1	10	DQ5
11	VSS	12	VSS
13	DQS0_c	14	DM0/DBI0
15	DQS0_t	16	VSS
17	VSS	18	DQ6
19	DQ2	20	DQ7
21	DQ3	22	VSS
23	VSS	24	DQ12
25	DQ8	26	DQ13
27	DQ9	28	VSS
29	VSS	30	DQS1_c
31	DM1/DBI1	32	DQS1_t
33	VSS	34	VSS
35	DQ10	36	DQ14
37	DQ11	38	DQ15
39	VSS	40	VSS
41	DQ16	42	DQ20
43	DQ17	44	DQ21
45	VSS	46	VSS
47	DQS2_c	48	DM2/DBI2
49	DQS2_t	50	VSS
51	VSS	52	DQ22
53	DQ18	54	DQ23
55	DQ19	56	VSS
57	VSS	5	DQ28
59	DQ24	60	DQ29
61	DQ25	62	VSS
63	VSS	64	DQS3_c
65	DM3/DBI3	66	DQS3_t
67	VSS	68	VSS
69	DQ26	70	DQ30

Pin #	Front side	Pin #	Back side
119	VSS	120	VSS
121	CLK0_t	122	CLK1_t
123	CLK0_c	124	CLK1_c
125	VSS	126	VSS
127	PARITY	128	A0
129	BA1	130	A10/AP
131	VSS	132	VSS
133	RFU	134	BA0
135	A14/WE_n	136	A16/RAS_n
137	VSS	138	VSS
139	RFU	140	A13
141	ALERT_n	142	A15/CAS_n
143	VSS	144	VSS
145	CS0_n	146	CS1_n
147	ODT0	148	ODT1
149	VSS	150	VSS
151	Not Used	52	Not Used
153	Not Used	154	Not Used
155	VSS	156	VSS
157	RFU	158	VREF_CA
159	VDD	160	VDD
161	VDD	162	VDD
163	VDD	164	VDD
165	VSS	166	VSS
167	DQ32	168	DQ36
169	DQ33	170	DQ37
171	VSS	172	VSS
173	DQS4_c	174	DM4/DBI4
175	DQS4_t	176	VSS
177	VSS	178	DQ38
179	DQ34	180	DQ39
181	DQ35	182	VSS
183	VSS	184	DQ44
185	DQ40	186	DQ45
187	DQ41	188	VSS

FIG. 9A

71	DQ27	72	DQ31
73	VSS	74	VSS
Key		Key	
75	VDD	76	VDD
77	VDD	78	VDD
79	VDD	80	VDD
81	RFU	82	Not Used
83	VSS	84	VSS
85	CKE0	86	CKE1
87	CKE2	88	CKE3
89	VSS	90	VSS
91	Not Used	92	Not Used
93	Not Used	94	Not Used
95	VSS	96	VSS
97	BG1	98	RESET_n
99	BG0	100	ACT_n
101	VSS	102	VSS
103	A12	104	A11
105	A9	106	A7
107	VSS	108	VSS
109	A8	110	A5
111	A6	112	A4
113	VSS	114	VSS
115	A3	116	A2
117	A1	118	EVENT_n

189	VSS	190	DQS5_c
191	DM4/DBI5	192	DQS5_t
193	VSS	194	VSS
195	DQ42	196	DQ46
197	DQ43	198	DQ47
199	VSS	200	VSS
201	DQ48	202	DQ52
203	DQ49	204	DQ53
205	VSS	206	VSS
207	DQS6_c	208	DM6/DBI6
209	DQS6_t	210	VSS
211	VSS	212	DQ54
213	DQ50	214	DQ55
215	DQ51	216	VSS
217	VSS	218	DQ60
219	DQ56	220	DQ61
221	DQ57	222	VSS
223	VSS	224	DQS7_c
225	DM7/DBI7	226	DQS7_t
227	VSS	228	VSS
229	DQ58	230	DQ62
231	DQ59	232	DQ63
233	VSS	234	VSS
235	SCL	236	SDA
237	VDD_SPD	238	SA0
239	VPP	240	SA1
241	VPP	242	VTT

FIG. 9A (CONT.)

LPDDR3 Mode Pinout (242-pin connector) 910

Pin #	Front side	Pin #	Back side
1	RSVD	2	RSVD
3	RSVD	4	RSVD
5	VSS	6	VSS
7	DQ0	8	DQ4
9	DQ1	10	DQ5
11	VSS	12	VSS
13	DQS0_c	14	DM0/DBI0
15	DQS0_t	16	VSS
17	VSS	18	DQ6
19	DQ2	20	DQ7
21	DQ3	22	VSS
23	VSS	24	DQ12
25	DQ8	26	DQ13
27	DQ9	28	VSS
29	VSS	30	DQS1_c
31	DM1/DBI1	32	DQS1_t
33	VSS	34	VSS
35	DQ10	36	DQ14
37	DQ11	38	DQ15
39	VSS	40	VSS
41	DQ16	42	DQ20
43	DQ17	44	DQ21
45	VSS	46	VSS
47	DQS2_c	48	DM2/DBI2
49	DQS2_t	50	VSS
51	VSS	52	DQ22
53	DQ18	54	DQ23
55	DQ19	56	VSS
57	VSS	5	DQ28
59	DQ24	60	DQ29
61	DQ25	62	VSS
63	VSS	64	DQS3_c
65	DM3/DBI3	66	DQS3_t
67	VSS	68	VSS
69	DQ26	70	DQ30

Pin #	Front side	Pin #	Back side
119	VSS	120	VSS
121	CLK0_t	122	CLK1_t
123	CLK0_c	124	CLK1_c
125	VSS	126	VSS
127	Not Used	128	CAB_09
129	CAB_06	130	CAB_07
131	VSS	132	VSS
133	RFU	134	CAB_04
135	CAB_02	136	CAB_03
137	VSS	138	VSS
139	RFU	140	CAB_00
141	Not Used	142	CAB_01
143	VSS	144	VSS
145	CS0_n	146	CS1_n
147	ODT0	148	Not Used
149	VSS	150	VSS
151	Not Used	52	Not Used
153	Not Used	154	Not Used
155	VSS	156	VSS
157	RFU	158	VREF_CA
159	VDD	160	VDD
161	VDD	162	VDD
163	VDD	164	VDD
165	VSS	166	VSS
167	DQ32	168	DQ36
169	DQ33	170	DQ37
171	VSS	172	VSS
173	DQS4_c	174	DM4/DBI4
175	DQS4_t	176	VSS
177	VSS	178	DQ38
179	DQ34	180	DQ39
181	DQ35	182	VSS
183	VSS	184	DQ44
185	DQ40	186	DQ45
187	DQ41	188	VSS

FIG. 9B

71	DQ27	72	DQ31
73	VSS	74	VSS
Key		Key	
75	VDD	76	VDD
77	VDD	78	VDD
79	VDD	80	VDD
81	RFU	82	VREF_DQ
83	VSS	84	VSS
85	CKEA0	86	CKEA1
87	CKEB2	88	CKEB3
89	VSS	90	VSS
91	Not Used	92	Not Used
93	Not Used	94	Not Used
95	VSS	96	VSS
97	CAA_09	98	RESET_n
99	CAA_05	100	CAA_08
101	VSS	102	VSS
103	CAA_06	104	CAA_07
105	CAA_01	106	CAA_04
107	VSS	108	VSS
109	CAA_03	110	CAA_00
111	CAA_02	112	Not Used
113	VSS	114	VSS
115	Not Used	116	CAB_05
117	CAB_08	118	EVENT_n

189	VSS	190	DQS5_c
191	DM4/DBI5	192	DQS5_t
193	VSS	194	VSS
195	DQ42	196	DQ46
197	DQ43	198	DQ47
199	VSS	200	VSS
201	DQ48	202	DQ52
203	DQ49	204	DQ53
205	VSS	206	VSS
207	DQS6_c	208	DM6/DBI6
209	DQS6_t	210	VSS
211	VSS	212	DQ54
213	DQ50	214	DQ55
215	DQ51	216	VSS
217	VSS	218	DQ60
219	DQ56	220	DQ61
221	DQ57	222	VSS
223	VSS	224	DQS7_c
225	DM7/DBI7	226	DQS7_t
227	VSS	228	VSS
229	DQ58	230	DQ62
231	DQ59	232	DQ63
233	VSS	234	VSS
235	SCL	236	SDA
237	VDD_SPD	238	SA0
239	VPP	240	SA1
241	VPP	242	VTT

FIG. 9B (CONT.)

LPDDR4 Mode Pinout (242-pin connector) 920

Pin #	Front side	Pin #	Back side
1	RSVD	2	RSVD
3	RSVD	4	RSVD
5	VSS	6	VSS
7	DQ0	8	DQ4
9	DQ1	10	DQ5
11	VSS	12	VSS
13	DQS0_c	14	DM0/DBI0
15	DQS0_t	16	VSS
17	VSS	18	DQ6
19	DQ2	20	DQ7
21	DQ3	22	VSS
23	VSS	24	DQ12
25	DQ8	26	DQ13
27	DQ9	28	VSS
29	VSS	30	DQS1_c
31	DM1/DBI1	32	DQS1_t
33	VSS	34	VSS
35	DQ10	36	DQ14
37	DQ11	38	DQ15
39	VSS	40	VSS
41	DQ16	42	DQ20
43	DQ17	44	DQ21
45	VSS	46	VSS
47	DQS2_c	48	DM2/DBI2
49	DQS2_t	50	VSS
51	VSS	52	DQ22
53	DQ18	54	DQ23
55	DQ19	56	VSS
57	VSS	5	DQ28
59	DQ24	60	DQ29
61	DQ25	62	VSS
63	VSS	64	DQS3_c
65	DM3/DBI3	66	DQS3_t
67	VSS	68	VSS
69	DQ26	70	DQ30

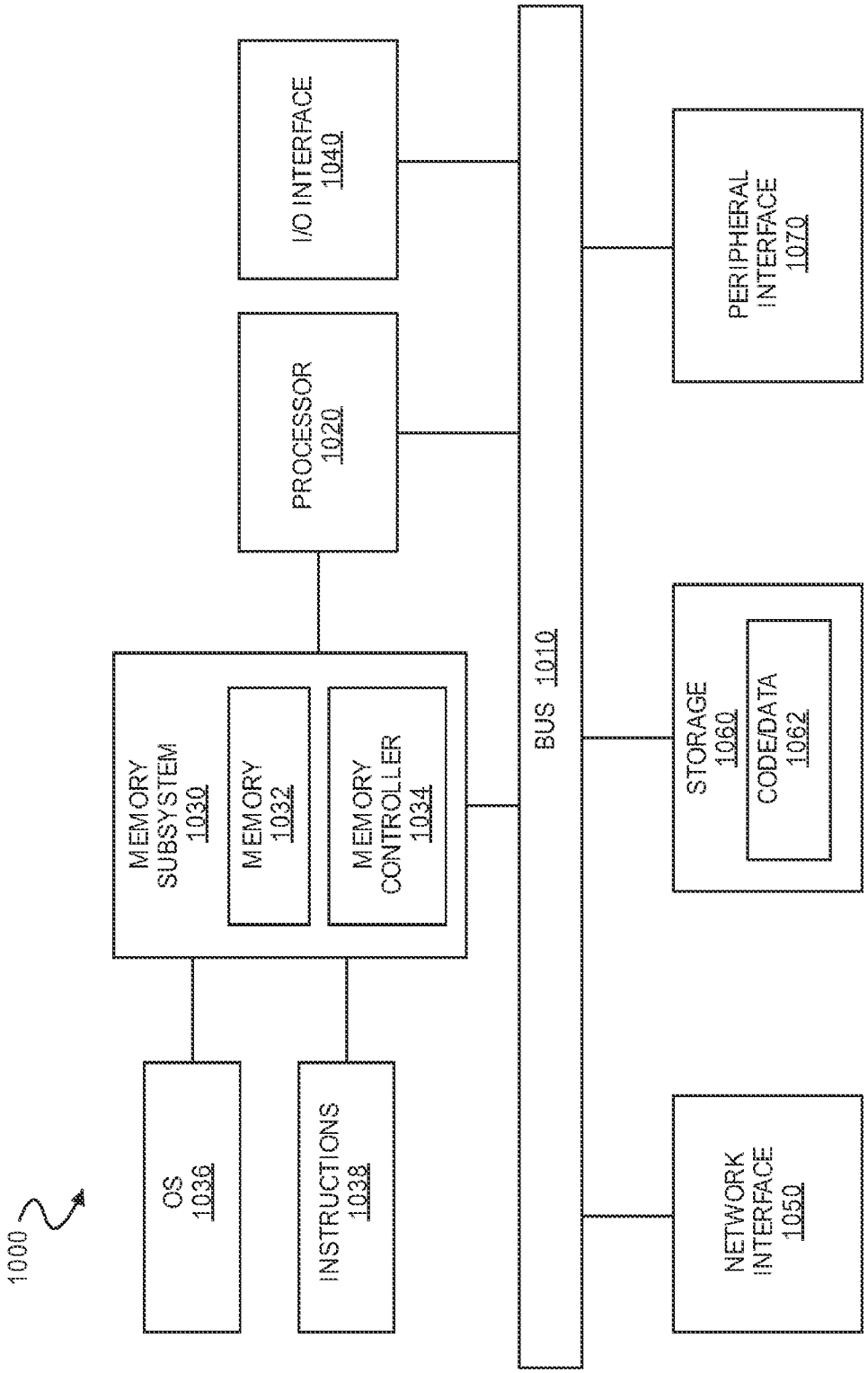
Pin #	Front side	Pin #	Back side
119	VSS	120	VSS
121	CLK0_t	122	CLKB_t
123	CLK0_c	124	CLKB_c
125	VSS	126	VSS
127	Not Used	128	Not Used
129	CAB_06	130	Not Used
131	VSS	132	VSS
133	RFU	134	CAB_04
135	CAB_02	136	CAB_03
137	VSS	138	VSS
139	RFU	140	CAB_00
141	Not Used	142	CAB_01
143	VSS	144	VSS
145	CSA0	146	CSB0
147	CSA1	148	CSB1
149	VSS	150	VSS
151	Not Used	52	Not Used
153	Not Used	154	Not Used
155	VSS	156	VSS
157	RFU	158	Not Used
159	VDD	160	VDD
161	VDD	162	VDD
163	VDD	164	VDD
165	VSS	166	VSS
167	DQ32	168	DQ36
169	DQ33	170	DQ37
171	VSS	172	VSS
173	DQS4_c	174	DM4/DBI4
175	DQS4_t	176	VSS
177	VSS	178	DQ38
179	DQ34	180	DQ39
181	DQ35	182	VSS
183	VSS	184	DQ44
185	DQ40	186	DQ45
187	DQ41	188	VSS

FIG. 9C

71	DQ27	72	DQ31
73	VSS	74	VSS
Key		Key	
75	VDD	76	VDD
77	VDD	78	VDD
79	VDD	80	VDD
81	RFU	82	Not Used
83	VSS	84	VSS
85	CKEA0	86	CKEA1
87	CKEB0	88	CKEB1
89	VSS	90	VSS
91	Not Used	92	Not Used
93	Not Used	94	Not Used
95	VSS	96	VSS
97	Not Used	98	RESET_n
99	CAA_05	100	Not Used
101	VSS	102	VSS
103	Not Used	104	Not Used
105	CAA_01	106	CAA_04
107	VSS	108	VSS
109	CAA_03	110	CAA_00
111	CAA_02	112	Not Used
113	VSS	114	VSS
115	Not Used	116	CAB_05
117	Not Used	118	EVENT_n

189	VSS	190	DQS5_c
191	DM4/DBI5	192	DQS5_t
193	VSS	194	VSS
195	DQ42	196	DQ46
197	DQ43	198	DQ47
199	VSS	200	VSS
201	DQ48	202	DQ52
203	DQ49	204	DQ53
205	VSS	206	VSS
207	DQS6_c	208	DM6/DBI6
209	DQS6_t	210	VSS
211	VSS	212	DQ54
213	DQ50	214	DQ55
215	DQ51	216	VSS
217	VSS	218	DQ60
219	DQ56	220	DQ61
221	DQ57	222	VSS
223	VSS	224	DQS7_c
225	DM7/DBI7	226	DQS7_t
227	VSS	228	VSS
229	DQ58	230	DQ62
231	DQ59	232	DQ63
233	VSS	234	VSS
235	SCL	236	SDA
237	VDD_SPD	238	SA0
239	VPP	240	SA1
241	VPP	242	VTT

FIG. 9C (CONT.)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OS 1036
INSTRUCTIONS 1038
MEMORY SUBSYSTEM 1030
MEMORY 1032
MEMORY CONTROLLER 1034
PROCESSOR 1020
I/O INTERFACE 1040
BUS 1010
STORAGE 1060
CODE/DATA 1062
PERIPHERAL INTERFACE 1070
NETWORK INTERFACE 1050

FIG. 10

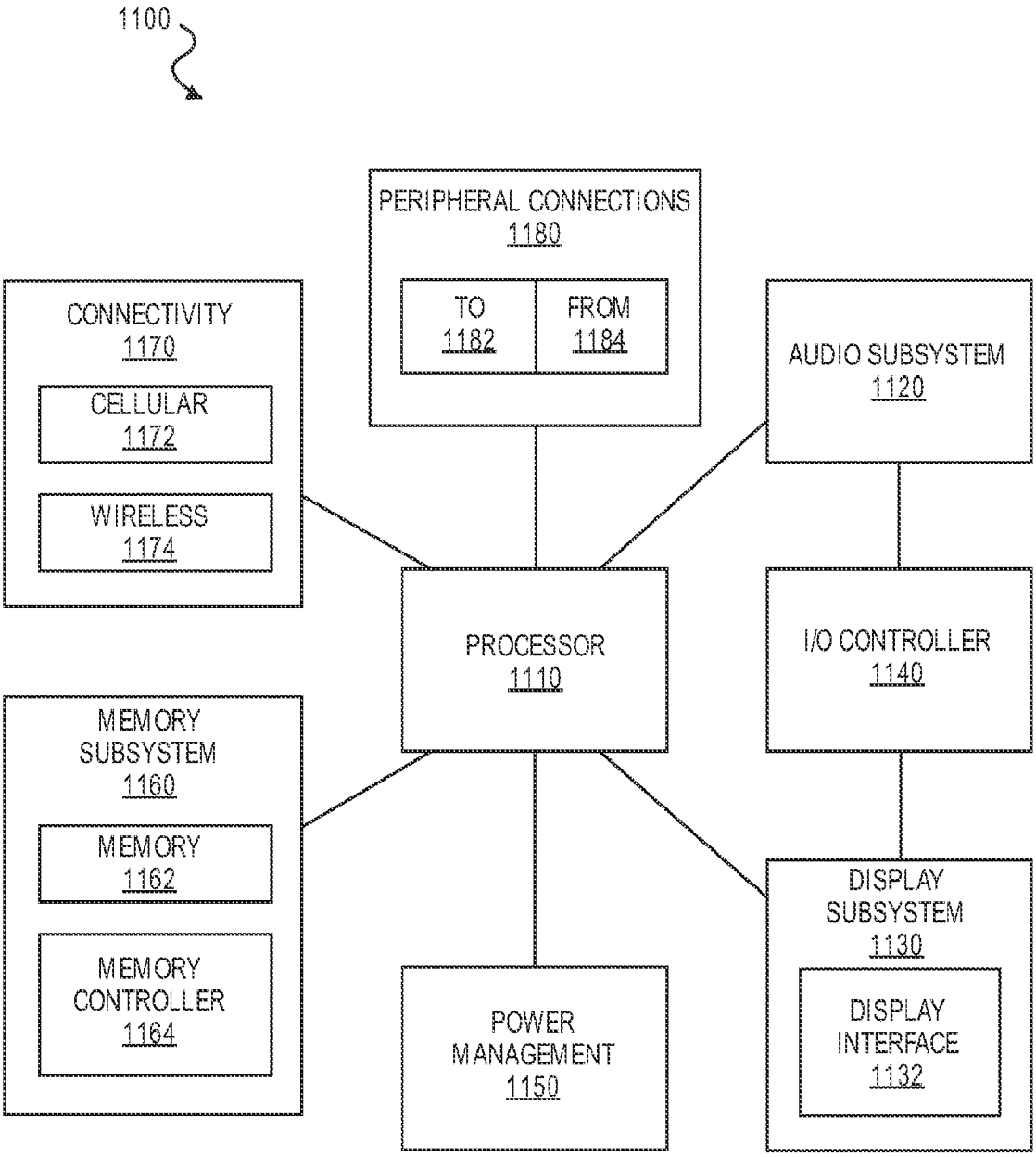
1100
PERIPHERAL CONNECTIONS
1180
TO
1182
FROM
1184
CONNECTIVITY
1170
CELLULAR
1172
WIRELESS
1174
AUDIO SUBSYSTEM
1120
PROCESSOR
1110
I/O CONTROLLER
1140
MEMORY
SUBSYSTEM
1160
MEMORY
1162
MEMORY
CONTROLLER
1164
POWER
MANAGEMENT
1150
DISPLAY
SUBSYSTEM
1130
DISPLAY
INTERFACE
1132

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/012279

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/16(2006.01)i, G06F 13/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 1/16; G11C 5/06; G11C 7/00; G06F 12/00; H05K 7/00; G06F 12/08; G06F 13/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: computer platform, any of memory devices, processor, voltage regulator, interconnect, detector logic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002-0144074 A1 (CHUNG-CHE WU et al.) 03 October 2002 See paragraphs [0014]-[0015], [0018]; claims 1-8; and figures 1, 3.	1-21
Y	US 2008-0259553 A1 (SHOU-KUO HSU et al.) 23 October 2008 See paragraphs [0011]-[0016].	1-21
A	US 2013-0054872 A1 (FRED CHARLES THOMAS, III et al.) 28 February 2013 See paragraphs [0010]-[0021], [0032]-[0034]; and figures 1, 4.	1-21
A	US 2013-0083585 A1 (JOE M. JEDDELOH) 04 April 2013 See paragraphs [0017]-[0023]; and figure 3.	1-21
A	US 7327612 B2 (REZA M. BACCHUS et al.) 05 February 2008 See column 2, line 34 - column 3, line 61; and figures 1-2.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 April 2015 (10.04.2015)	**13 April 2015 (13.04.2015)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/012279

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