(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 May 2006 (18.05.2006)

PCT

(10) International Publication Number
WO 2006/053257 A1

(51) International Patent Classification:
H01L 27/082 (2006.01) *H01L 21/331* (2006.01)

(21) International Application Number:
PCT/US2005/041049

(22) International Filing Date:
10 November 2005 (10.11.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/904,437 10 November 2004 (10.11.2004) US

(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **KHATER, Marwan, H.** [JO/US]; 606 Hudson Harbor Drive, Poughkeepsie, NY 12601 (US). **PAGETTE, Francois** [CA/US]; 1508 Max Way, Fishkill, NY 12524 (US).

(74) Agent: **ANDERSON, Jay, H.**; IBM Corporation, Dept. 18G, Bldg. 321/482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

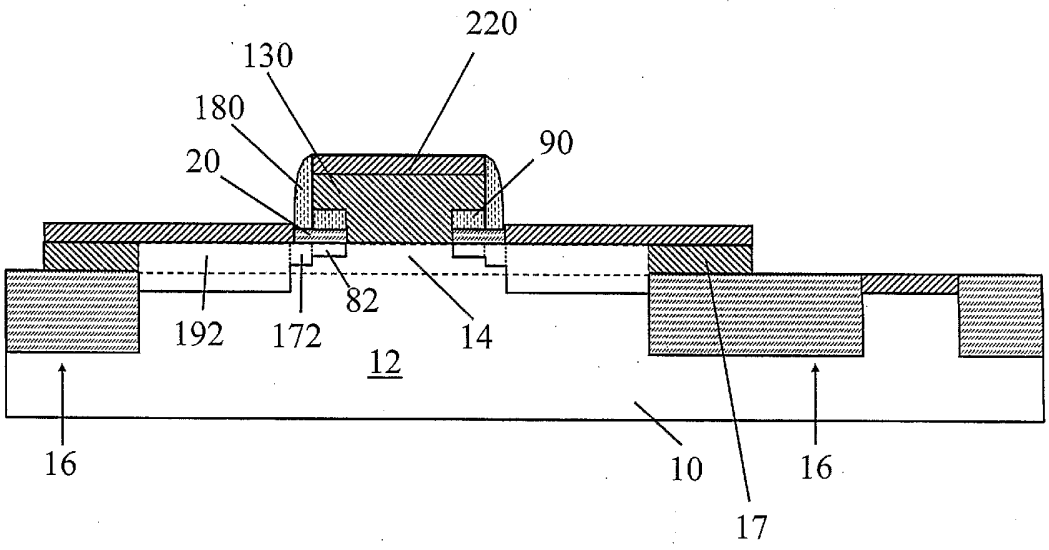
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** BIPOLAR TRANSISTOR WITH SELFALIGNED SILICIDE AND EXTRINSIC BASE



(57) **Abstract:** Disclosed is a bipolar transistor and a method of forming the transistor, where the transistor includes a collector (12) in a substrate (10), an intrinsic base (14) above the collector, an extrinsic base adjacent the intrinsic base, and an emitter (130) above the intrinsic base. The extrinsic base includes extrinsic base implant regions (82, 172, 192) adjacent the intrinsic base, when viewed in cross-section. The transistor is formed by patterning an emitter pedestal (50) for the lower portion of the emitter on the substrate above the intrinsic base. The extrinsic base is formed in regions not protected by the emitter pedestal. Subsequently, the emitter, associated spacers (180) and a silicide region (220) are formed. The silicide, extrinsic base and emitter are all self-aligned with each other.

WO 2006/053257 A1

BIPOLAR TRANSISTOR WITH SELFALIGNED SILICIDE AND EXTRINSIC BASE

Technical Field

This invention relates to self-aligned bipolar transistor (BT) for which the extrinsic base implant, extrinsic base silicide, and the emitter are self-aligned to one another.

Background Art

It has been shown that introducing a SiGe epitaxial layer to serve as the base of a bipolar transistor allows the bipolar transistor to achieve high switching speeds. By reducing the parasitic base resistance and capacitance, one can take advantage of the speed increase to further increase in the maximum oscillation frequency (fmax). One easy approach to accomplish this goal is to reduce the lateral dimensions of the transistor. Aligning one part of the transistor to another is traditionally done by lithography. In designing such a structure one must consider the alignment and critical dimension tolerance associated with the lithography processes. Integration schemes that make use of self-alignment instead of lithography, where of one part of the transistor is used to align another feature of the transistor, have proven to be efficient in reducing the lateral dimensions and increasing transistor performance.

For a conventional bipolar transistor, the extrinsic base layer is implanted after the patterning of the emitter polysilicon layer. These conventional patterning processes still rely on lithography to align the emitter polysilicon layer pattern to the emitter opening and the subsequent contact. The emitter polysilicon layer pattern is typically large enough to allow for tolerance in the lithographic processes for the emitter contact. Therefore, for this type of integration scheme, the extrinsic base implant and silicide are non-self aligned and are spaced far away from the emitter base junction, which results in high base resistance. The maximum oscillation frequency of such a non-self aligned transistor is limited by a base resistance (Rb) caused by such spacing.

The below-referenced U.S. patents disclose embodiments that were satisfactory for the purposes for which they were intended. The disclosures of the below-referenced prior U.S.

patents, in their entireties, are hereby expressly incorporated by reference into the present invention for purposes including, but not limited to, indicating the background of the present invention and illustrating the state of the art.

For example, in US Patent 6,534,372, the extrinsic base is delimitated by a permanent spacer formed around a temporary emitter pedestal or by the temporary emitter pedestal itself. The temporary pedestal is later removed by lithography and etching to be replaced by a polysilicon emitter. The permanent spacer must then be of sufficient width for the second lithographic pattern edge with its associated critical dimensions (CD) and alignment tolerance to be formed on top of the spacer. In addition, the spacer width has to be sufficient to provide emitter-base isolation. This adds a structural constraint on the emitter dimension and minimum distance between the heavy doped extrinsic base area and the emitter-base junction. Also, the emitter polysilicon layer and the extrinsic base silicide are defined by lithography which adds to the lateral dimension and base resistance.

In US Patent Application 6,531,720, the lateral profile of the extrinsic base doping is determined by a dual spacer formed around a temporary emitter pedestal. The emitter polysilicon layer and the extrinsic base silicide are defined by lithography which adds to the lateral dimension and the base resistance. Another drawback of this integration scheme is that the temporary pedestal lays on top of a thick stack of oxide nitride and polysilicon layers. In this case, the stack is needed to later form the emitter-base isolation and, consequently, the dopant implantation through such a thick stack have to be of high energy to achieve low base resistance in the extrinsic base region. This results in less control over the doping profile and loss of intrinsic base region due to dopant diffusion.

Disclosure of Invention

The invention presents a method of forming a transistor in an integrated circuit structure that begins by forming a collector in a substrate and then forming an intrinsic base above the collector. The invention patterns an alignment layer over the substrate to have an alignment opening and then patterns an emitter pedestal (sacrificial placeholder) on the substrate in the alignment opening. Then, the invention can perform a first implant to form first extrinsic base portions in regions of the substrate not protected by the emitter pedestal and the alignment layer. Next, the invention removes the emitter pedestal and forms an

emitter in the alignment opening, which is self-aligned to the first extrinsic base implant. After removing the alignment layer, the invention performs a second implant to form second extrinsic base portions in regions of the substrate not protected by the emitter. Then, sidewall spacer is formed on the emitter and a third implant is performed to form third extrinsic base portions in regions of the substrate not protected by the emitter and the sidewall spacer.

Similarly, the process of forming the emitter comprises depositing an emitter material conformally within the alignment opening. The thickness of the emitter material within the alignment opening determines the width of the emitter. This conformal deposition process again leaves a recess in the emitter material where the alignment opening is positioned. As was done with the emitter pedestal, a mask is formed within the recess the emitter material not protected by the mask is removed.

In another embodiment, the invention forms a collector in a substrate and an intrinsic base above the collector. Then, the invention patterns an emitter pedestal for the lower portion of the emitter on the substrate above the intrinsic base. Before actually forming the emitter or associated spacers, the invention forms an extrinsic base in regions of the substrate not protected by the emitter pedestal. After this, the invention removes the emitter pedestal and eventually forms the emitter where the emitter pedestal was positioned.

This embodiment provides a process of forming the extrinsic base that first performs a first impurity implant into the regions of the substrate not protected by the emitter pedestal, without any spacers present. This allows the sides of the extrinsic base regions to be directly vertically below and directly vertically aligned with sides of the lower portion of the emitter. After this first implant, the invention then forms first sidewall spacer on the emitter pedestal and performs a second impurity implant into regions of the substrate not protected by the emitter pedestal or the first sidewall spacer. The invention then removes the first sidewall spacer and repeats the implant process with a wider sidewall spacer. Therefore, the invention forms second sidewall spacer on the emitter pedestal. These second sidewall spacers extend further from the emitter pedestal than did the first sidewall spacer. Then, the invention performs a third impurity implant into regions of the substrate not protected by the emitter pedestal or the second sidewall spacer.

This processing causes the extrinsic base to include multiple steps adjacent the sides of the emitter when viewed in cross-section. These steps comprise lengths of the extrinsic base

that extend different depths into the substrate, wherein each successive length of the extrinsic base away from the emitter and the intrinsic base extend further into the substrate. Also, the thickness of the first sidewall spacer and the second sidewall spacer is independent of the thickness of the isolation regions that will be formed adjacent the lower portion of the emitter later.

Before the invention removes the emitter pedestal, it forms an alignment layer adjacent the emitter pedestal. When the emitter pedestal is removed, this leaves an emitter opening in the alignment layer. Then, the subsequent processing forms the emitter in the emitter openings of the alignment layer. Also, the invention forms an etch stop layer on the substrate and the thickness of the etch stop layer is controlled to reduce the energy required for the process of forming the extrinsic base regions.

The resulting structure has a collector and intrinsic base in the substrate, extrinsic base regions in the substrate adjacent the intrinsic base, and an emitter above the intrinsic base. The emitter has a T-shape where the upper portion is wider than the lower portion. The sides of the extrinsic base regions can be directly vertically below and directly vertically aligned with the sides of a lower portion of the emitter that is directly above the intrinsic base, or can be positioned below the emitter. These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

Brief Description of the Drawings

The invention will be better understood from the following detailed description with reference to the drawings, in which:

Figure 1 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 2 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 3 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 4 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 5 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 6 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 7 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 8 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 9 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 10 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 11 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 12 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 13 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 14 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 15 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 16 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 17 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 18 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 19 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 20 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 21 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 22 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 23 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 24 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 25 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 26 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 27 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 28 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 29 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 30 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 31 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 32 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 33 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 34 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 35 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 36 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 37 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 38 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 39 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 40 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 41 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 42 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 43 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 44 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 45 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 46 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 47 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 48 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 49 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 50 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 51 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 52 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 53 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 54 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 55 is a schematic diagram of a partially completed bipolar transistor according to the invention;

Figure 56 is a schematic diagram of a partially completed bipolar transistor according to the invention; and

Figure 57 is a schematic diagram of a partially completed bipolar transistor according to the invention.

Best Mode for Carrying Out the Invention

The present invention and the various features and advantageous details thereof are explained more fully with reference to the nonlimiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of

skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

The various solutions toward improving bipolar transistors that are discussed in the background section leave room for improvement in bipolar transistors in a number areas. For example, there is a need for 1) the extrinsic base implant to be self-aligned to the emitter opening; 2) the extrinsic base silicide to be self-aligned to the emitter opening; 3) the emitter polysilicon pattern to be self-aligned to the emitter opening; 4) the dopant profile to be formed in proximity of the emitter-base junction to optimize the base resistance and emitter-base leakage current; and 5) the extension base implant to be performed through only a thin oxide layer.

This disclosure describes a self-aligned transistor with an implanted extrinsic base that addresses the points mentioned above. More specifically, as shown in the embodiment in Figures 1-22, the invention forms a transistor in an integrated circuit structure that begins by forming a collector 12 in a substrate 10 and an intrinsic base 14 above the collector 12. Regions 18 are shallow trench isolation (STI) of the substrate 10 that separate the transistor from other structures. In this example, regions 16 comprise, for example, doped polysilicon 17 and various deposited oxides 18, 19. The methodologies and materials that can be used to form these structures are well known to those of ordinarily skilled in the art as explained in, for example, US Patent 6,534,372, mentioned above.

As shown in Figure 2, the invention forms a thin (10-20 nm) etch stop layer 20 (such as a deposited oxide), a nitride layer 26, and an alignment layer 22 which can comprise any suitable material, such as undoped polysilicon, etc. The thickness of the etch stop layer 20 is controlled to reduce the energy required for the process of forming the extrinsic base regions 82, 172, 192 that are discussed below. Another deposited oxide layer 24 is formed over the alignment layer 22 in the structure in Figure 2.

Next, as shown in Figure 3, a photoresist 30 is patterned over the oxide layer 24 and, as shown in Figure 4, a material removal process (such as etching) is used to pattern the oxide layer 24, the alignment layer 22, and the nitride layer 26 stopping on the etch stop layer 20. This process forms an alignment opening 40.

In Figure 5, a sacrificial material 50, such as undoped polysilicon, is conformally deposited over the oxide layer and within the alignment opening 40. This sacrificial material

50 will eventually become the emitter pedestal that is used to align the implants and the emitter. This conformal deposition process forms a second opening 52 in the first opening 40. Then, as shown in Figure 6, a mask material 60 (such as nitride) is deposited into the second opening 52. As shown in Figure 7, the mask material 60 is used to pattern the sacrificial material 50 into the emitter pedestal structure 50. Again, any conventional material removal process, such as etching, etc., can be used to pattern the sacrificial material 50. With the mask 60 in place above the sacrificial material 50, the first of a series of extrinsic base implant impurity doping processes is performed as indicated by arrows 80 in Figure 8. This process forms the first section of the extrinsic base 82.

In Figure 9, additional nitride 90 is deposited and is selectively removed down to a level equal to nitride layer 26 (as shown in Figure 10) using any selective material removal process that is designed to only attack the nitride 90 and leave the remaining structures substantially intact. The remaining thickness of nitride 90 will serve as an isolation dielectric between the emitter and the base. In Figure 11, the emitter pedestal 50 is removed and in Figure 12 both oxide 24 and oxide layer 20 are removed (again using selective removal processes).

Then, in Figure 13, the emitter material 130 (such as doped polysilicon, or any other conductive material) is deposited in a conformal deposition process that produces a third opening 132 in a similar manner to second opening 52, as described above. In a similar manner to the previous processing, a mask material 140 such as a deposited oxide or other masking material is formed within the third opening 132 (as shown in Figure 14) and then the exposed portions of the emitter material 130 and the undoped polysilicon 22 are removed using material 140 as a mask, which results in the structure shown Figure 15. In Figure 16, this material removal process is continued (or a different material removal process can be commenced) to remove the exposed portions of the nitride layer 26, 90. Again, any conventional material removal process, such as etching, can be utilized in these steps.

In Figure 17, a second impurity 170 is implanted into the exposed portions of the substrate10 to form the second portion of the extrinsic base 172. After this, spacer 180 is formed along the sidewalls of the emitter 130. The spacer 180 can comprise, for example, a nitride (or other similar material) that is deposited and then removed in a directional removal process (such as anisotropic etching) that removes the nitride from horizontal surfaces at a

faster rate than it removes the nitride material from vertical surfaces, thereby leaving the sidewall spacer 180 along the sidewalls of the emitter 130 as shown in Figure 18. Next, as shown in Figure 19, a third impurity implant 190 is performed to form the third portion of the extrinsic base implant 192.

In Figure 20, the etch stop layer 20 and the mask 140 are removed, again using any selective material removal process, such as etching. In Figure 21 the boundary of the conductor 17 is defined using conventional patterning processes (such as masking and etching). In Figure 22, a silicide region 220 is formed over the conductors 17 and the extrinsic base region 192 using well-known siliciding processes that involve applying heat in the presence of a metal, as is well known to those ordinarily skilled in this art field. Thus, the silicide regions 220 are formed without having to use alignment masks, etc., and therefore, self-aligned silicide regions or salicides 220. In other words, the silicide 220 of the extrinsic base 192 and the top of the emitter 130 is self-aligned to the extent to base 82, 172, 192 and the emitter 130. Thus, with the use of the spacers 180 and the alignment features (such as the nitride 90, the emitter pedestal 50, etc.), the silicide 220, the extrinsic base 82, 172, 192, and the emitter 130 are all self-aligned with each other and do not require the more expensive and less accurate mask-type alignment processes.

The resulting structure shown in Figure 22 has a collector 12 and intrinsic base 14 in the substrate 10, extrinsic base regions 82, 172, 192 in the substrate 10 adjacent the intrinsic base 14, an emitter 130 above the intrinsic base 14 and self-aligned silicide regions 220. The emitter 130 has a T-shape where the upper portion is wider than the lower portion. Further, the extrinsic base 82, 172, 192 includes multiple steps, when viewed in cross-section. These steps comprise lengths of the extrinsic base 82, 172, 192 that extend different depths into the substrate 10, wherein each successive length of the extrinsic base 82, 172, 192 away from intrinsic base 14 extends further into the substrate 10 from the top of the substrate 10.

The embodiment shown in Figures 23-41 produces a similar structure as the embodiment shown in Figures 1-22, using different processing techniques. The same or similar items that are discussed above with respect to the embodiment shown in Figures 1-22 are identified with the same identification character or number and a redundant discussion of such elements is avoided for brevity.

The structure shown Figure 23 is similar to the structure shown in Figure 2 except that

layers 22, 24, and 26 are replaced with layer 230 which can comprise, for example, nitride. In Figure 24, a mask 30 is formed in a similar manner as shown below in Figure 3, and in Figure 25, the same opening 40 discussed below in Figure 4 is formed. Again in Figure 26, the sacrificial material 50 is formed and the same is patterned in Figures 27-28 as discussed below with respect to Figures 6 and 7. Note that in Figure 28, the mask material 60 is removed while in Figure 7 the mask material 60 is allowed to remain. The same impurity implant 80 is made in Figure 29 as was made in Figure 8. Then, in Figure 30, the sacrificial material 50 is removed.

In Figure 31, conformal nitride (310) and undoped polysilicon (312) layers are deposited over the structure. In Figure 32, sidewall spacer 320 (such as deposited oxide) is formed in a similar sidewall spacer formation process that formed the previous sidewall spacer 180. In Figure 33, a selective removal process removes the undoped polysilicon layer 312. This removal process does not affect the regions of the undoped polysilicon 312 that are protected by the spacers 320. In Figure 34, the spacers 320 are removed and in Figure 35 the exposed portion of the nitride layer 310 is removed. Following this, the remaining undoped polysilicon 312 is removed, as shown in Figure 36, and the central exposed portion of the etch stop layer 20 is removed, again using a selective material removal processes, as shown Figure 37

In Figure 38, the emitter material 130 is deposited as was done in Figure 13, above. In a similar manner to that shown Figure 14 above, in Figure 39, the mask 140 is formed in the recess 132 of the emitter material. Next, the exposed portions of the emitter material 130 are removed, again in a selective material removal process, as shown in Figure 40. The nitride regions 310 and 230 are removed (again in a selective material removal process) resulting in the structure shown in Figure 41. The structure shown in Figure 41 is substantially similar to the structure shown in Figure 16 and processing steps similar to the those shown in Figures 17-22 are performed on the structure to complete this embodiment of the invention.

The second embodiment is shown in Figures 42-57. More specifically, as shown in Figure 42, this process begins with a structure that is somewhat similar to that shown in Figure 2 and includes the etch stop layer 20 and the sacrificial material 50 above the etch stop layer 20. The sacrificial layer 50 is patterned using standard photolithographic techniques to form an emitter pedestal 50 for the lower portion of the emitter on the substrate 10 above the

intrinsic base 14, as shown in Figure 43.

Before forming the emitter or associated spacers, the invention forms an extrinsic base 82, 172, 192 in regions of the substrate 10 not protected by the emitter pedestal 50, as shown in Figures 44-46. The invention provides a process of forming the extrinsic base 82, 172, 192 that first performs a first impurity implant 80 into the regions of the substrate 10 not protected by the emitter pedestal 50, without any spacer present, to form the initial portion of the extrinsic base 82, as shown in Figure 44. This allows the sides of the initial portion of the extrinsic base 82 to be directly vertically below and directly vertically aligned with sides of the lower portion of the emitter 130 (Figure 55) that will eventually replace the emitter pedestal 50.

After this first implant 80, the invention then forms first sidewall spacer 54 on the emitter pedestal 50 and performs a second impurity implant 170 into regions of the substrate 10 not protected by the emitter pedestal 50 or the first sidewall spacer 450, as shown Figure 45. The invention then removes the first sidewall spacer 54 and repeats the implant process with a wider sidewall spacer 460, as shown Figure 46. More specifically, the invention forms second sidewall spacer 460 on the emitter pedestal 50. The second sidewall spacer 460 extends further from the emitter pedestal 50 than did the first sidewall spacer 450. Then, the invention performs a third impurity implant 190 into regions of the substrate 10 not protected by the emitter pedestal 50 or the second sidewall spacer 460. After this, and shown Figure 47, the second sidewall spacer 460 is removed.

As shown in Figure 46, this processing causes the extrinsic base 82, 172, 192 to include multiple steps 82, 172, 192 adjacent the intrinsic base 14, when viewed in cross-section. These steps are also referred to herein as a retrograde doping profile. These steps comprise lengths of the extrinsic base 82, 172, 192 that extend different depths into the substrate 10, wherein each successive length of the extrinsic base 82, 172, 192 away from the intrinsic base 14 extend further (deeper) into the substrate 10. The intrinsic base 14 has a shape that mirrors the multiple step shape of the extrinsic base 82, 172, 192.

One of the benefits of this aspect of the invention is that the thicknesses of the first sidewall spacer 450 and the second sidewall spacer 460 are independent of the thickness of the isolation regions 20, 480 (shown in Figure 57) that will be formed adjacent the lower portion of the emitter 130 later. Therefore, unlike conventional methodologies, with the

invention the dimensions of the steps in the extrinsic base 82, 172, 192 is completely independent of the spacer or isolation regions that will be formed next to the lower portion of the emitter 130. Thus, the invention can position the edges of the extrinsic base wherever necessary to optimize the performance of the transistor, without regard to the dimensions of the isolation regions 20, 480 that will be positioned adjacent to the lower portion of the T-shaped emitter 130.

In Figures 48-53, the invention prepares a layer 480 for the emitter 130 that will be formed in Figure 55. More specifically, in Figure 48 conformal nitride 480 and oxide 482 layers are formed over the structure. In Figure 49, the oxide layer 482 is patterned to expose a portion of the nitride layer 480. Next, in Figure 50, additional nitride is added to the previous nitride layer 480 to form a thicker nitride layer 500. In Figure 51, the nitride 480, 500 is etched down to a level below the top of the emitter pedestal 50. Then, in Figure 52, the oxide layer 482 is removed. Finally, in Figure 53, the emitter pedestal 50 is removed leaving opening 530. Figure 54 illustrates an optional embodiment that forms sidewall spacer 540 on the sidewalls of layer 480. If this sidewall spacer 540 is utilized, when the emitter 130 is formed, it will be spaced from the side of the extrinsic base 82, 172, 192. In this description, the "side" of the extrinsic base is the vertical portion of region 482 that it is adjacent to the intrinsic base 14. Therefore, these optional sidewall spacer 540 can be used, when necessary, to provide additional control regarding the horizontal spacing between the side of the extrinsic base 82, 172, 192 and the sides of the lower portion of the T-shaped emitter structure 130. The various material deposition and removal processes that are discussed above are well known to those ordinarily skilled in the art and will vary depending upon which materials are used in the specific design, and a detailed discussion of the same is avoided herein for brevity.

Thus, as shown above, before the invention removes the emitter pedestal 50, it forms a layer 480 adjacent the emitter pedestal 50. When the emitter pedestal 50 is removed, this leaves an emitter opening 530 in the layer 480. Note that the position of the emitter opening 530 in the layer 480 is completely self aligned by previously formed structures and does not require any lithographic-type structures, which avoids many problems of conventional methodologies.

As shown in Figure 55, the invention forms the T-shaped emitter 130 where the emitter pedestal 50 was positioned. Once again, one ordinarily skilled in the art would

understand that the emitter 130 can be formed of many useful conductors, such as polysilicon. Next, in Figure 56, the exposed portion of layer 480 is removed, and in Figure 57, the exposed portion of the etch stop layer 20 is removed. These processing steps form isolation regions 20, 480 that isolates the emitter 130 from the extrinsic base 82, 172, 192.

In this embodiment, the sides of the extrinsic base region 82 are directly vertically below and directly horizontally aligned with the sides of a lower portion of the emitter 130 that is directly above the intrinsic base 14. Thus, the top of the intrinsic base 14 has the same width as the lower section of the emitter 130 and the extrinsic base regions 14 do not extend below the lower portion of the emitter 130.

Therefore, as shown above, in this embodiment, the lateral dimension of the transistor is reduced by maximizing the use of self-alignment. The extrinsic base 82, 172, 192 is partially implanted prior to the polysilicon emitter 130 formation to form a doping profile in proximity of the emitter-base junction. Thus, with the invention, the emitter polysilicon 130 pattern is self-aligned to the emitter opening 130 and the extrinsic base implant 82, 172, 192. Further, the temporary emitter pedestal 50 lays on the thin etch stop layer 20 which allows for low energy ion implantation, which provides better control of the extrinsic base doping profile depth and lateral diffusion. The use of the disposable pedestal 50 to form the extrinsic base 82, 172, 192 doping allows for an optimum profile that is independent of other structures of the transistor such as emitter-base isolation regions 20, 100.

Industrial Applicability

This invention is applicable to the manufacture of very-large-scale integrated circuits in which high switching speeds are desired, and particularly in the manufacture of high-performance computing devices.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

What is claimed is:

1. A bipolar transistor comprising:
a substrate (10);
a collector (12) in said substrate;
an intrinsic base (14) above said collector;
an extrinsic base adjacent said intrinsic base; and
an emitter (130) above said intrinsic base,
wherein said extrinsic base includes extrinsic base implant regions (82, 172, 192) adjacent said intrinsic base, when viewed in cross-section.

2. The bipolar transistor in claim 1, wherein the top of said intrinsic base (14) has the same width as a lower section of said emitter (130) that is directly above said intrinsic base.

3. The bipolar transistor in claim 1, wherein said extrinsic base implant regions (82, 172, 192) do not extend below a lower portion of said emitter that is directly above said intrinsic base.

4. The bipolar transistor in claim 1, wherein said extrinsic base implant regions are aligned with sides of said emitter.

5. The bipolar transistor in claim 1, wherein
said extrinsic base implant regions comprise lengths of said extrinsic base that extend different depths into said substrate, and
each successive length of said extrinsic base away from said intrinsic base extends deeper into said substrate.

6. The bipolar transistor in claim 4, further comprising isolation regions (90) adjacent a lower portion of said emitter that is directly above said intrinsic base, wherein the lengths of said extrinsic base implant regions are independent of the size of said isolation regions.

7. The bipolar transistor in claim 1, wherein

said emitter (130) comprises a lower portion and an upper portion that is wider than said lower portion, and

said sides of said emitter comprise sides of said lower portion of said emitter.

8. The bipolar transistor in claim 1, further comprising silicide regions (220) above said extrinsic base and said emitter,

wherein said silicide regions, said extrinsic base, and said emitter are all self-aligned with each other.

9. A method of forming a bipolar transistor structure, said method comprising:

forming a collector (12) in a substrate (10);

forming an intrinsic base (14) above said collector;

patterning an emitter pedestal (50) on said substrate above said intrinsic base;

forming an extrinsic base implant (80, 170, 190) in regions of said substrate not protected by said emitter pedestal;

removing said emitter pedestal; and

forming an emitter (130) where said emitter pedestal was positioned.

10. The method in claim 9, further comprising, before removing said emitter pedestal, forming an isolation layer (90) adjacent said emitter pedestal.

11. The method in claim 10, wherein said process of removing said emitter pedestal leaves an emitter opening in said alignment layer, and wherein said process of forming said emitter forms said emitter in said emitter opening of said alignment layer.

12. The method in claim 9, wherein said process of forming said extrinsic base comprises:

performing a first impurity implant (80) into regions (82) of said substrate not protected by said emitter pedestal;

forming a first sidewall spacer (450) on said emitter pedestal;

performing a second impurity implant (170) into regions (172) of said substrate not protected by said emitter pedestal and said first sidewall spacer;

removing said first sidewall spacer;

forming a second sidewall spacer (460) on said emitter pedestal, wherein said second sidewall spacer extends further from said emitter pedestal than did said first sidewall spacer; and

performing a third impurity implant (190) into regions (192) of said substrate not protected by said emitter pedestal and said second sidewall spacer.

13. The method in claim 12, further comprising:

removing said second sidewall spacer; and

after forming said emitter, forming an isolation region (480) directly adjacent said emitter,

wherein the thicknesses of said first sidewall spacer and said second sidewall spacer and their related implants are independent of the thickness of said isolation region.

14. The method in claim 9, further comprising, before patterning said emitter pedestal on said substrate, forming an etch stop layer (20) over said substrate.

15. The method in claim 14, wherein the thickness of said etch stop layer is controlled to reduce the energy required for said process of forming said extrinsic base regions.

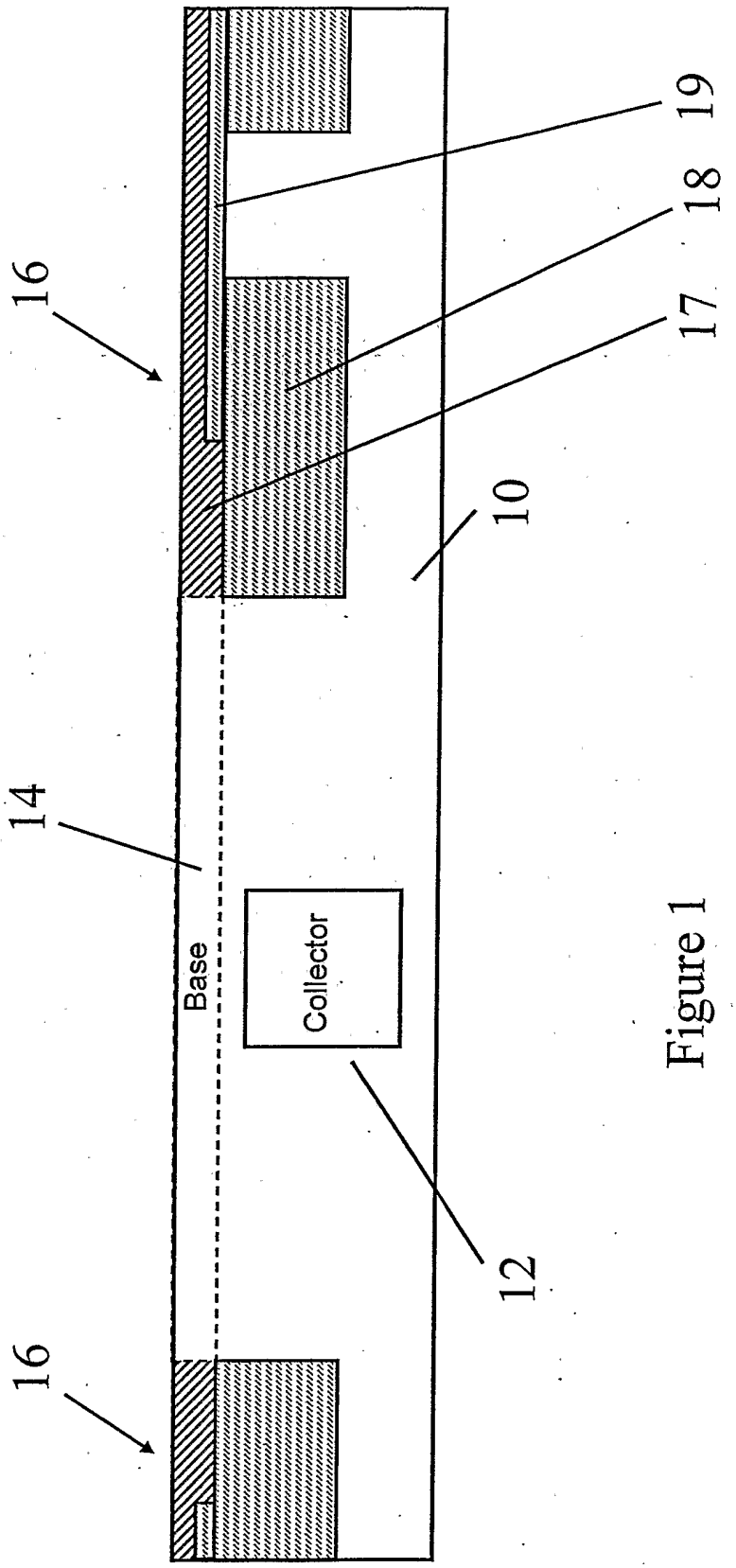


Figure 1

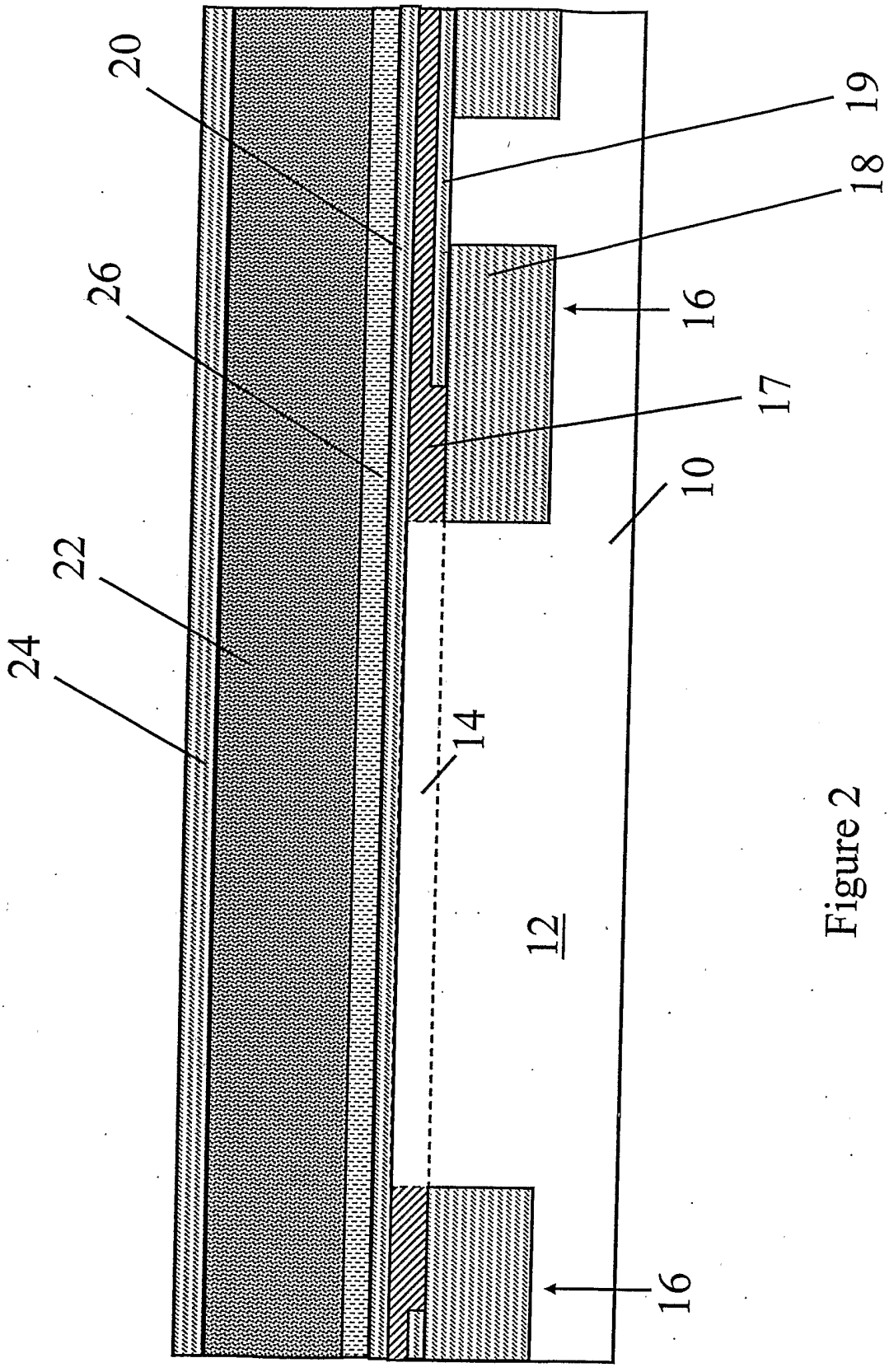


Figure 2

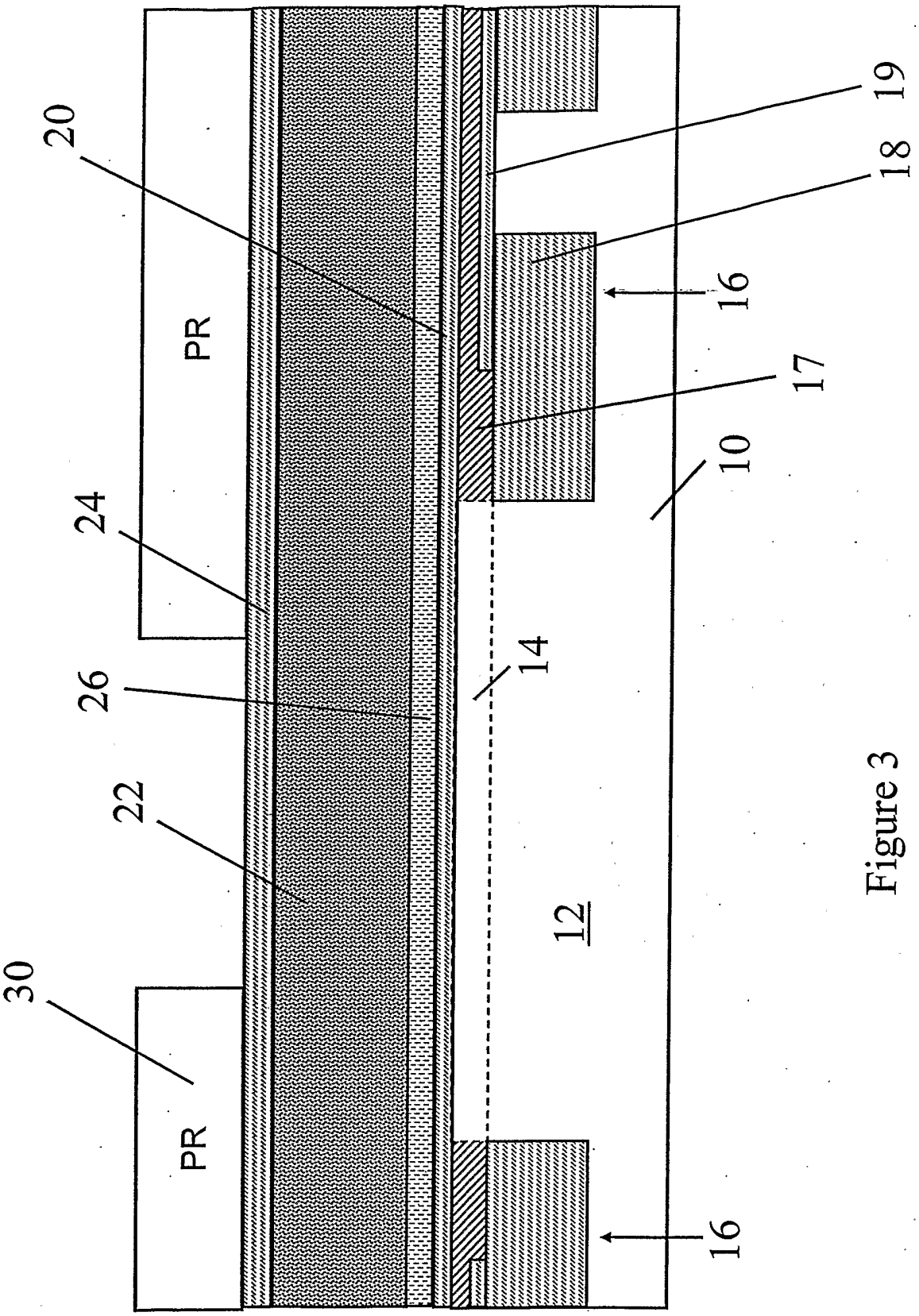


Figure 3

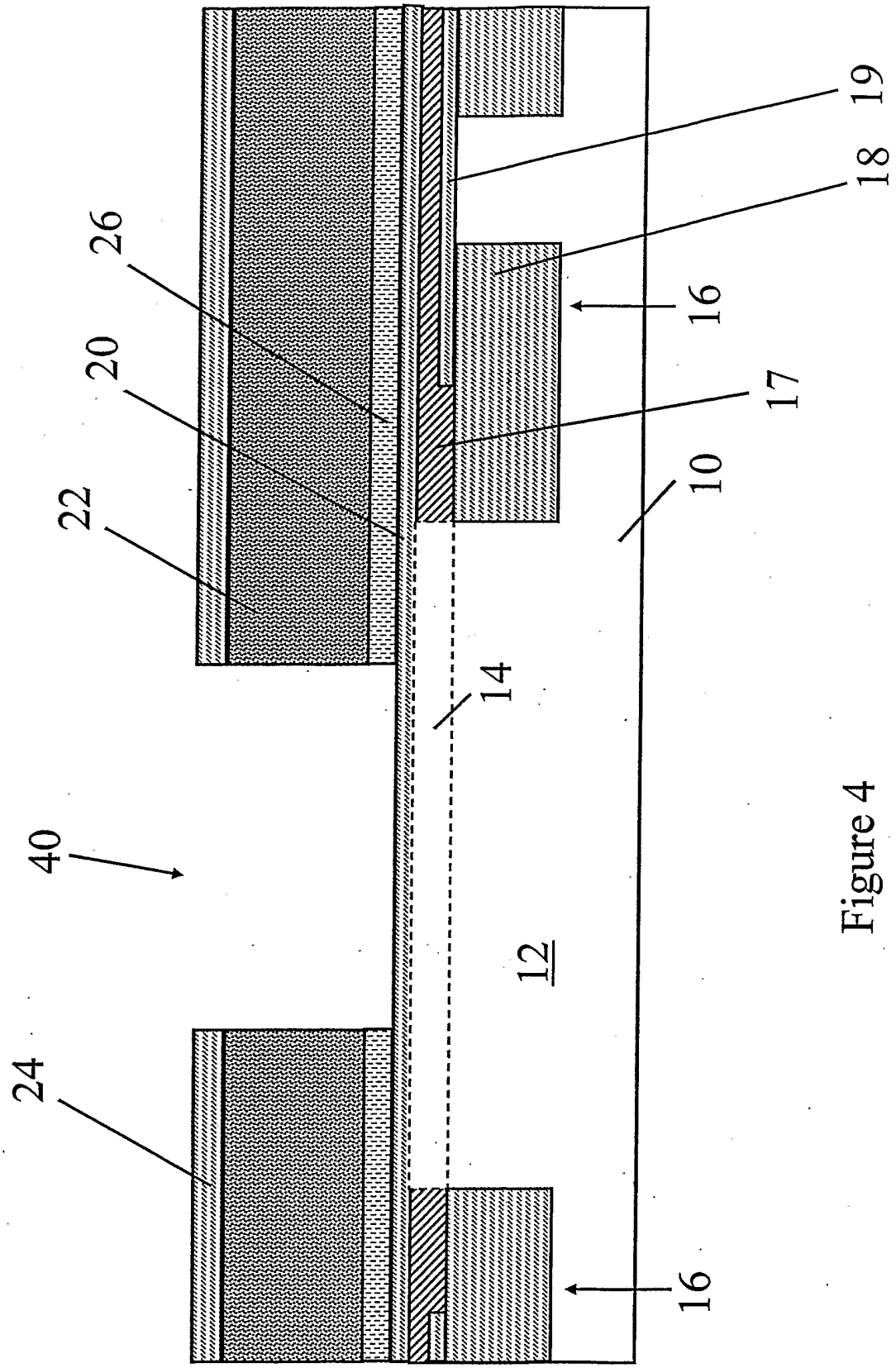


Figure 4

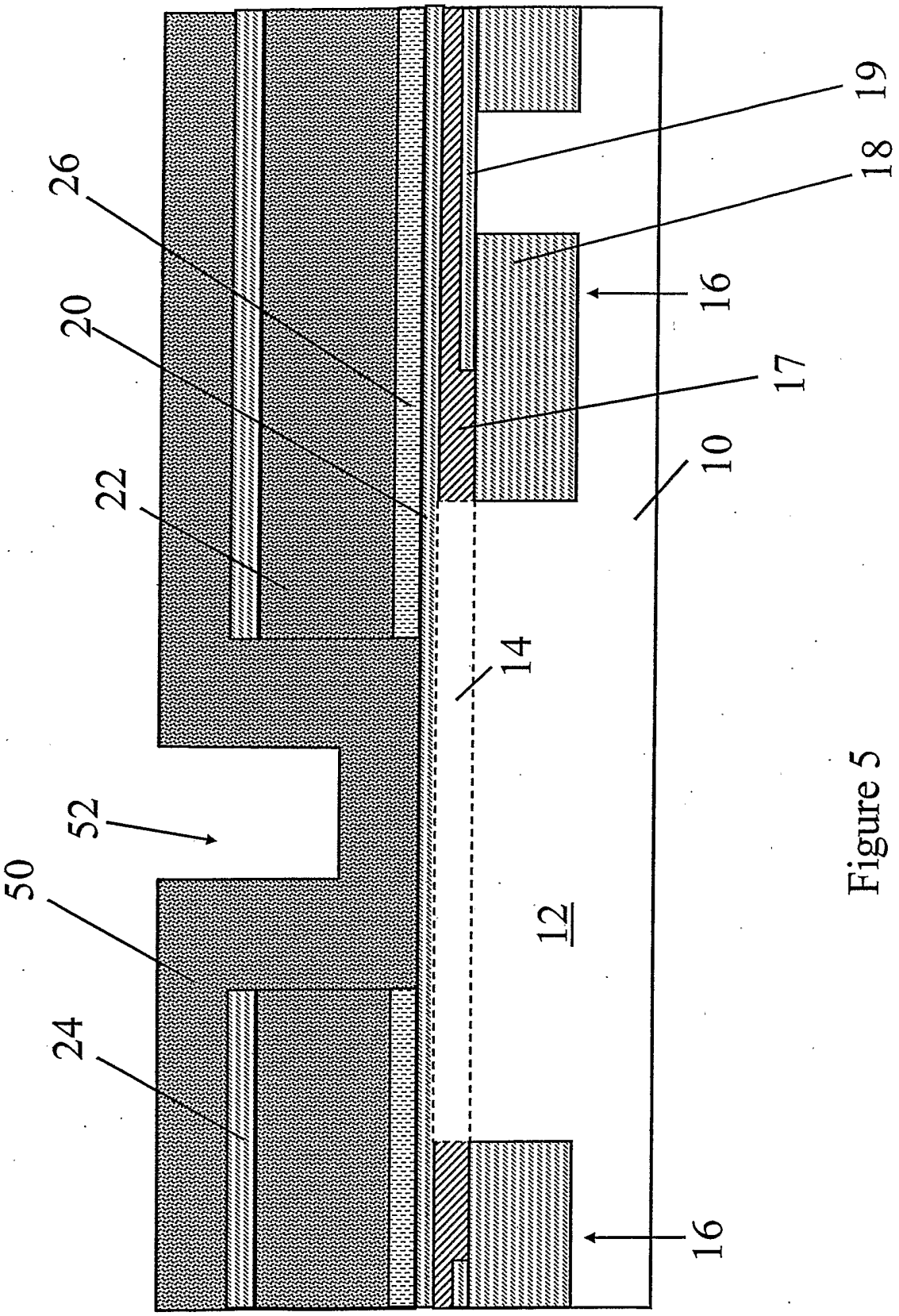


Figure 5

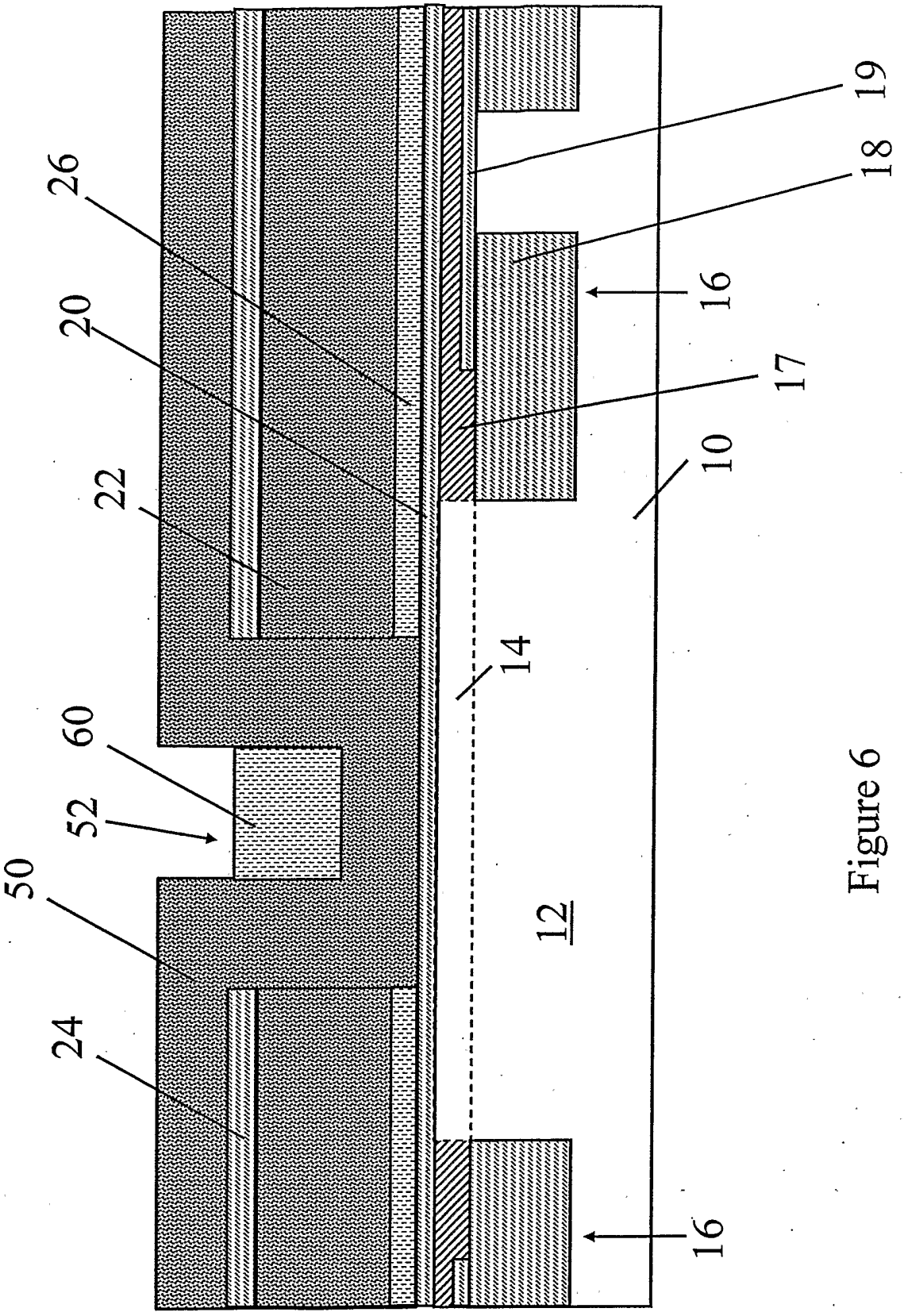


Figure 6

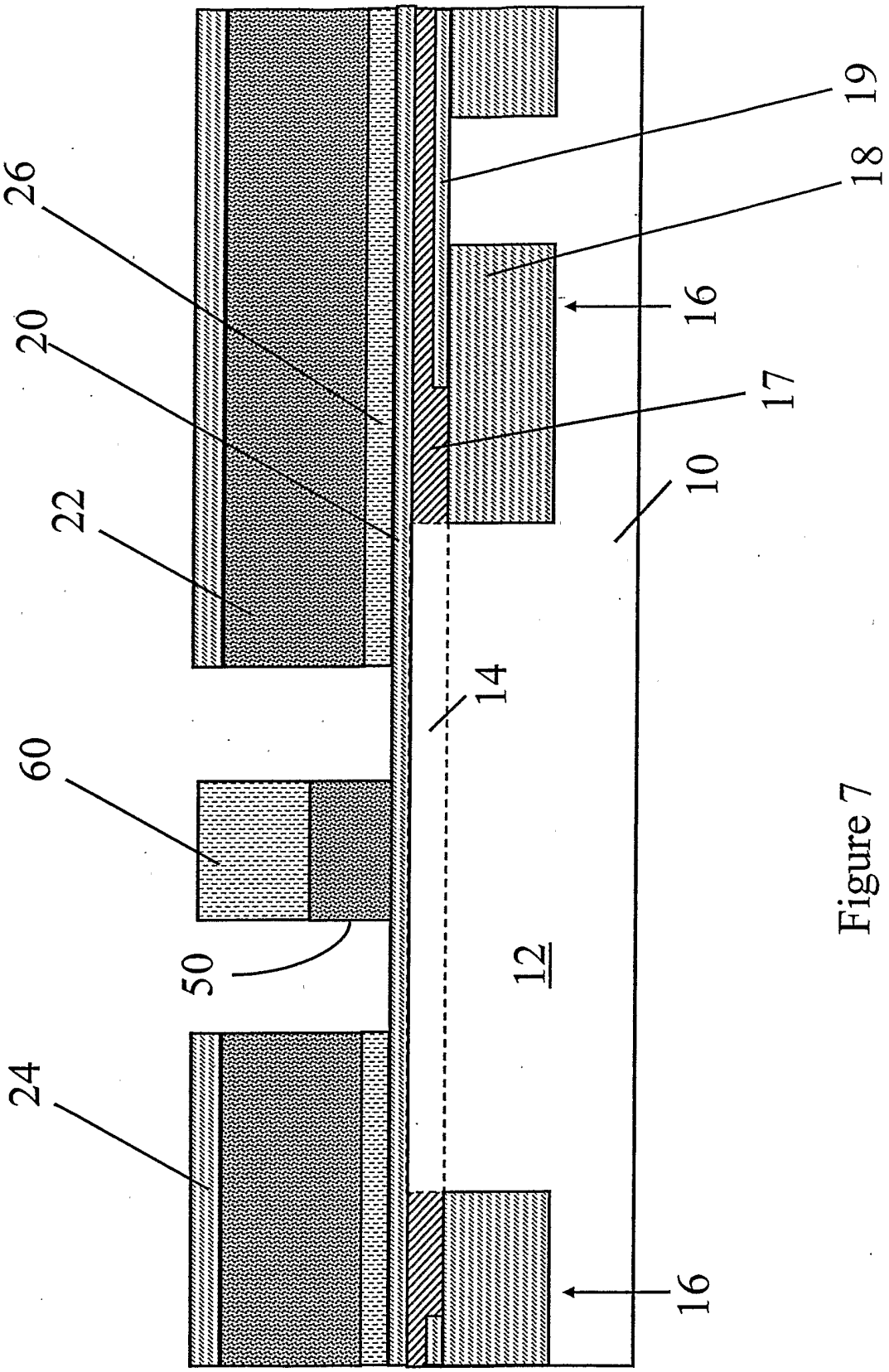


Figure 7

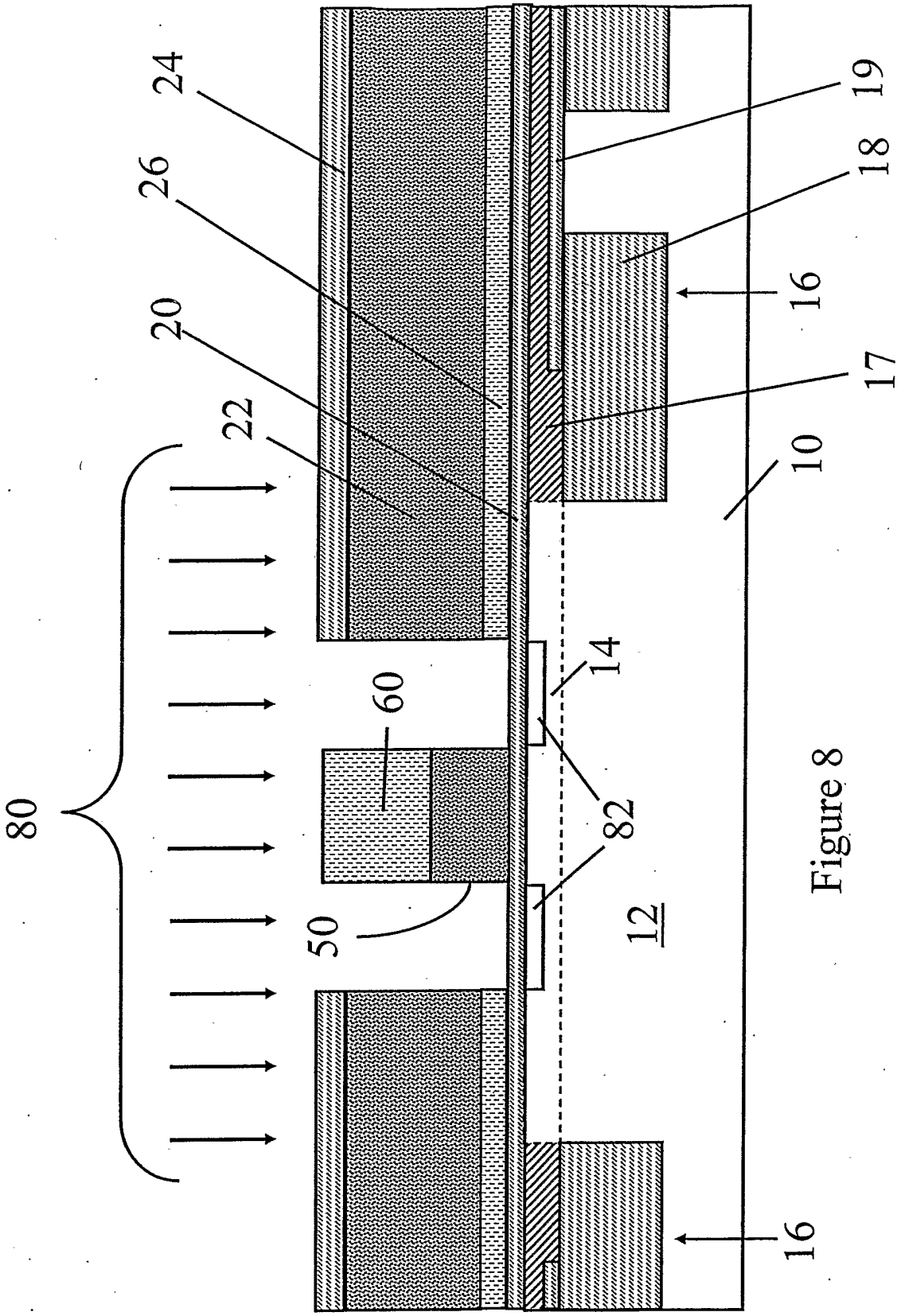


Figure 8

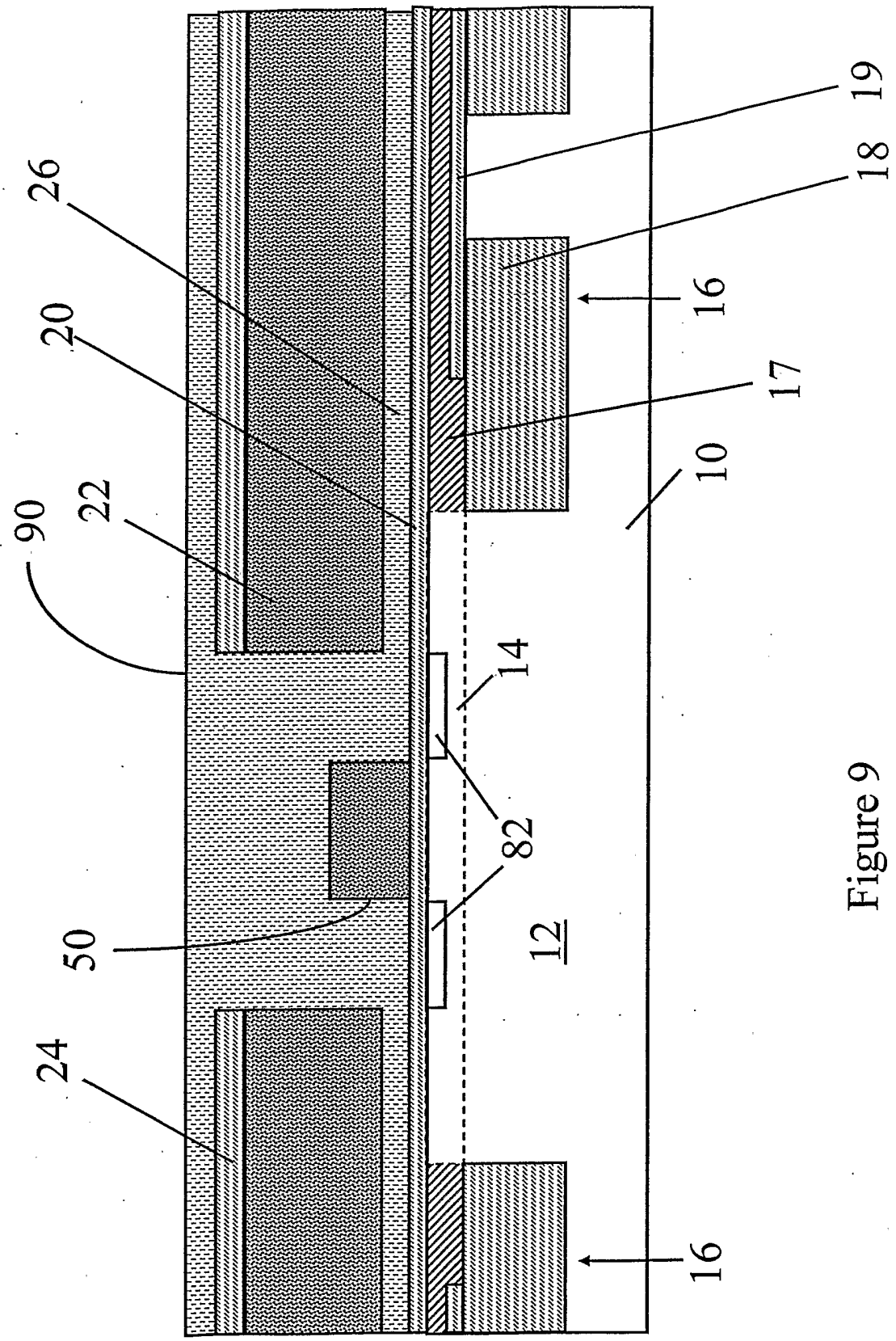


Figure 9

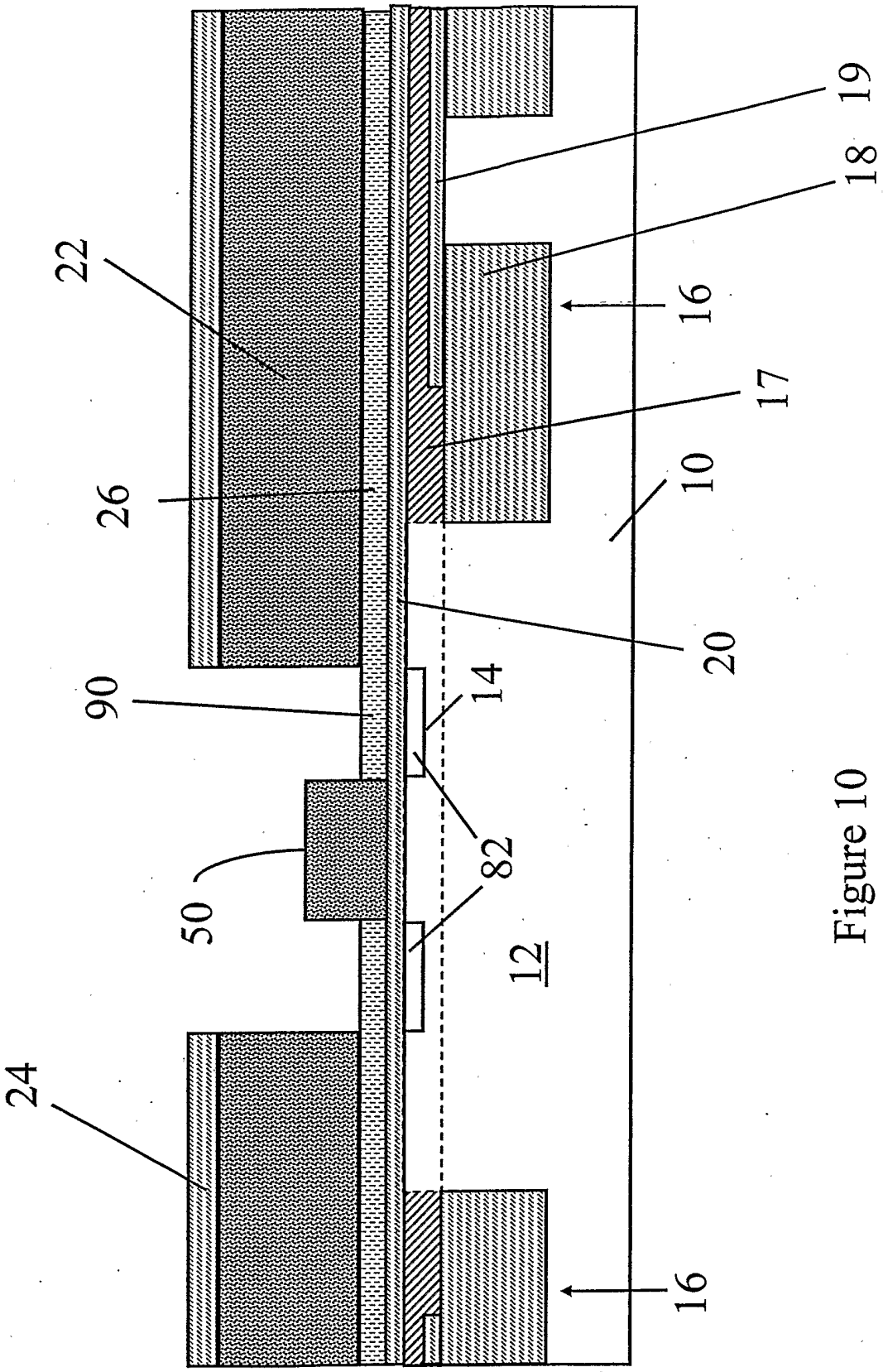


Figure 10

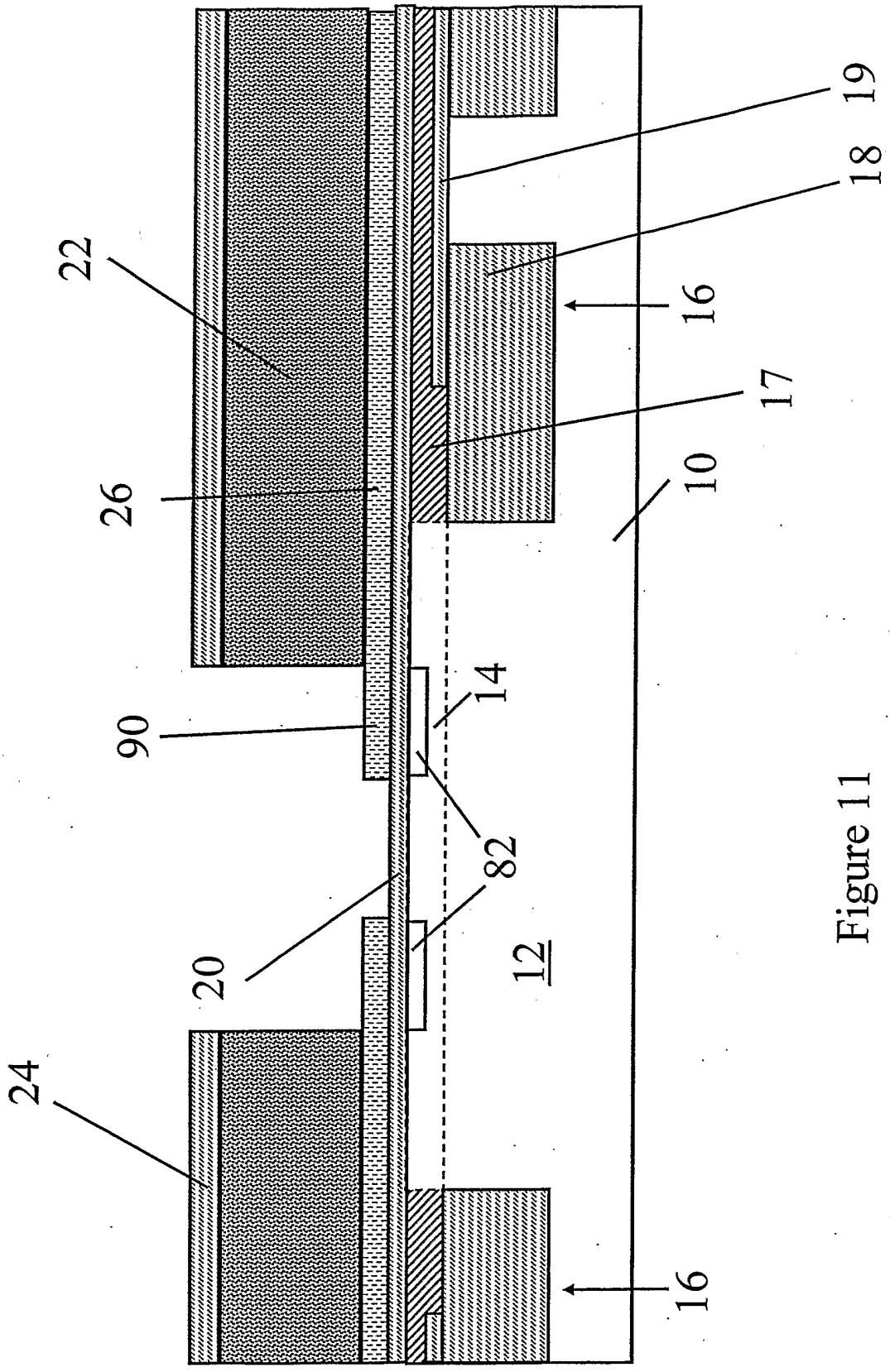


Figure 11

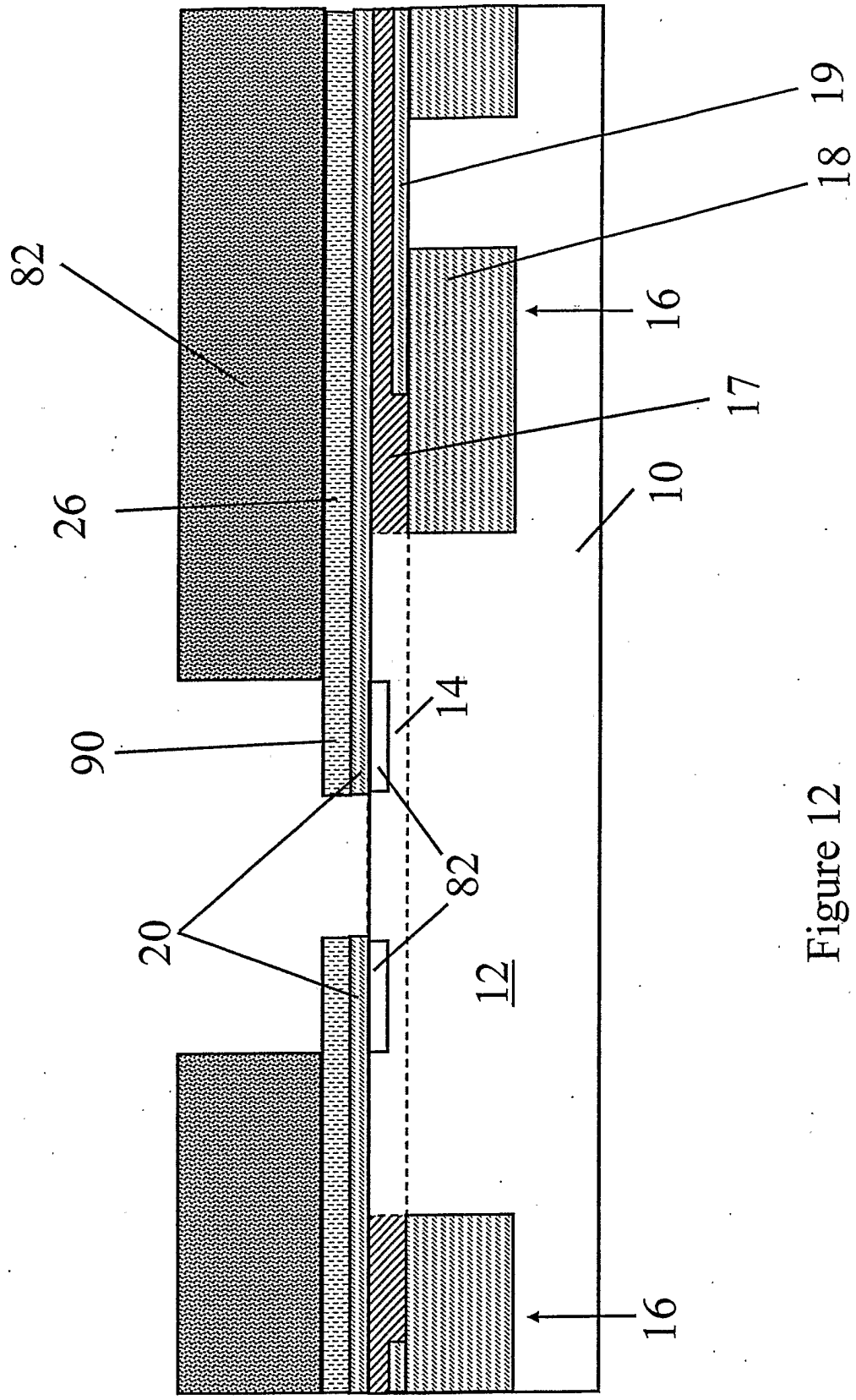


Figure 12

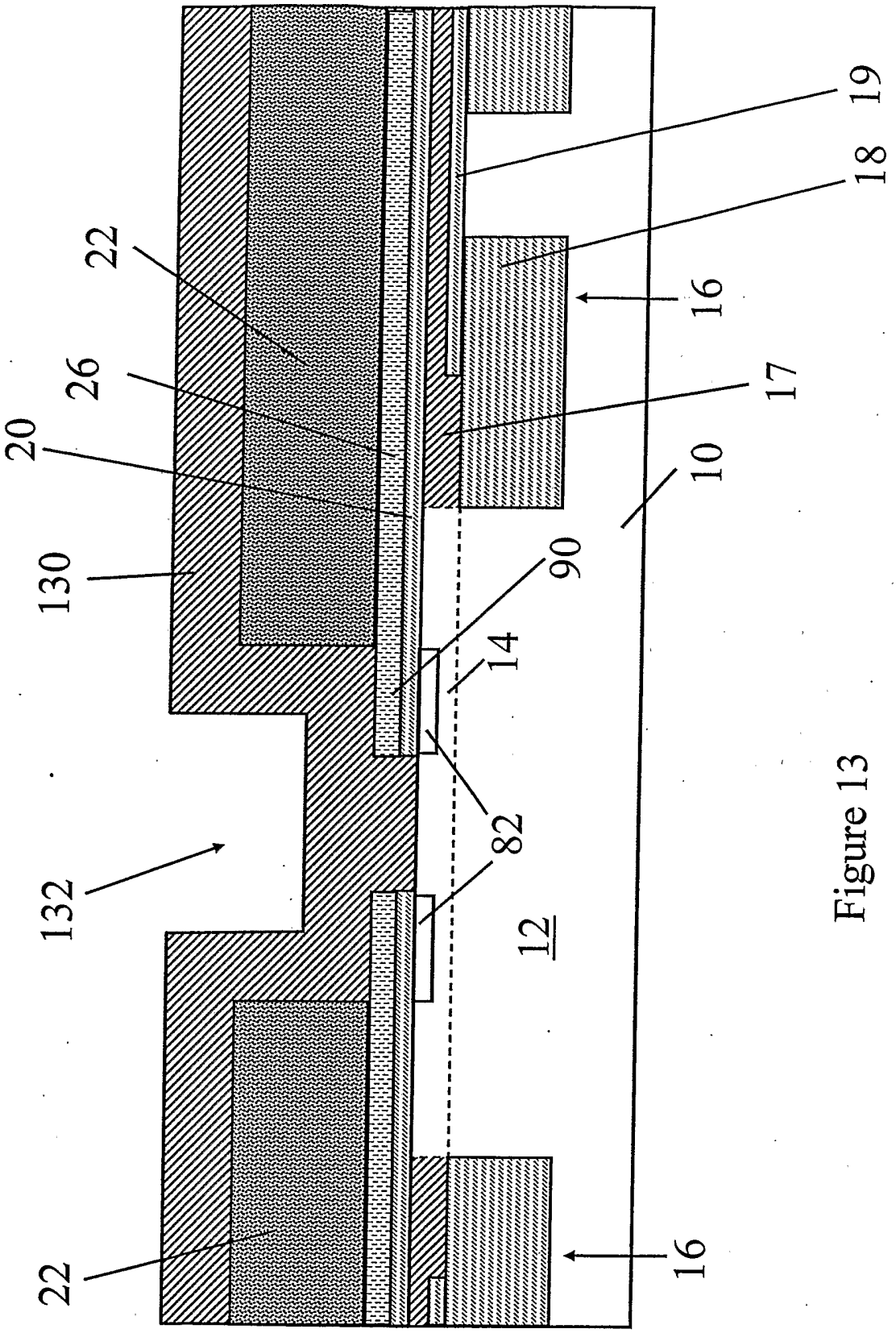


Figure 13

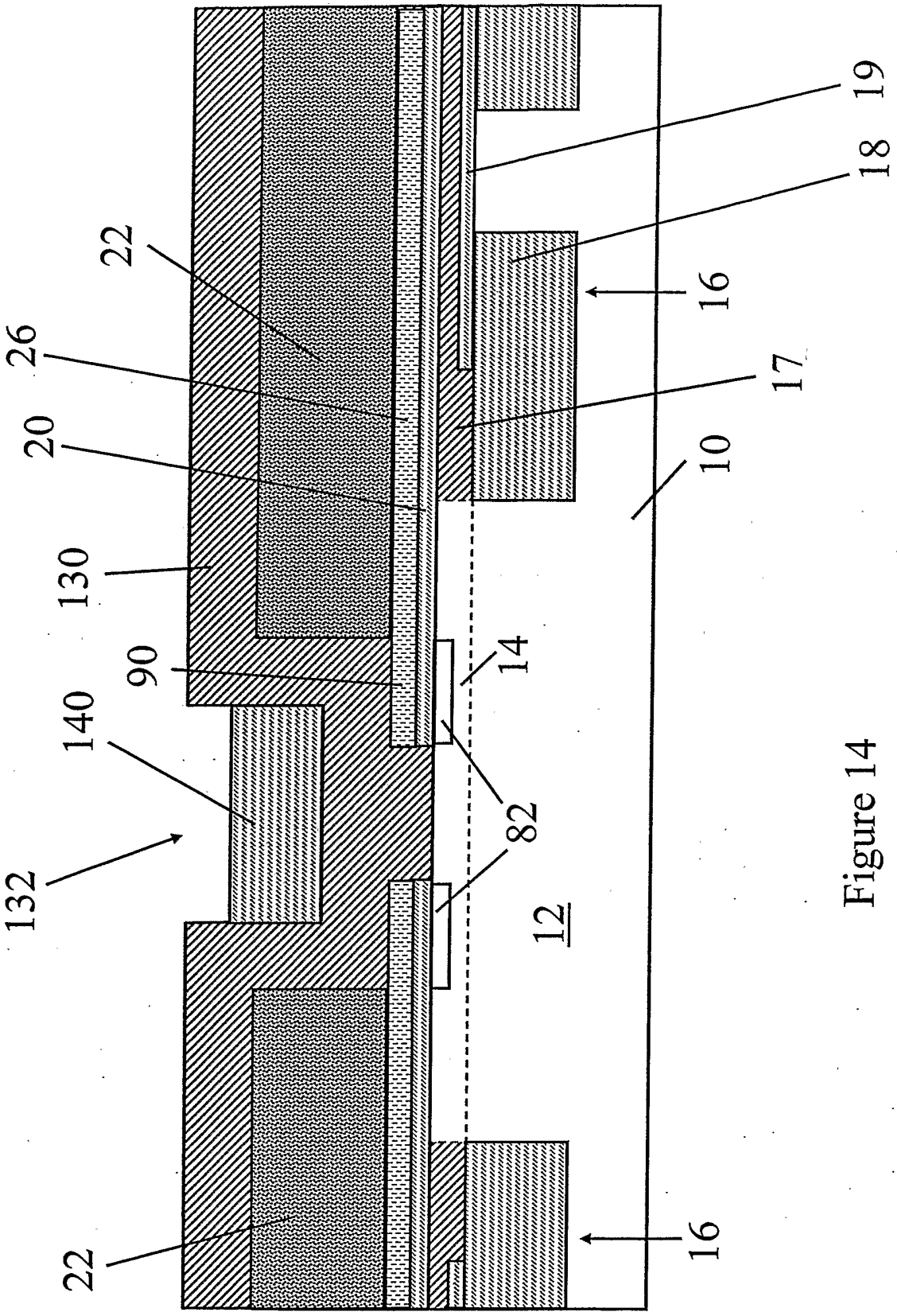


Figure 14

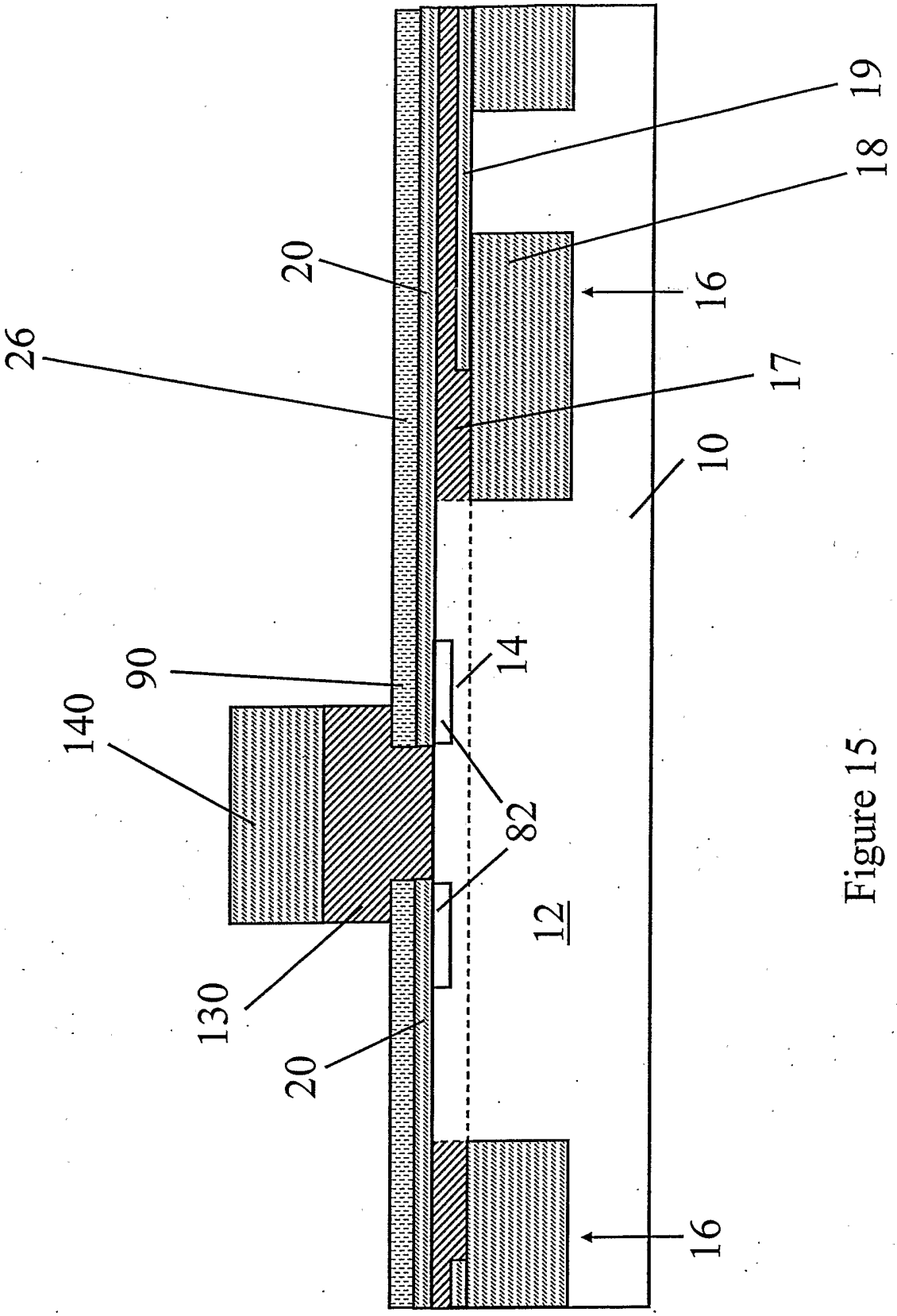


Figure 15

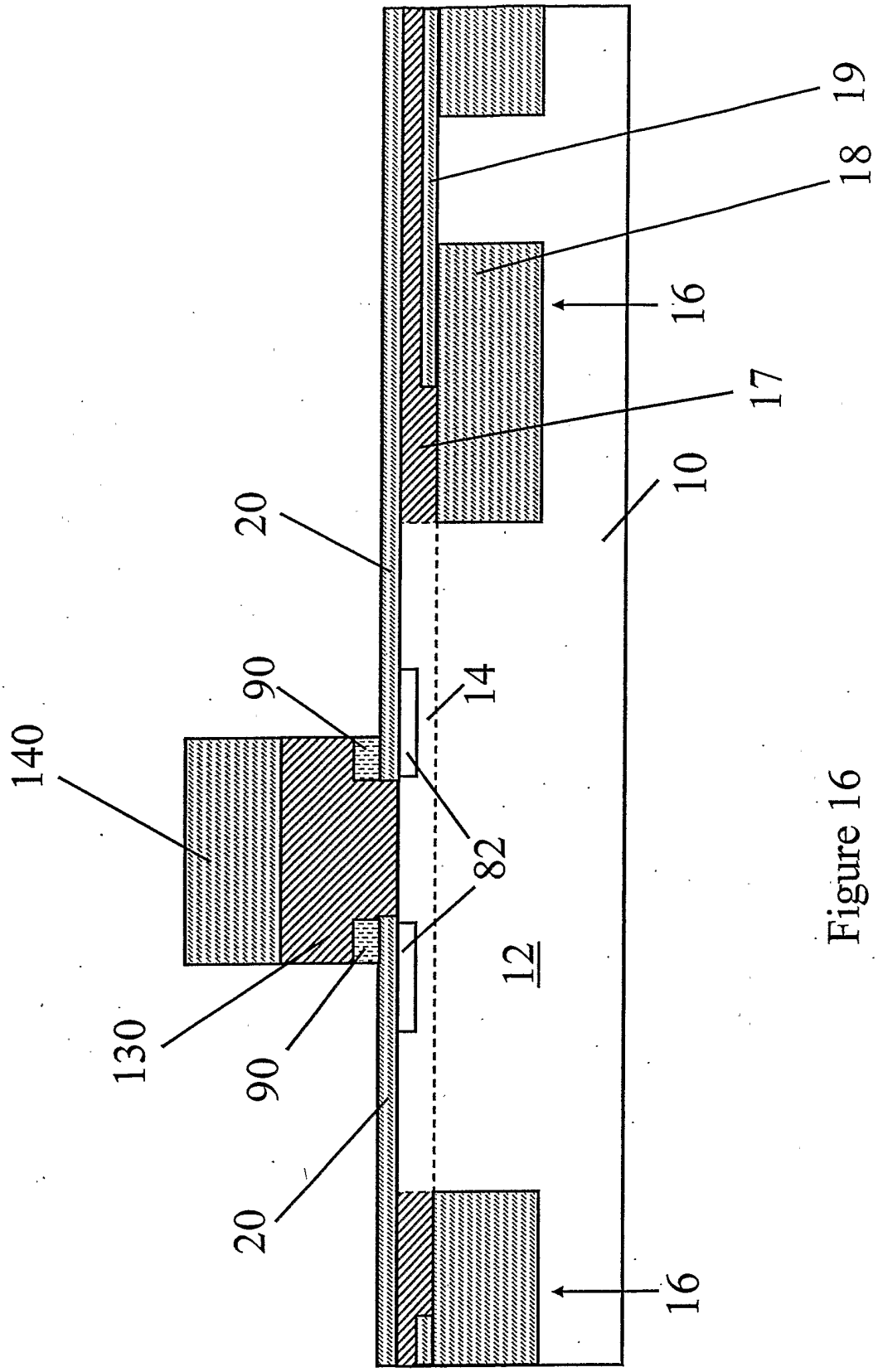


Figure 16

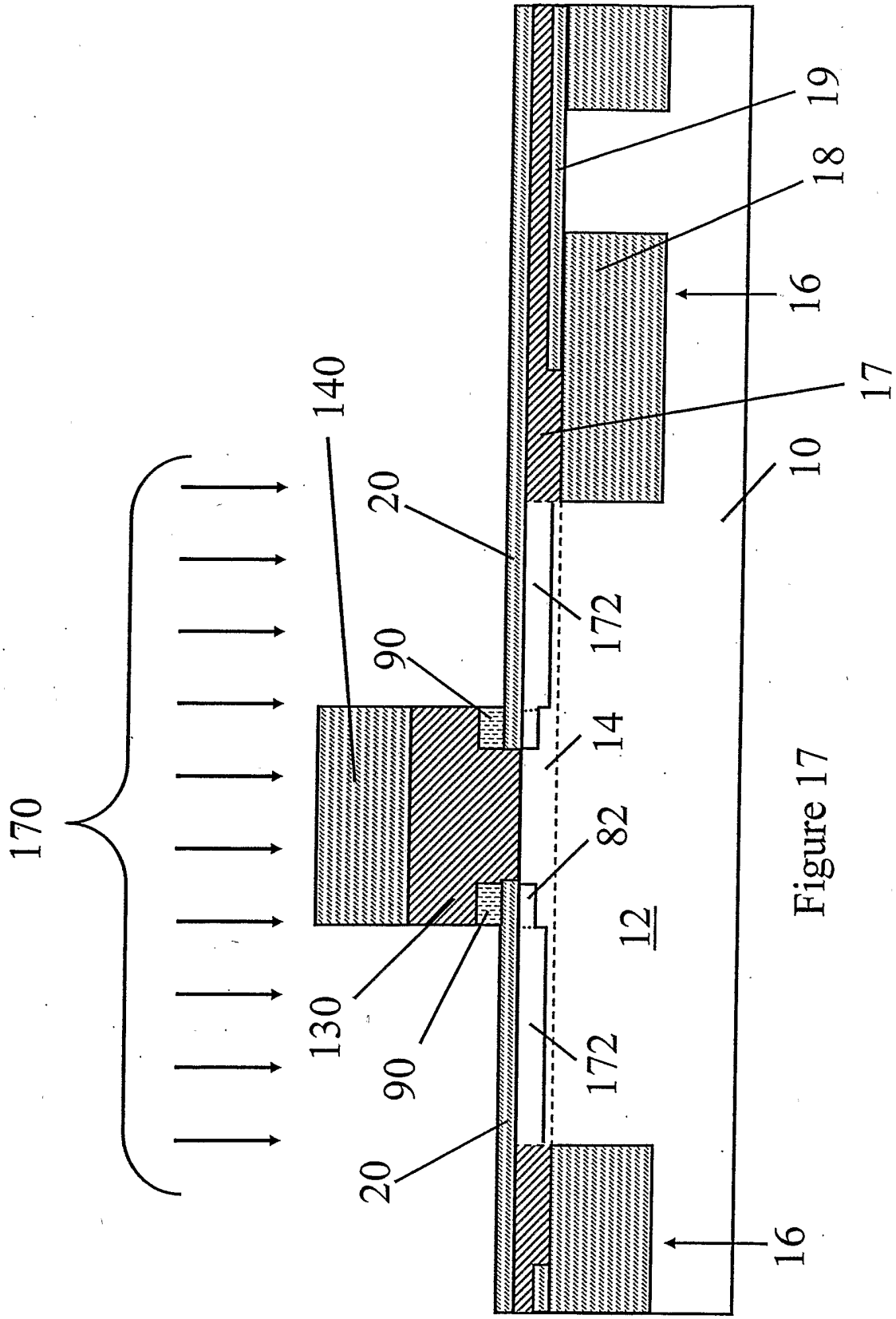


Figure 17

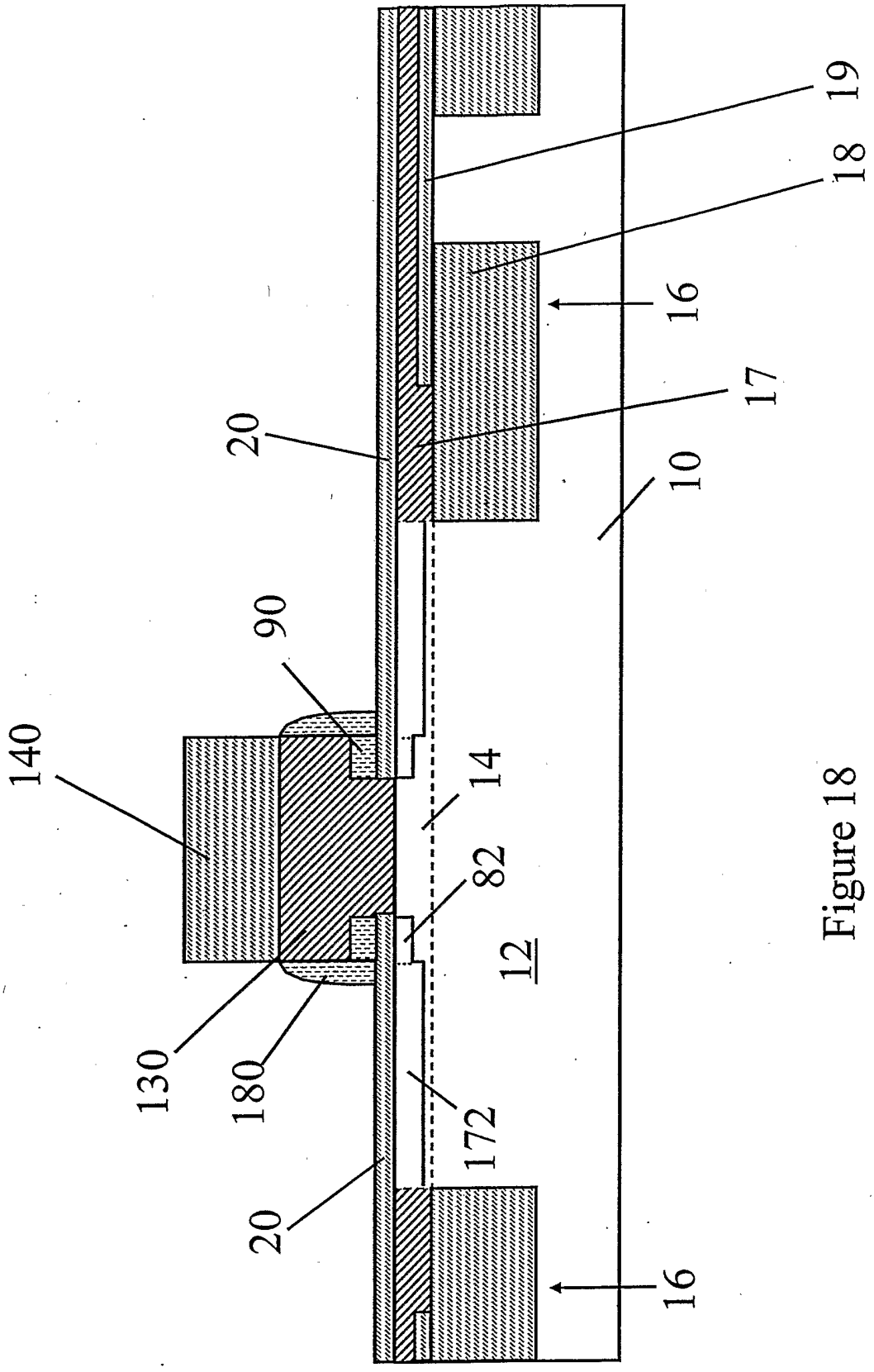


Figure 18

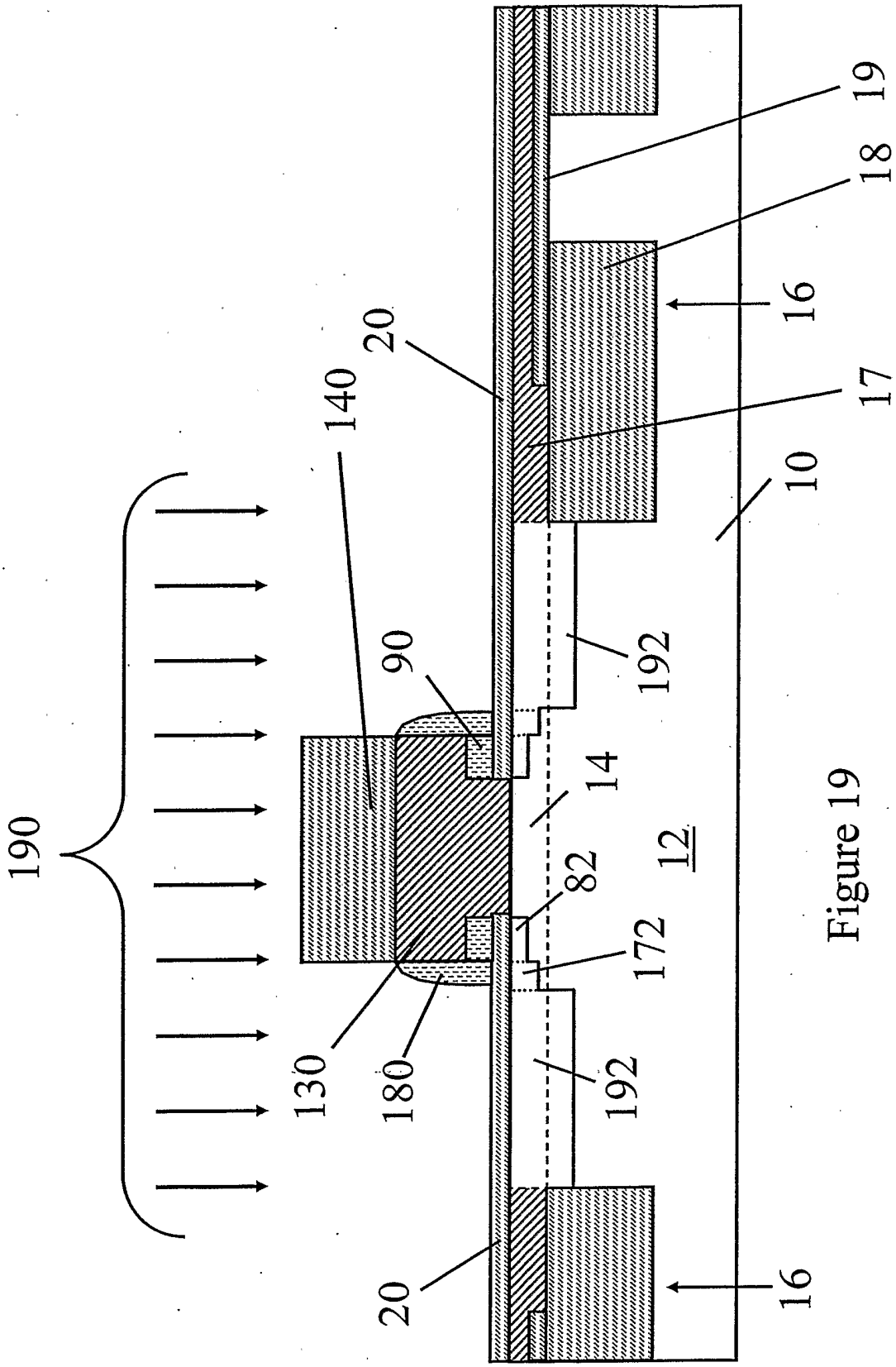


Figure 19

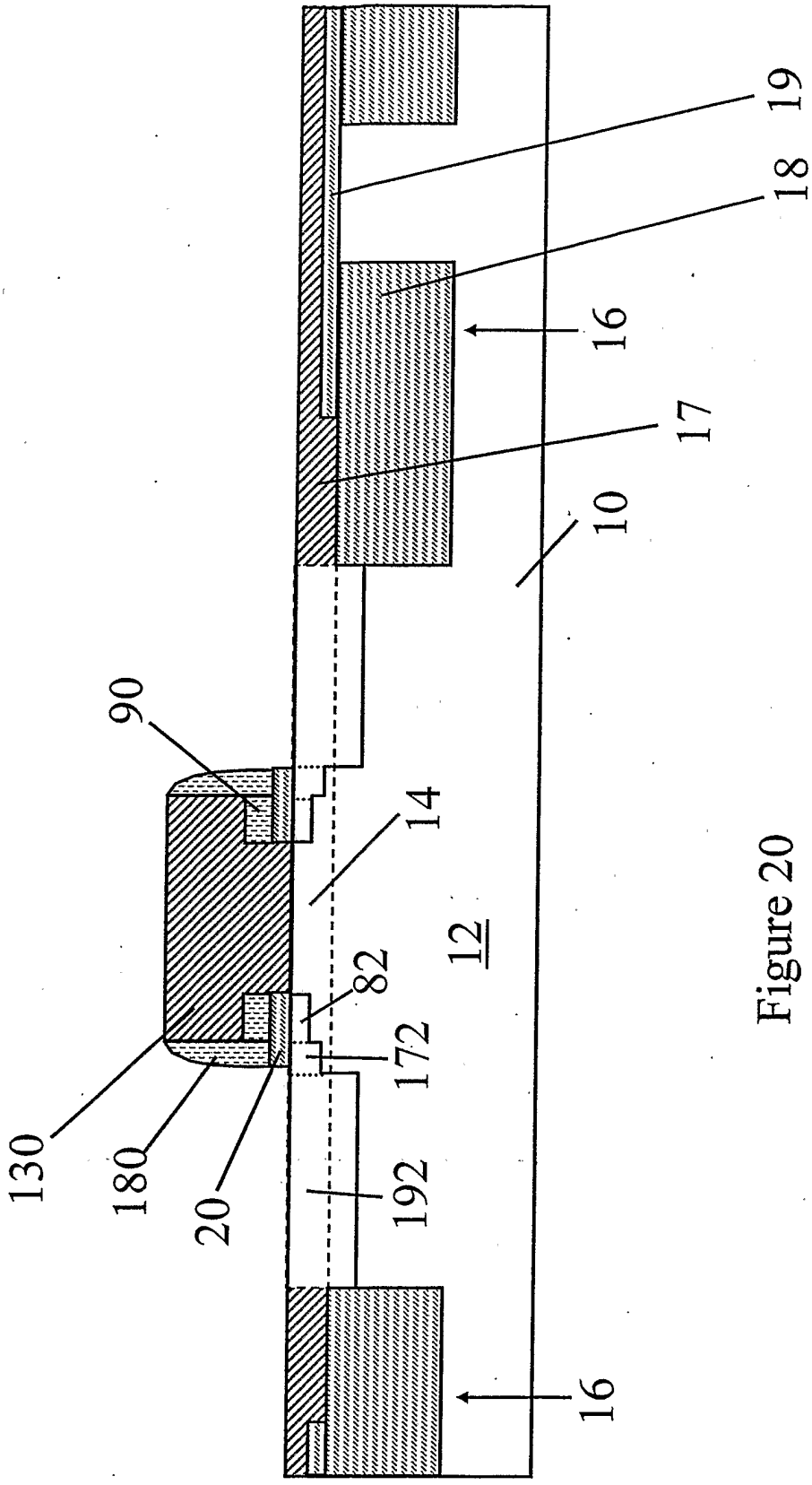


Figure 20

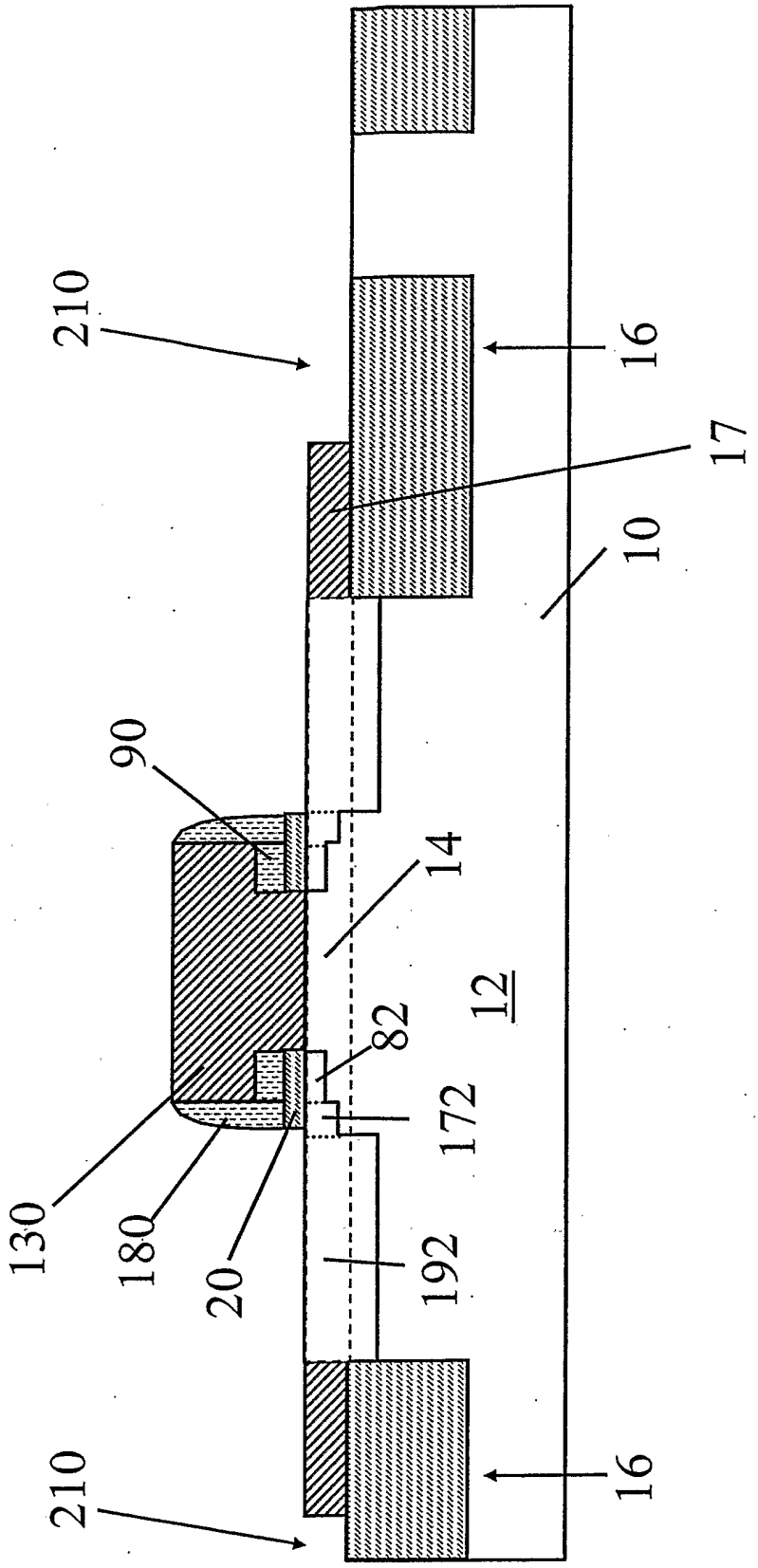


Figure 21

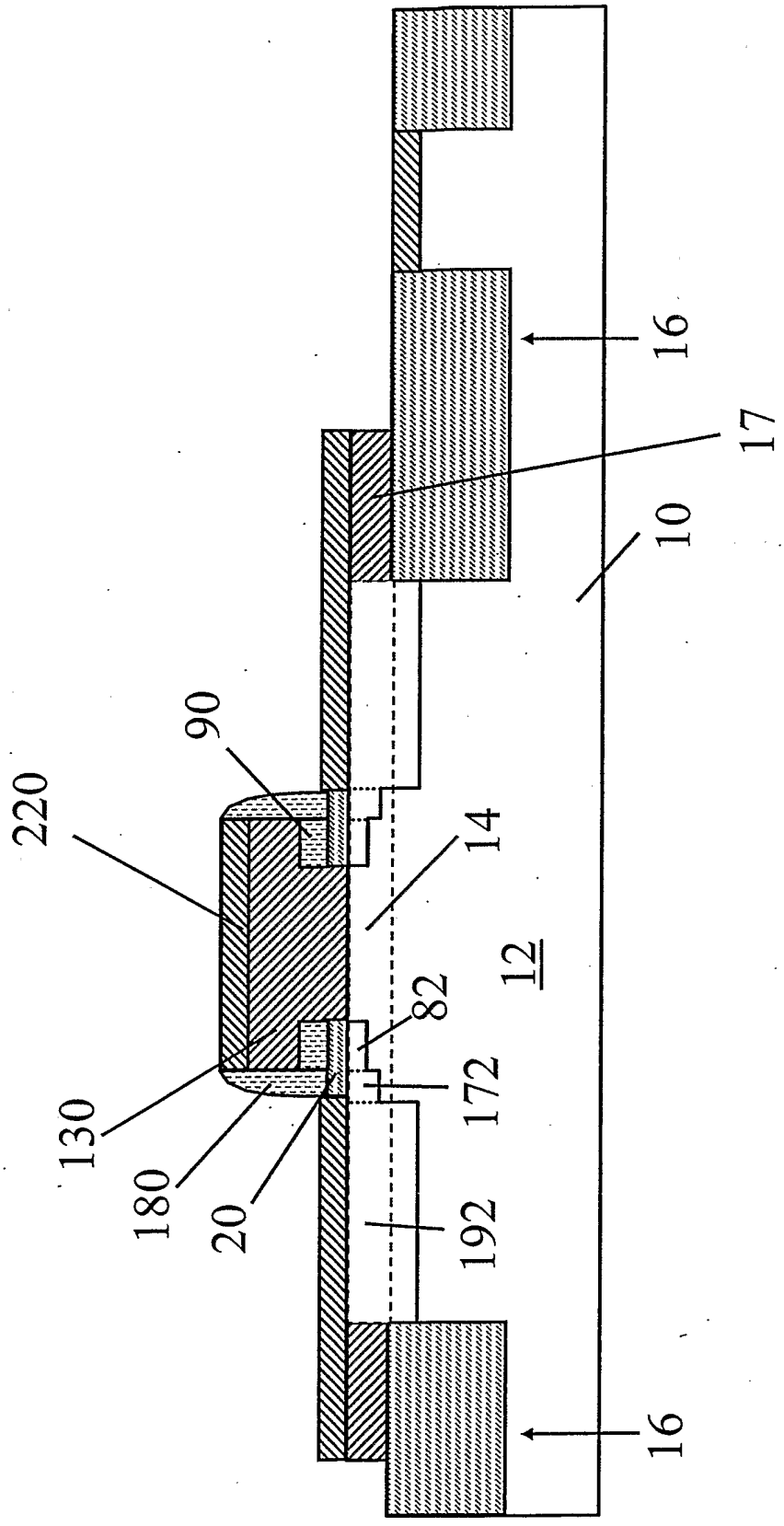


Figure 22

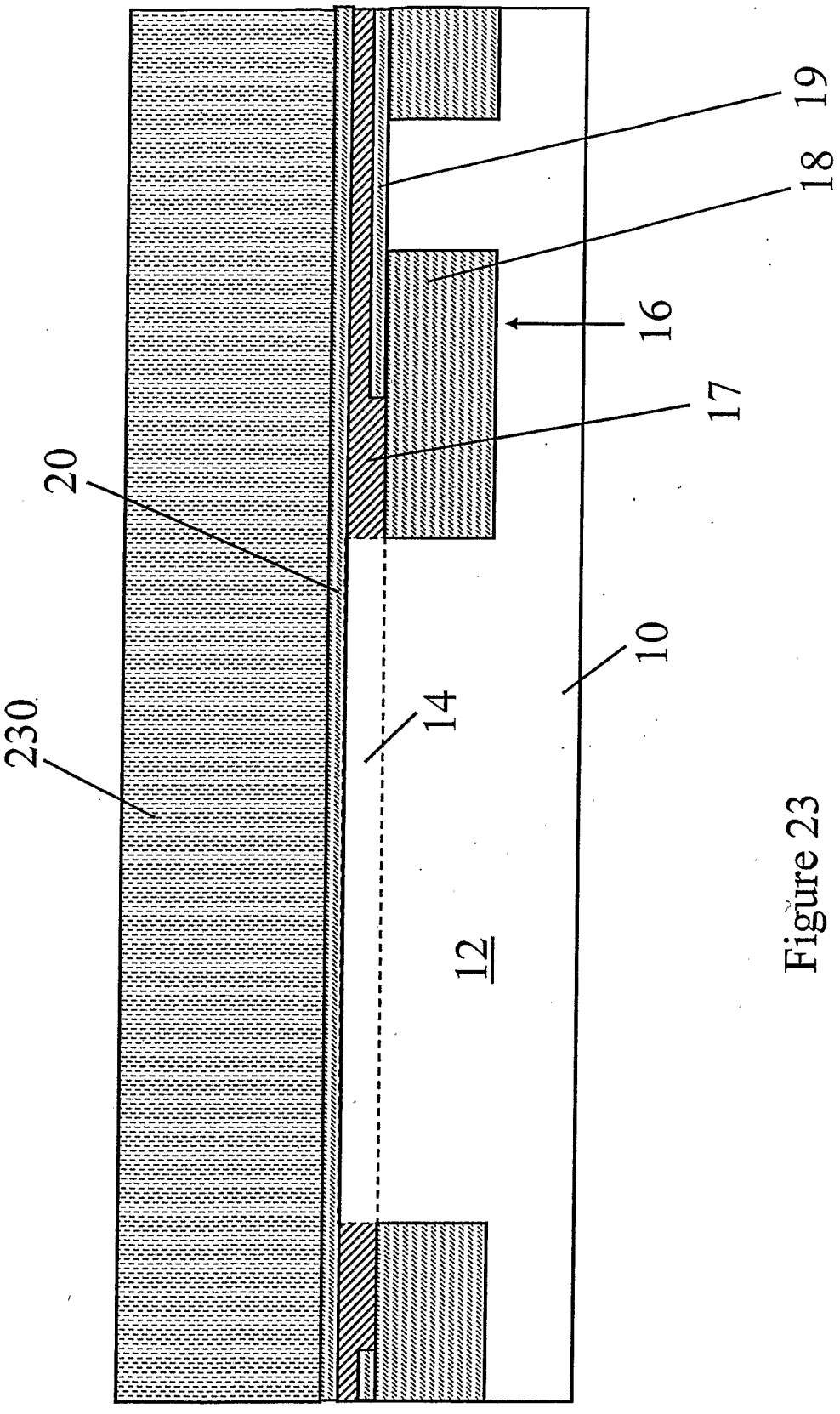


Figure 23

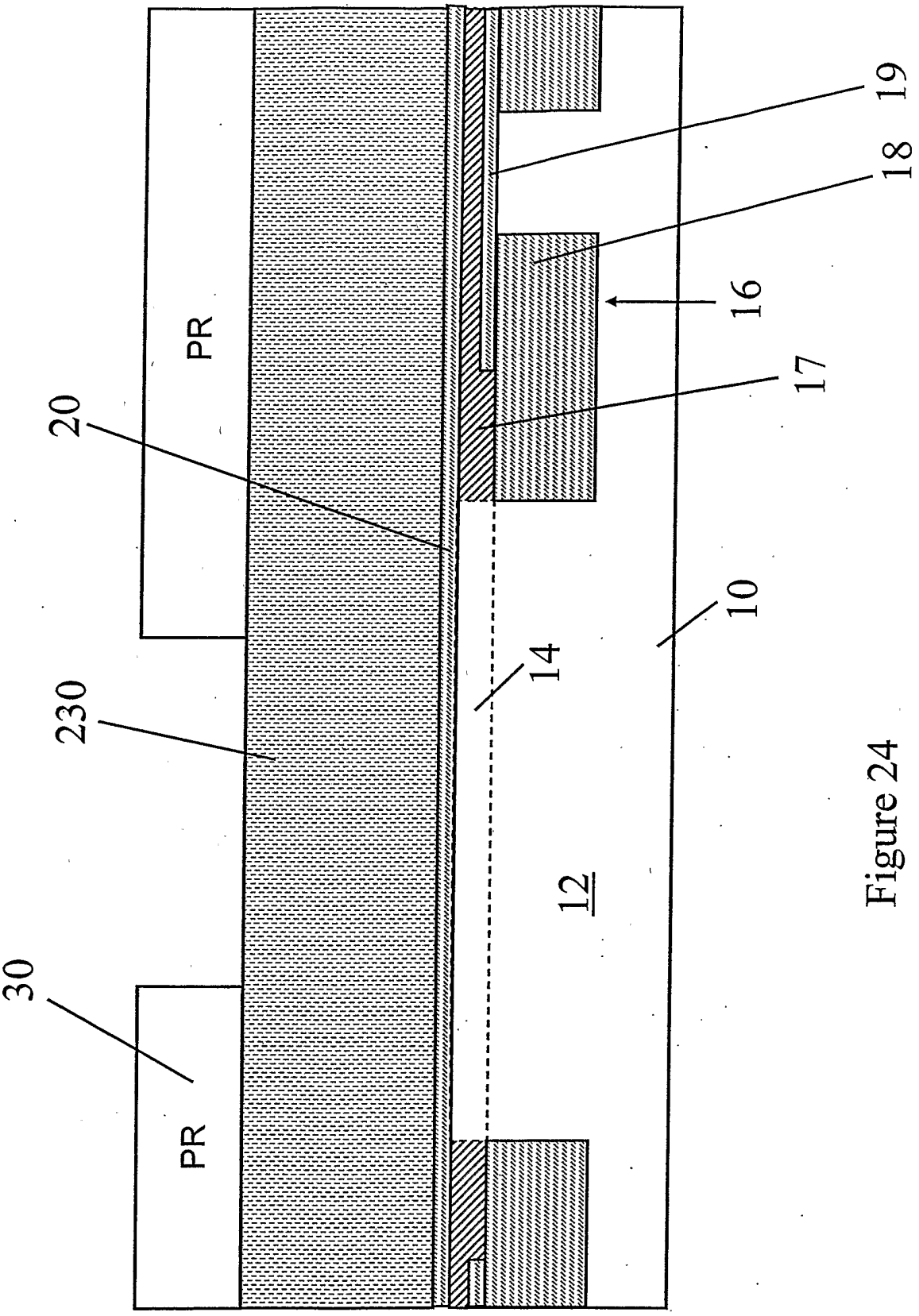


Figure 24

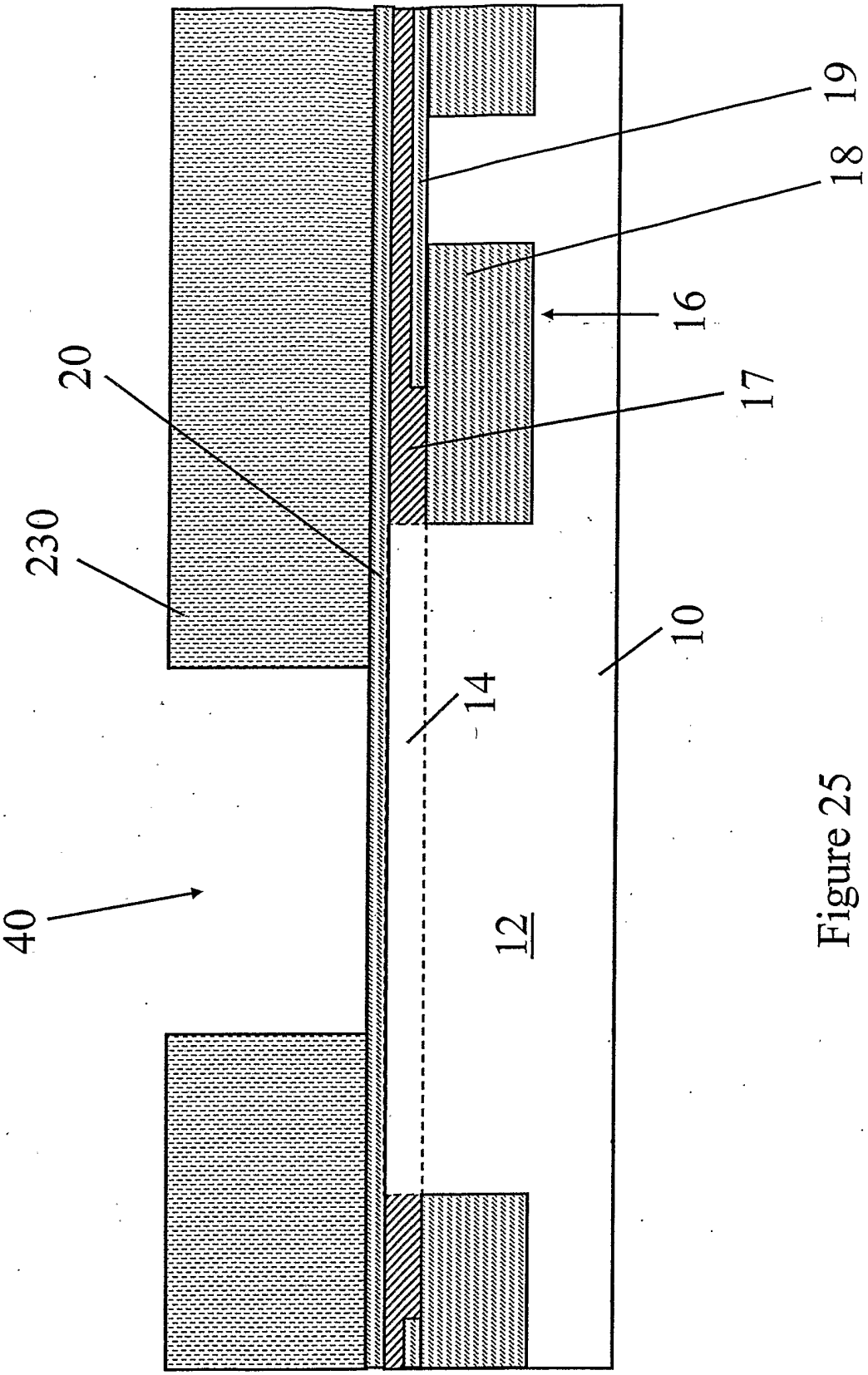


Figure 25

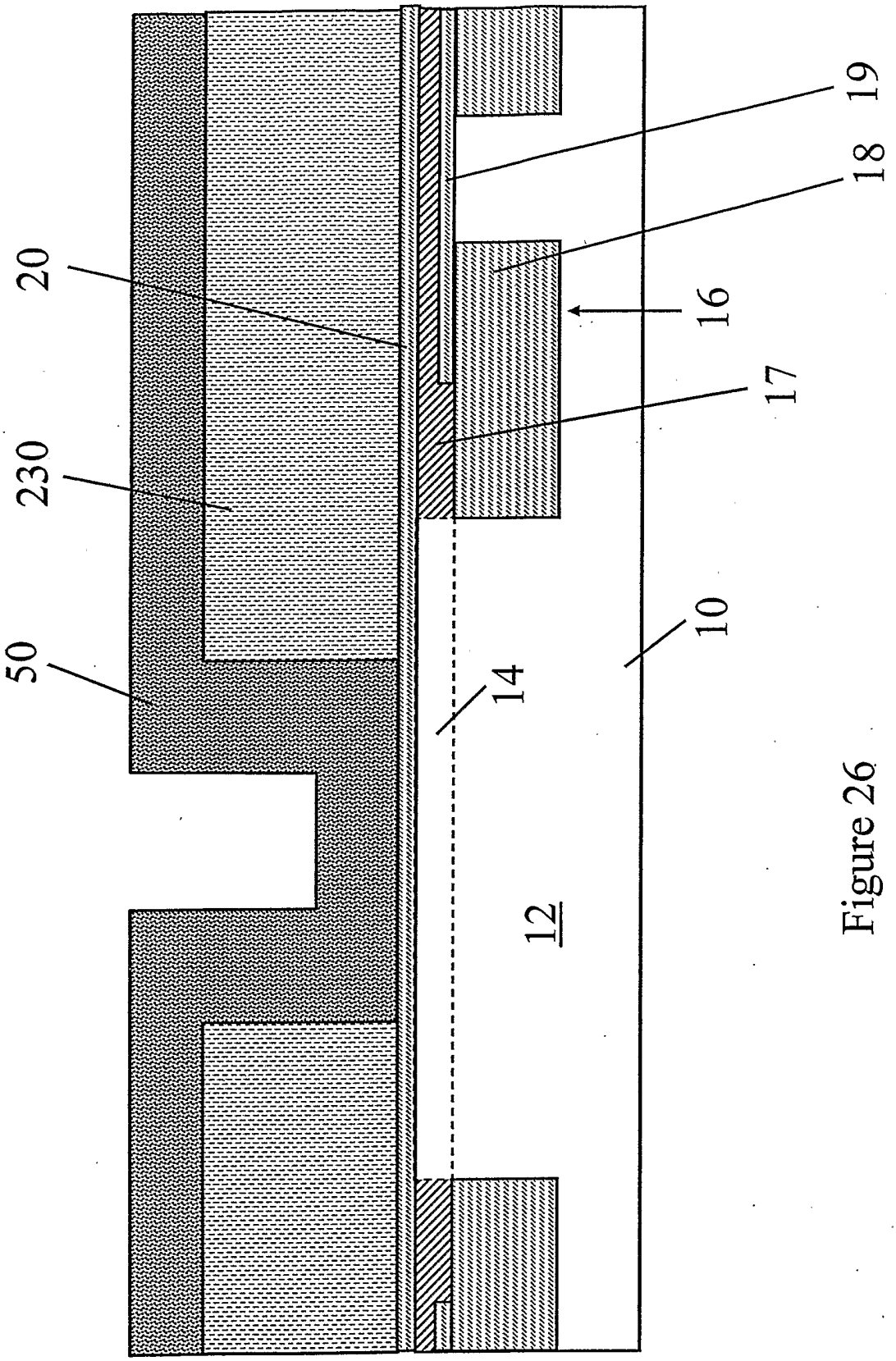


Figure 26

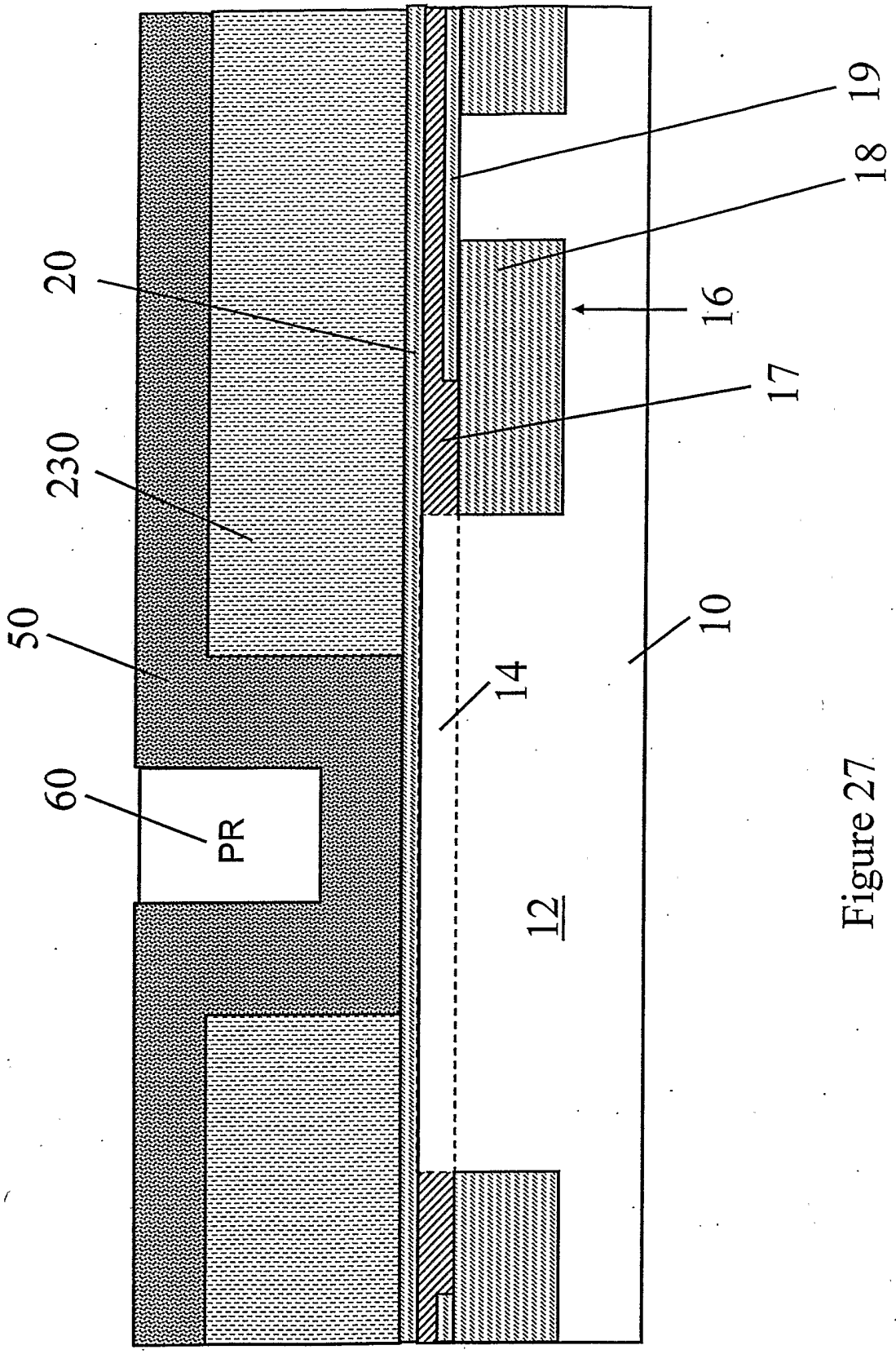


Figure 27

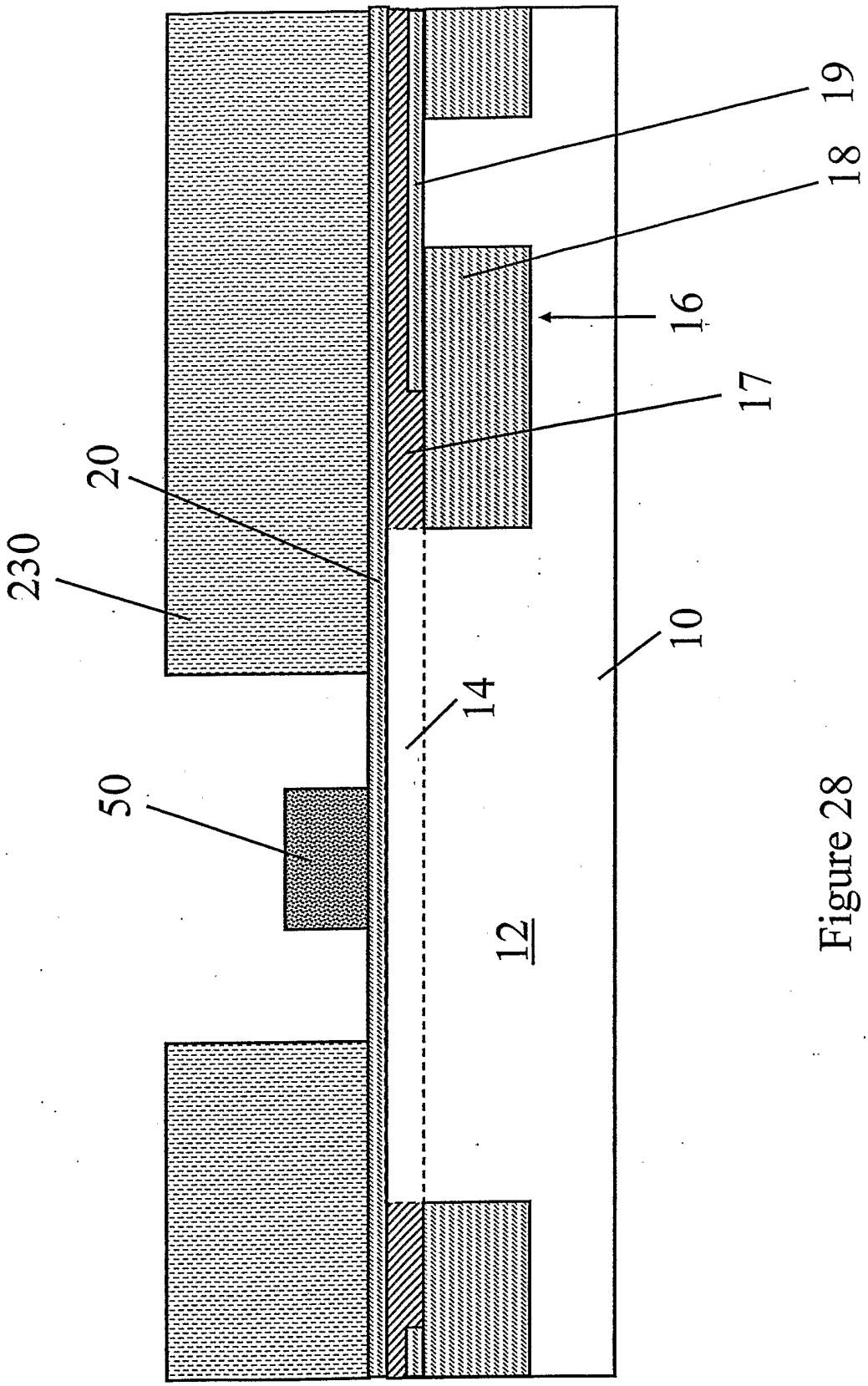


Figure 28

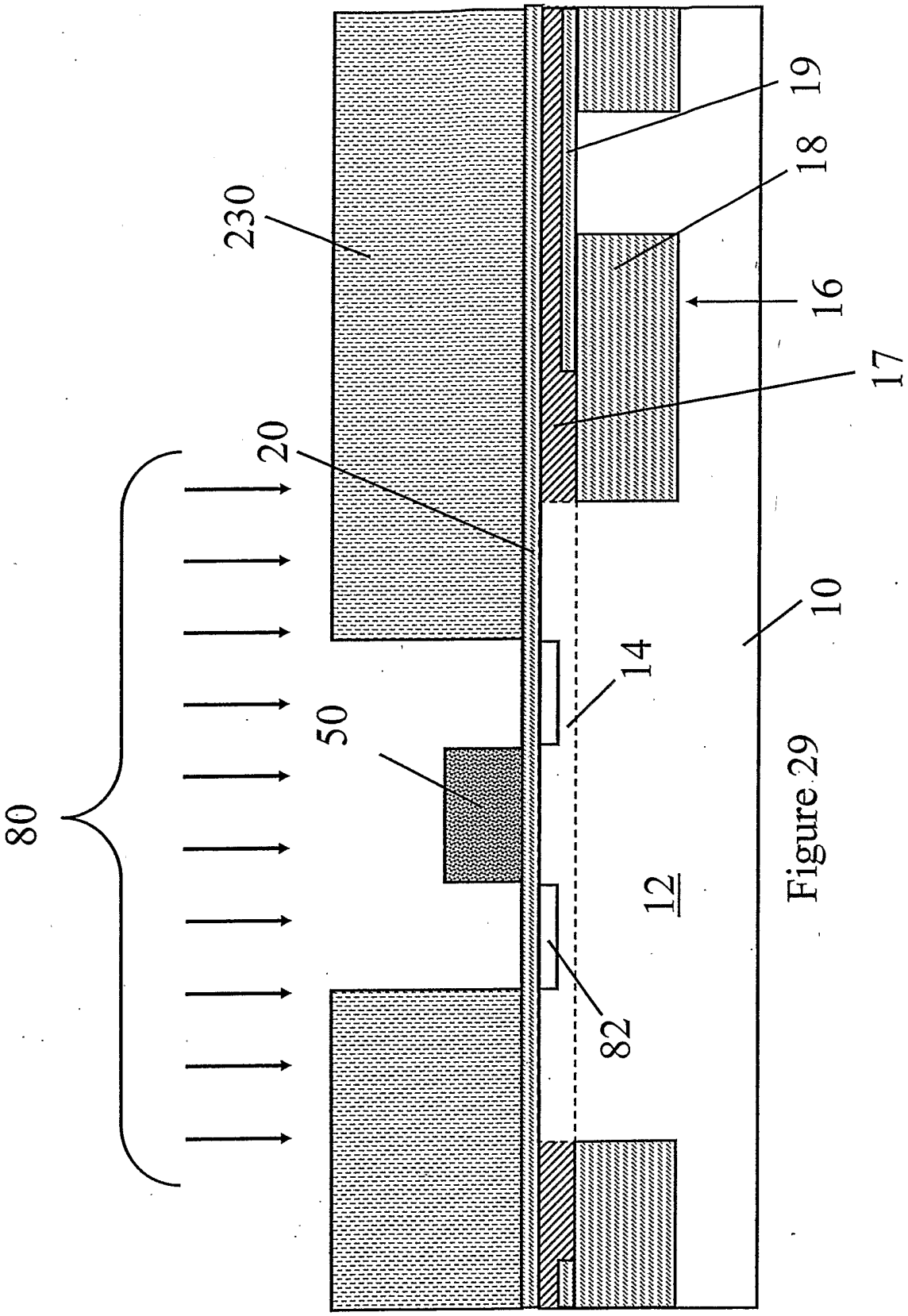


Figure 29

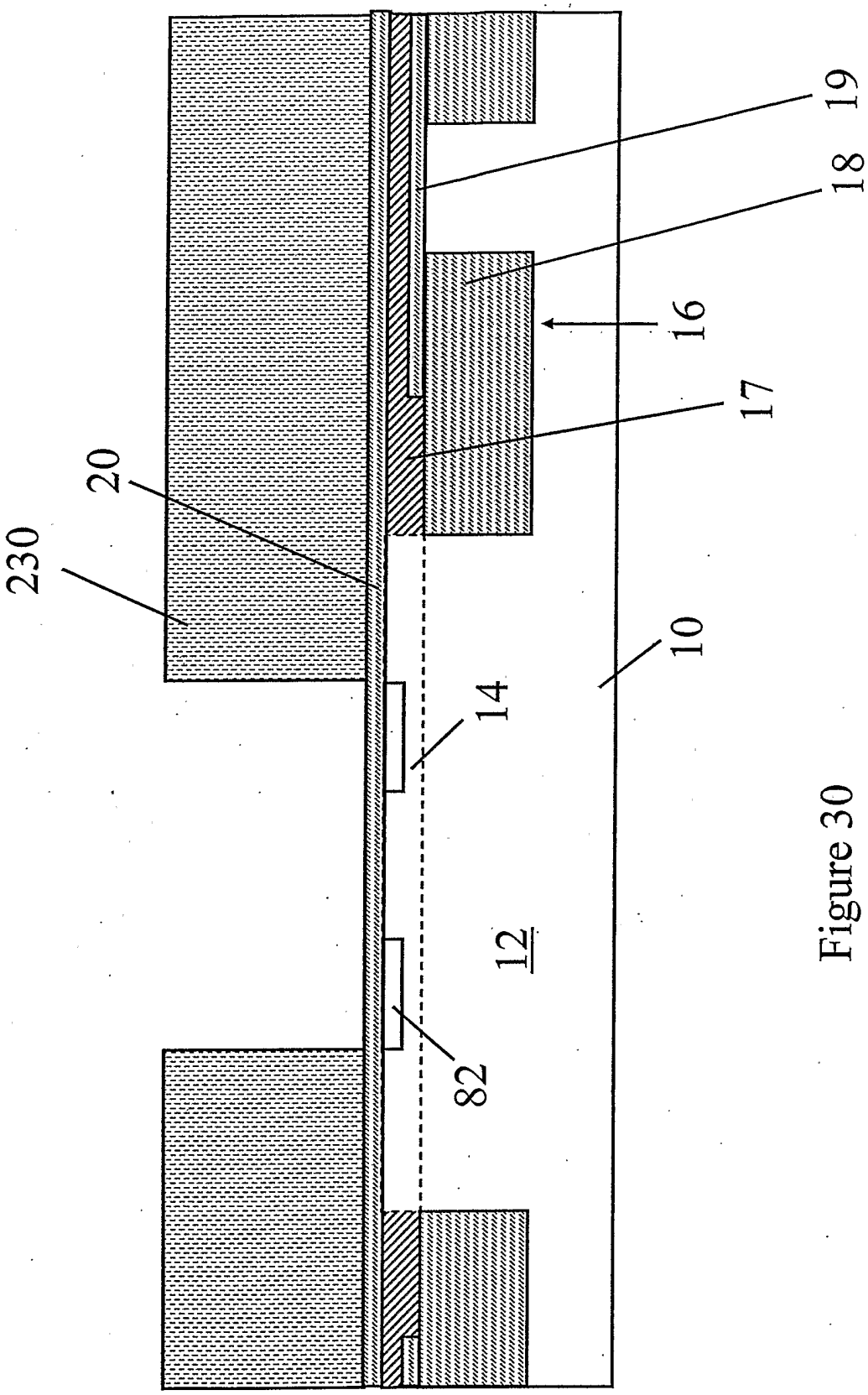


Figure 30

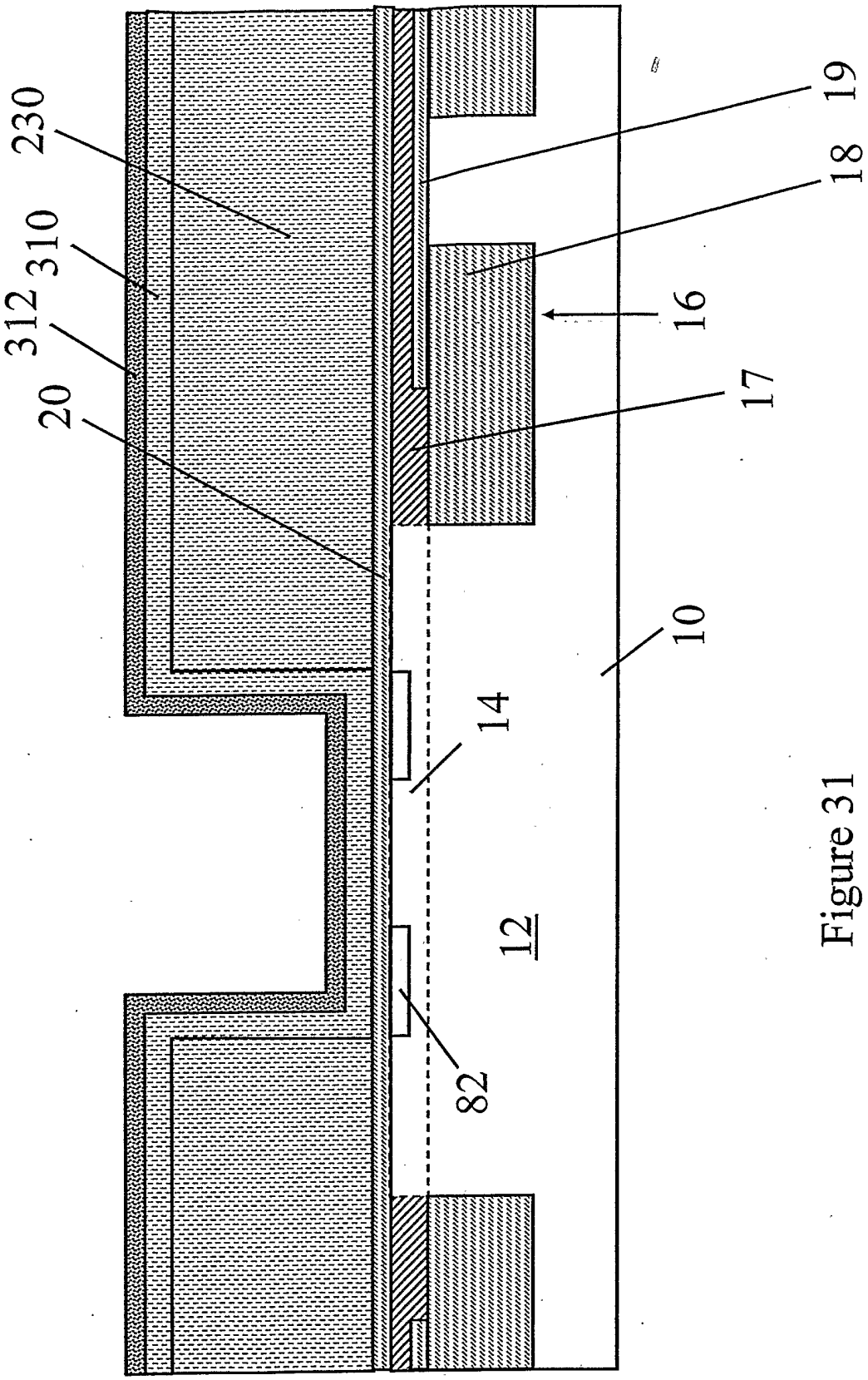


Figure 31

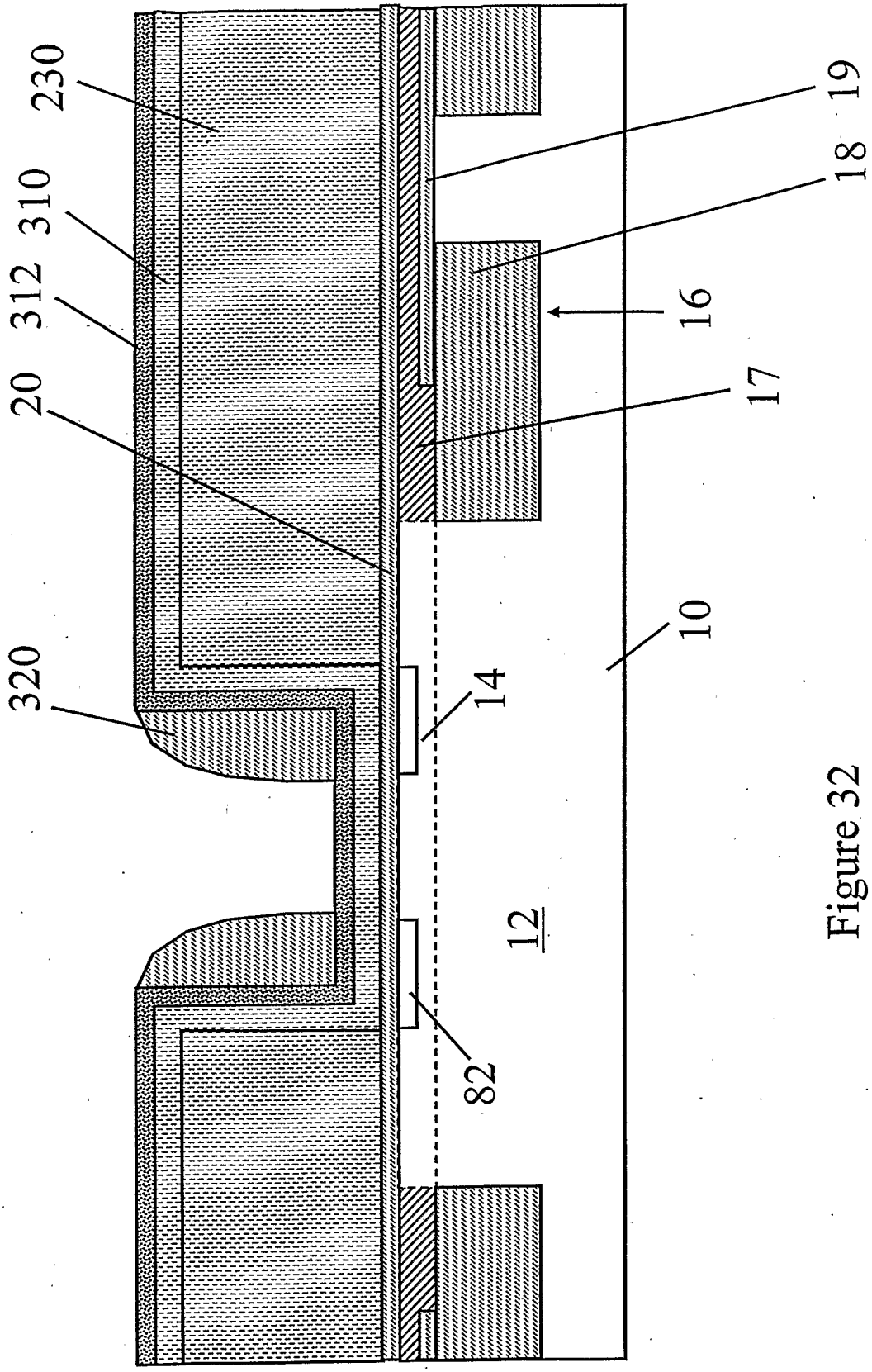


Figure 32

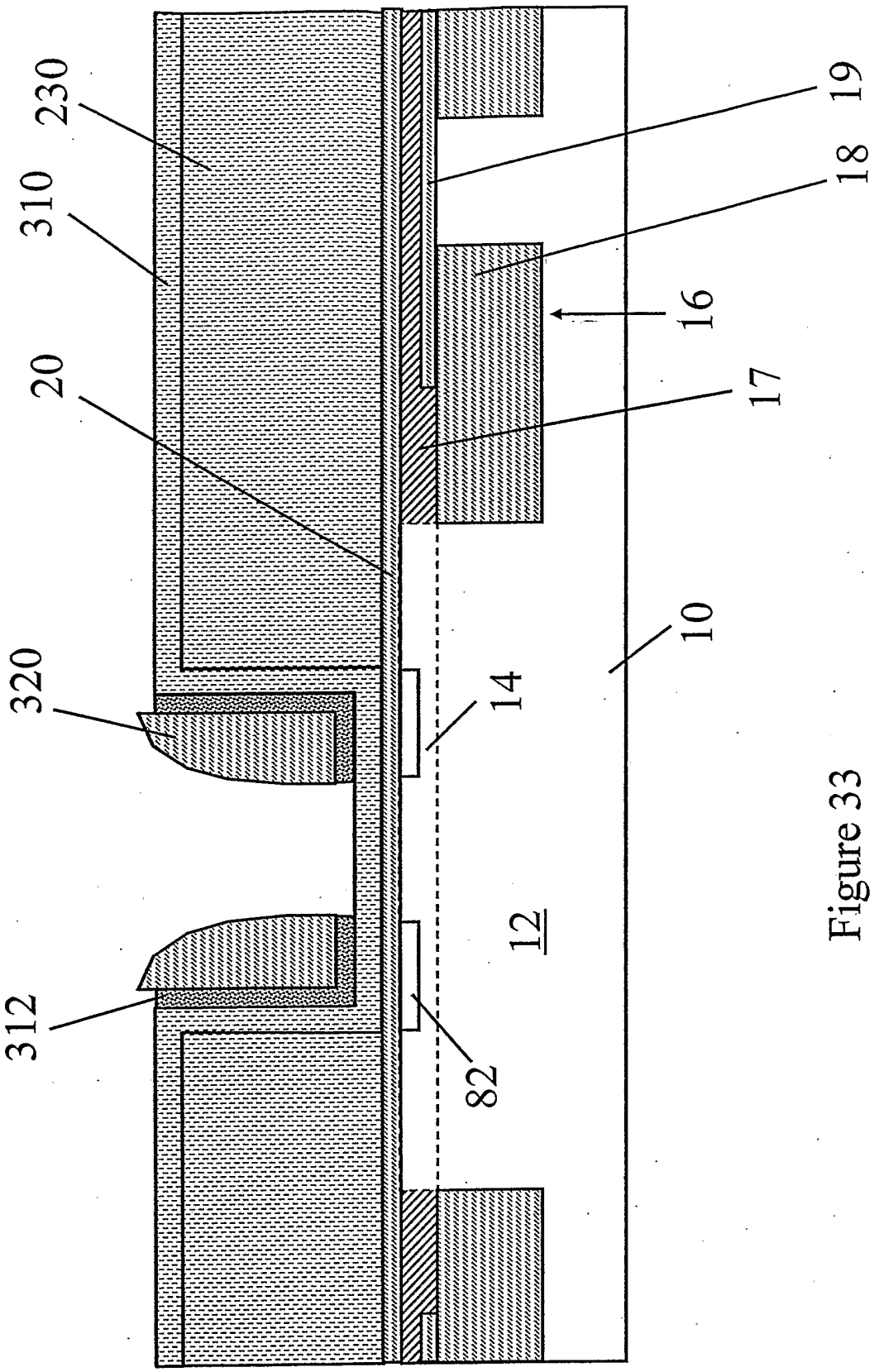


Figure 33

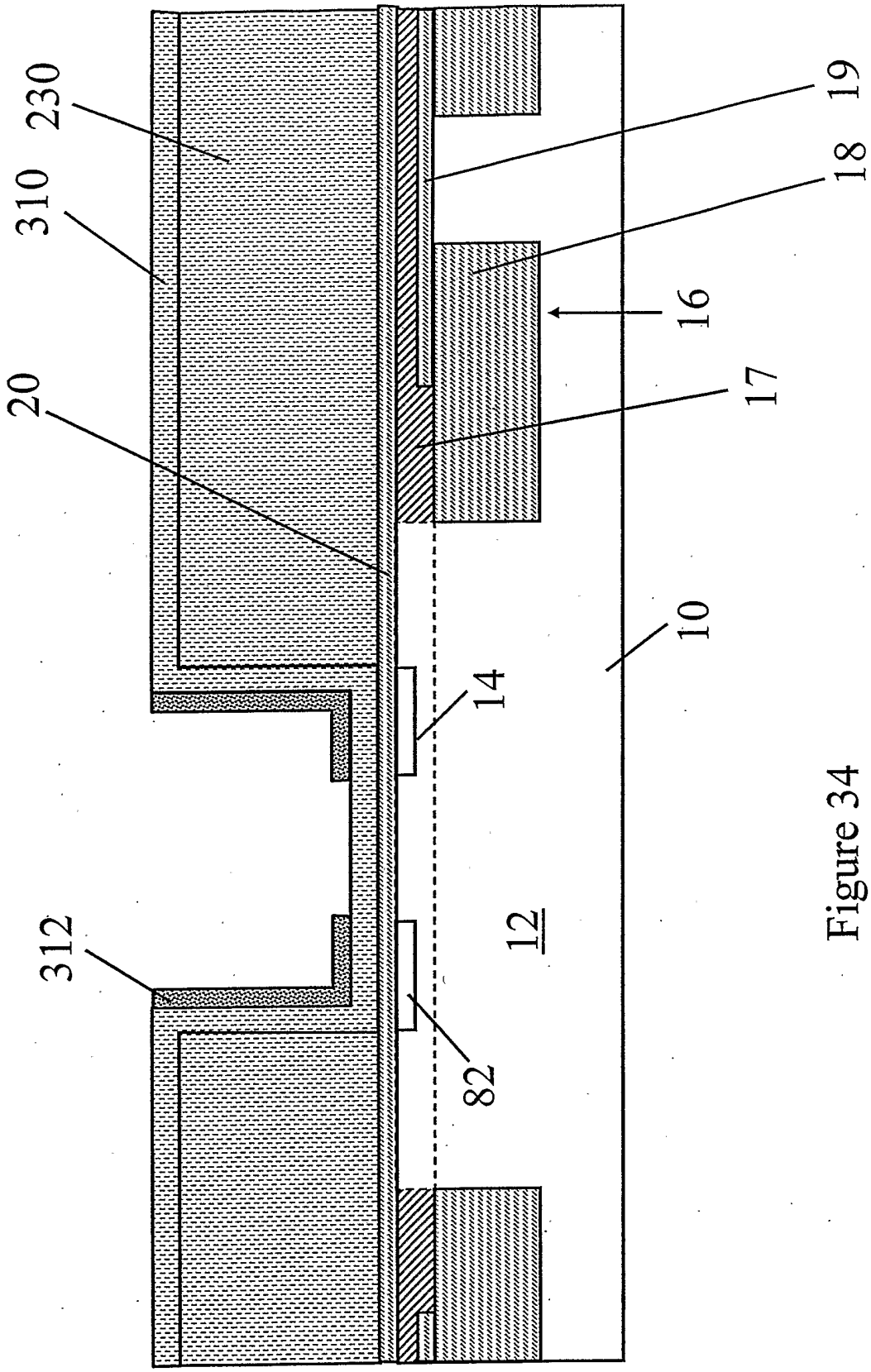


Figure 34

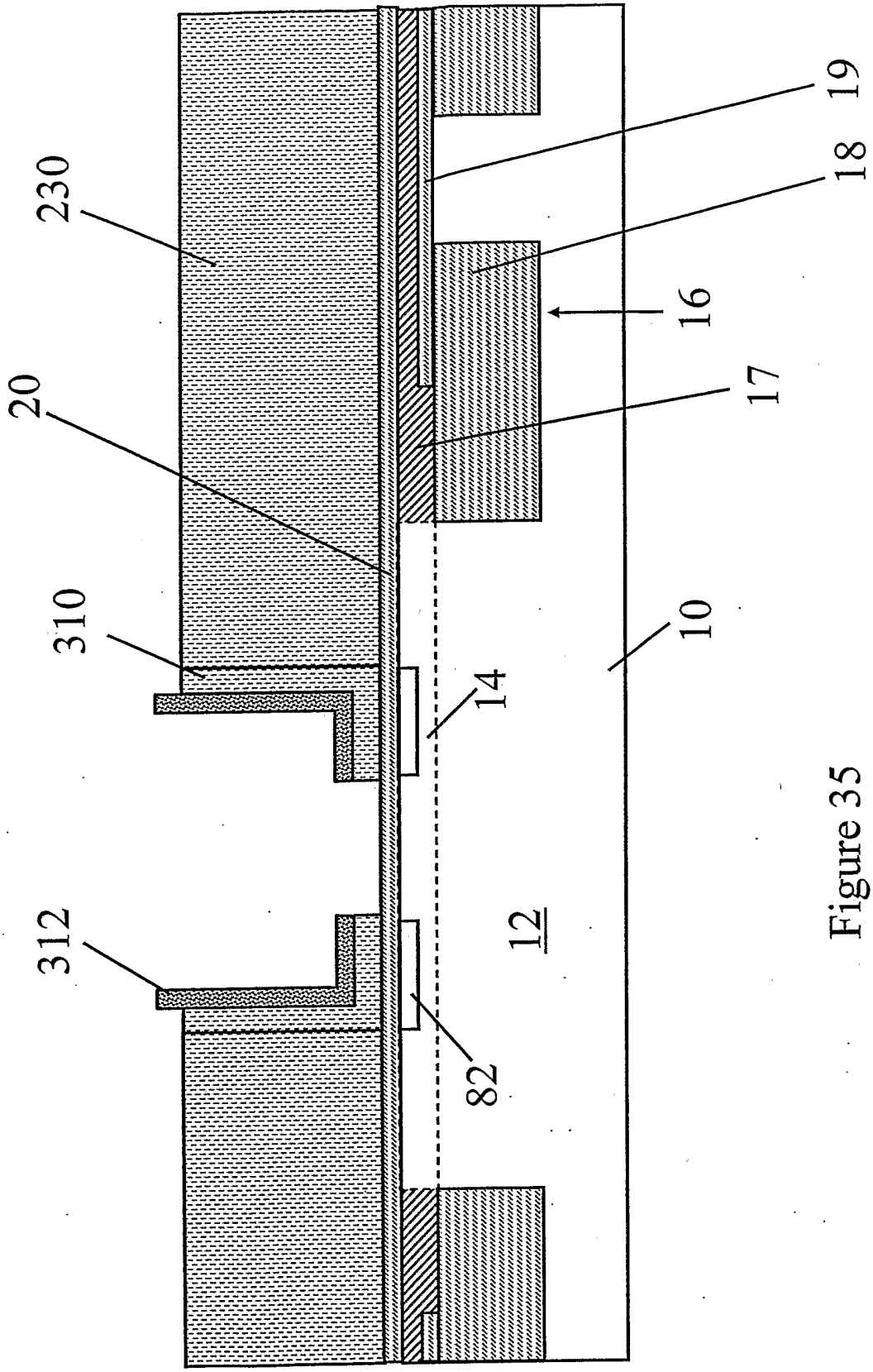


Figure 35

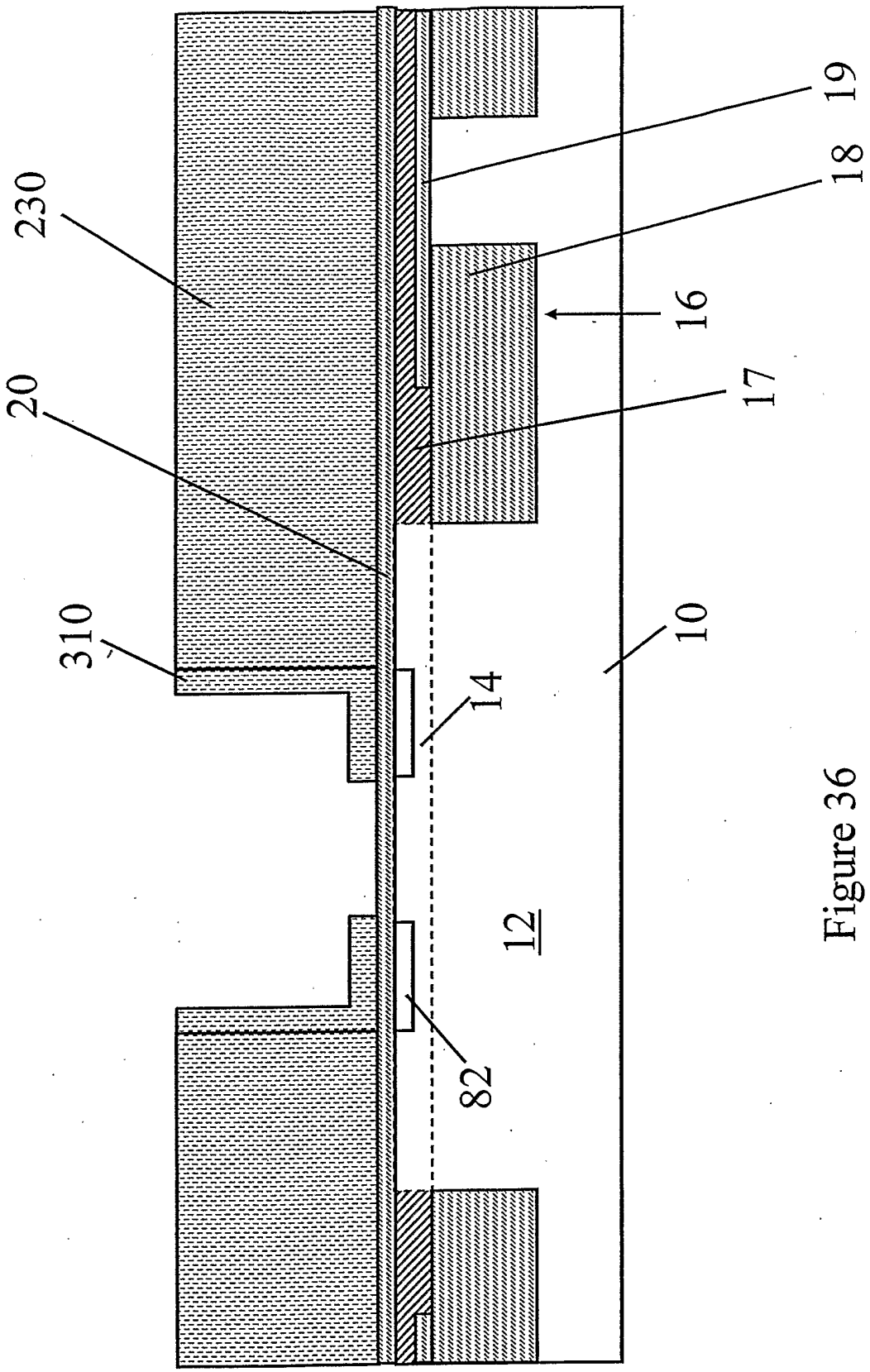


Figure 36

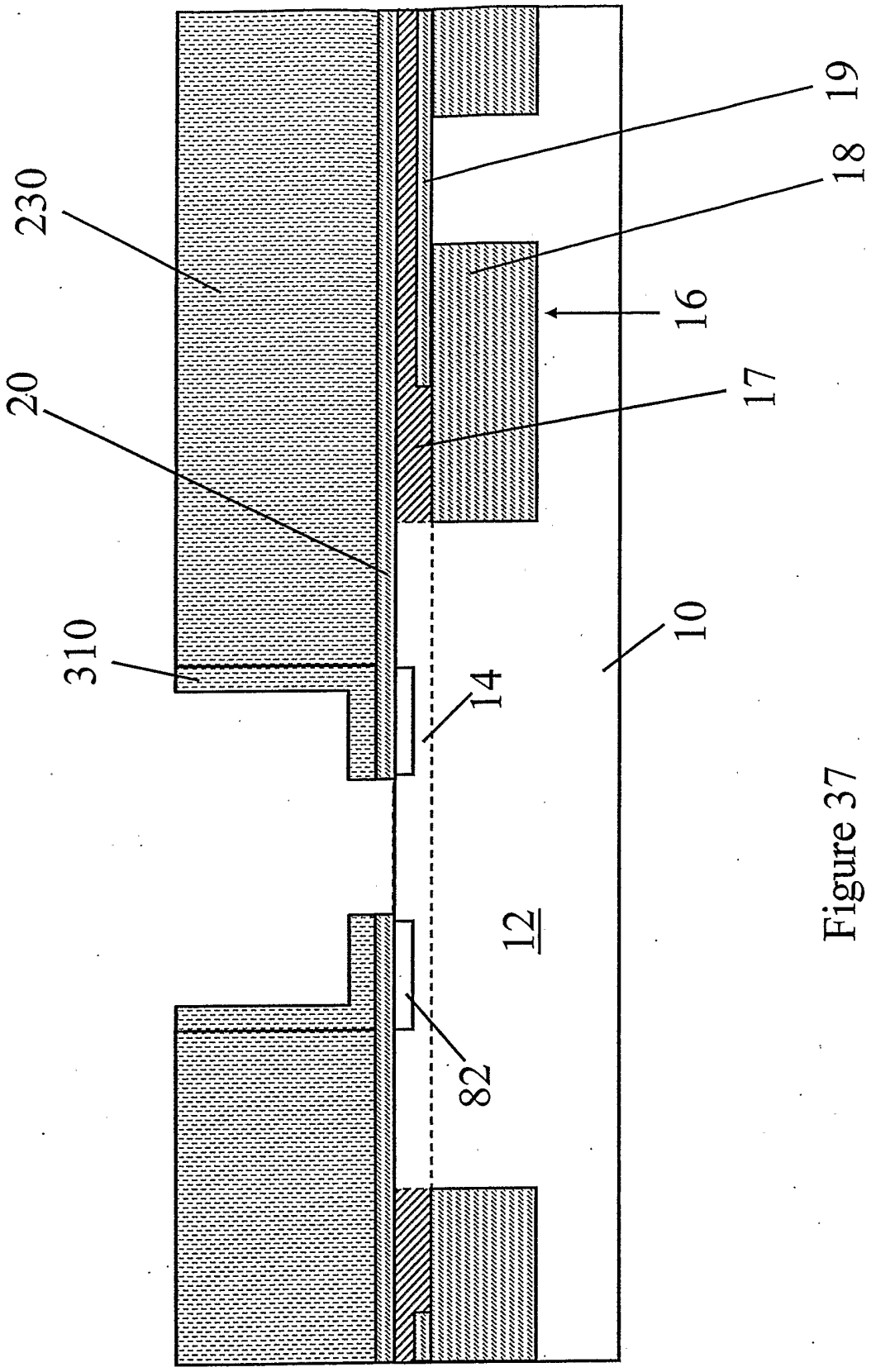


Figure 37

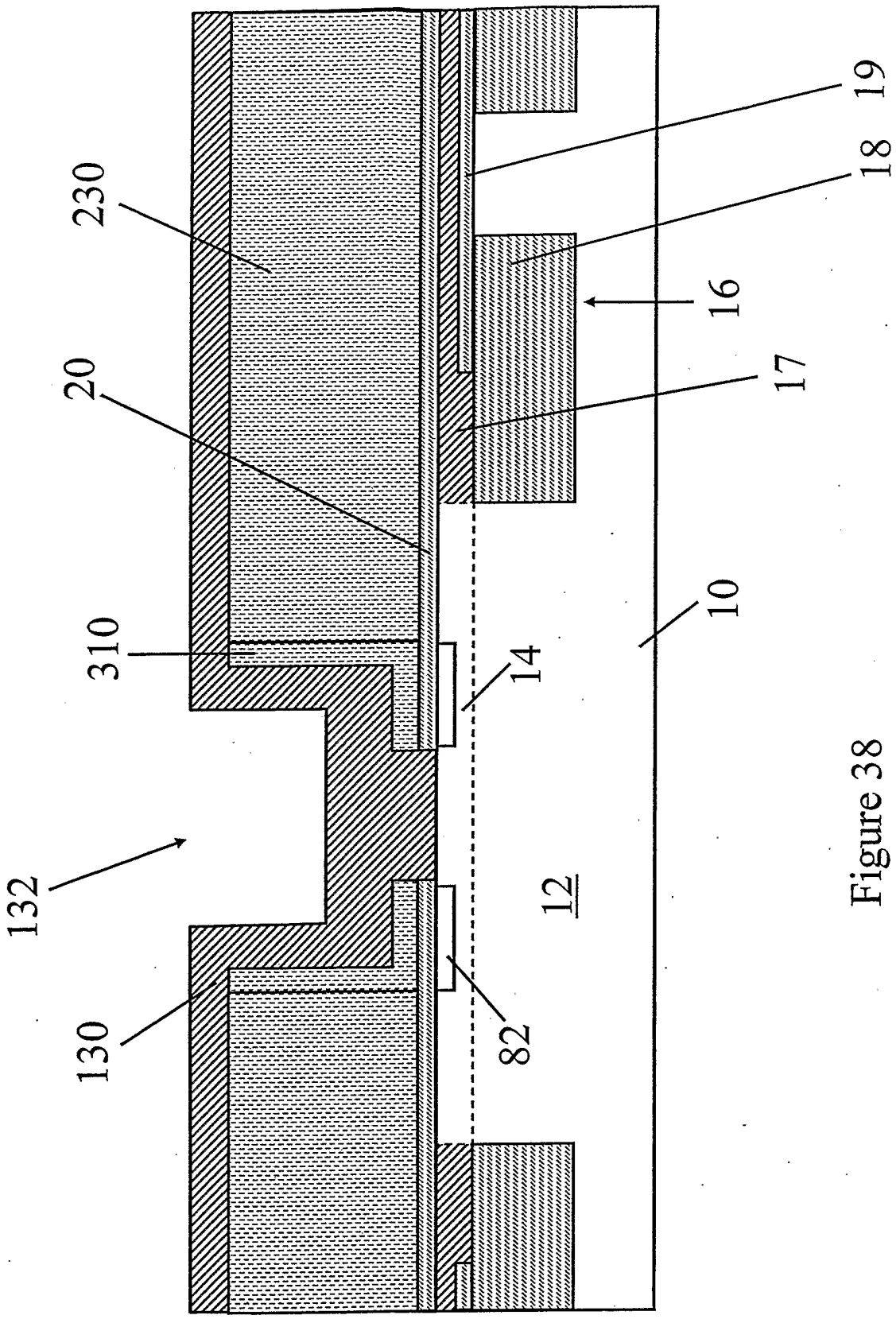


Figure 38

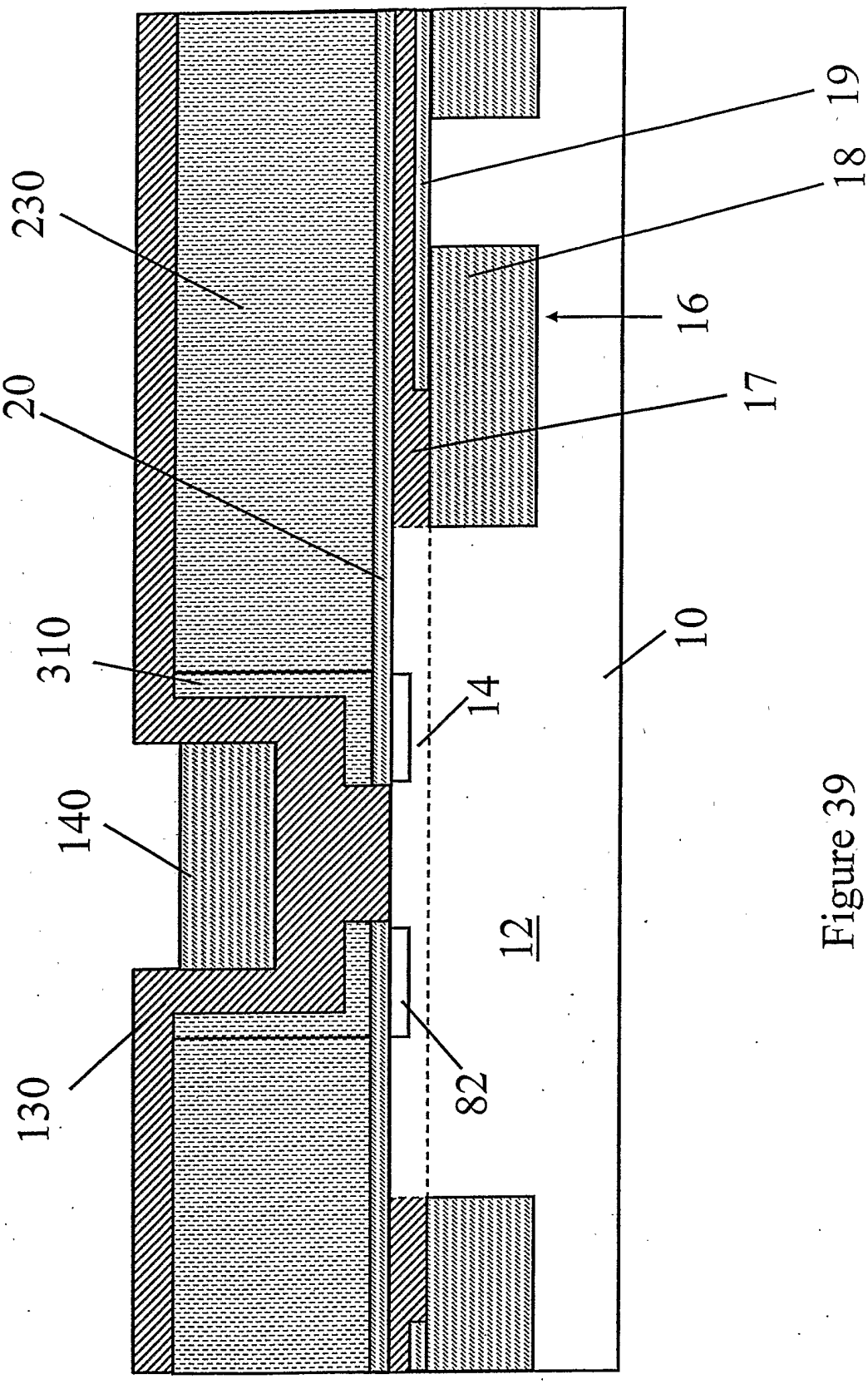


Figure 39

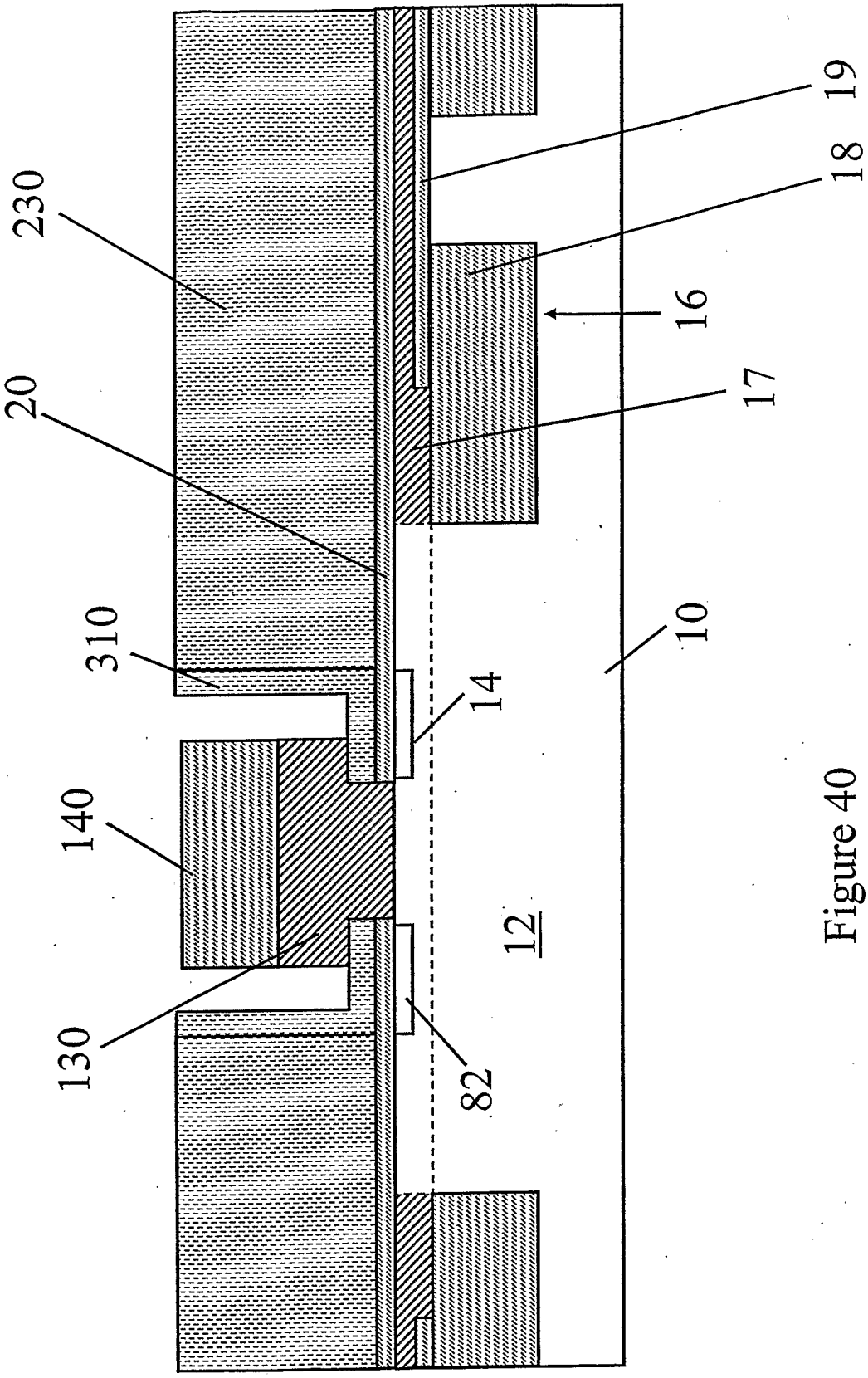


Figure 40

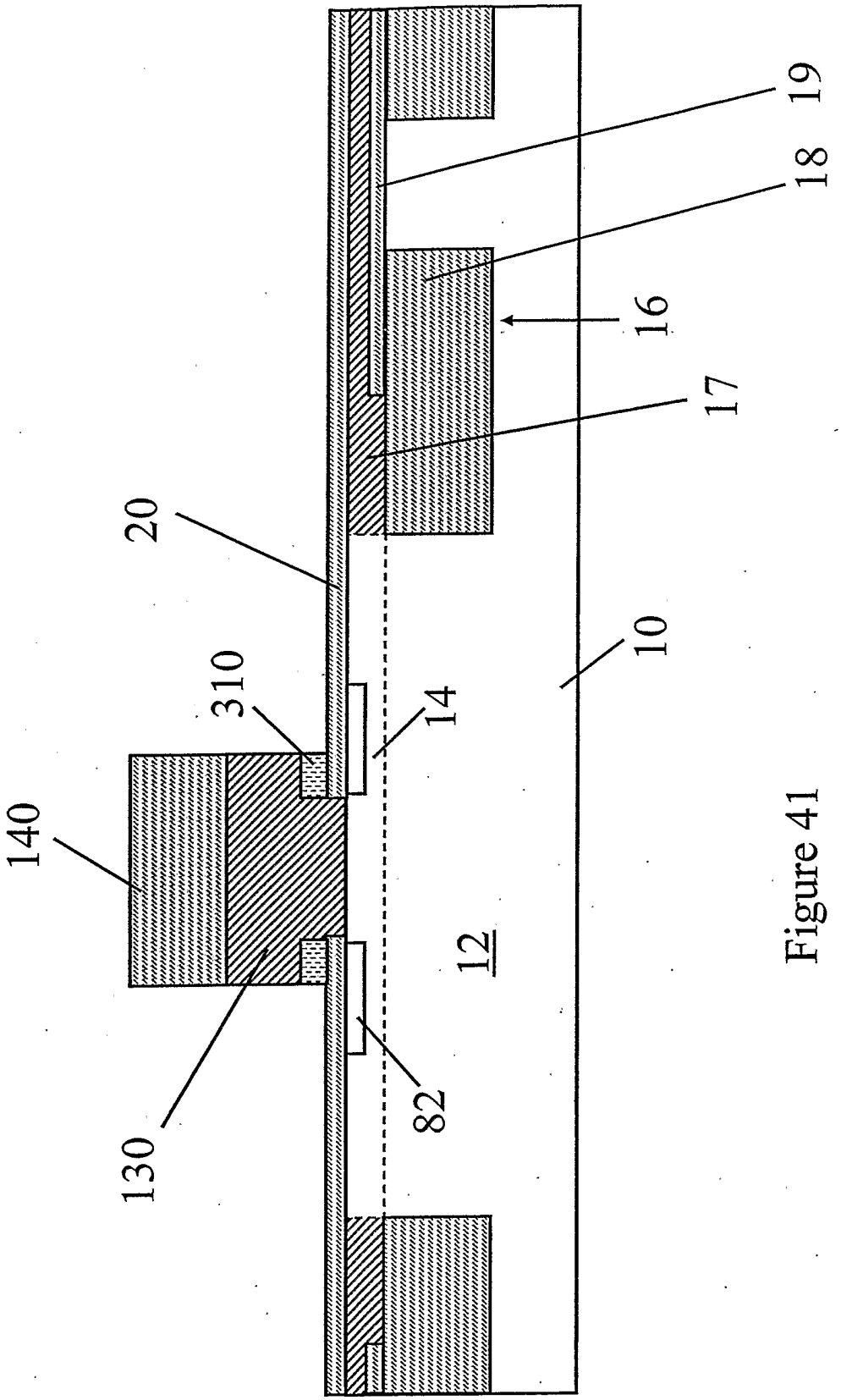


Figure 41

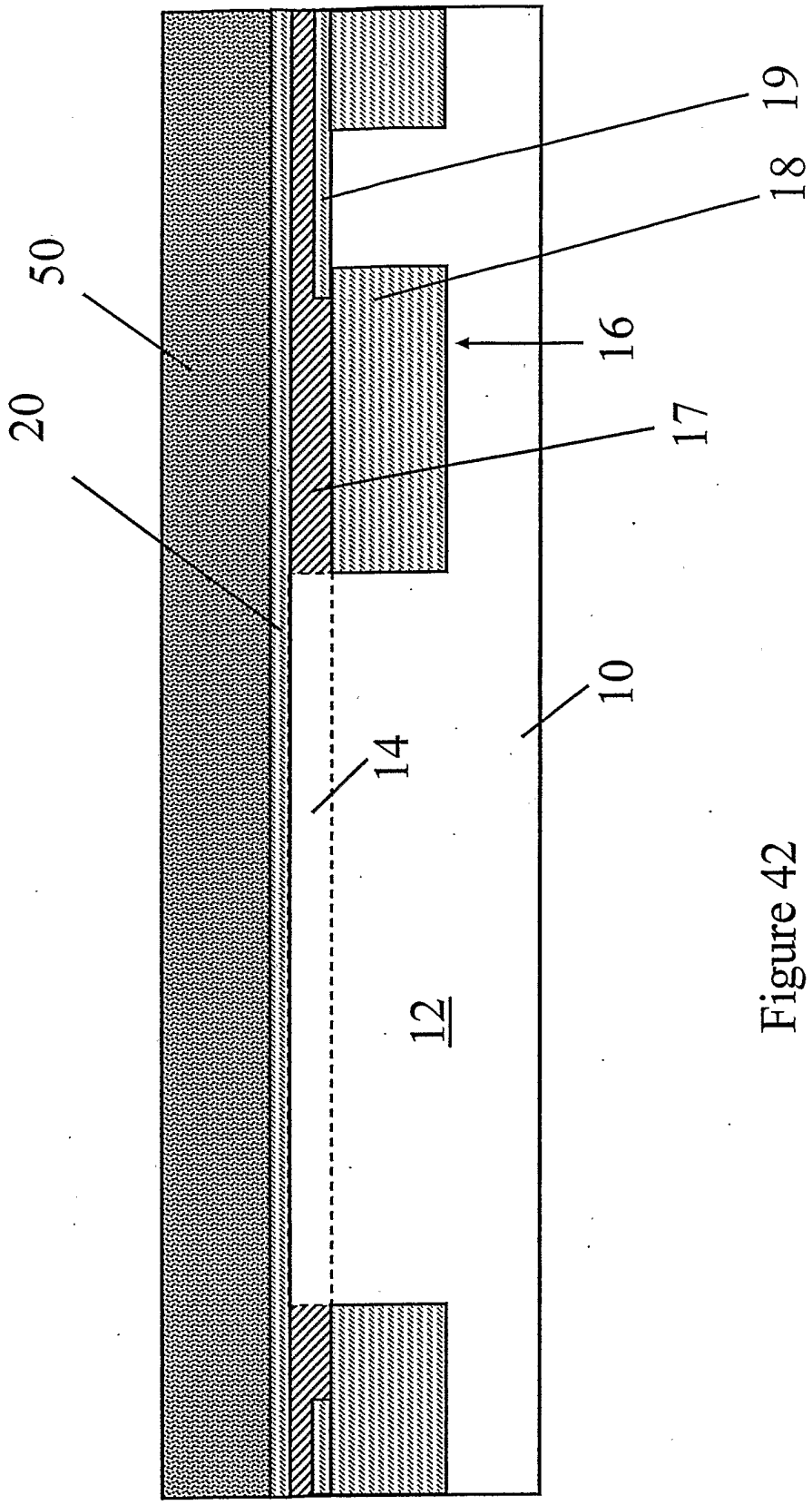


Figure 42

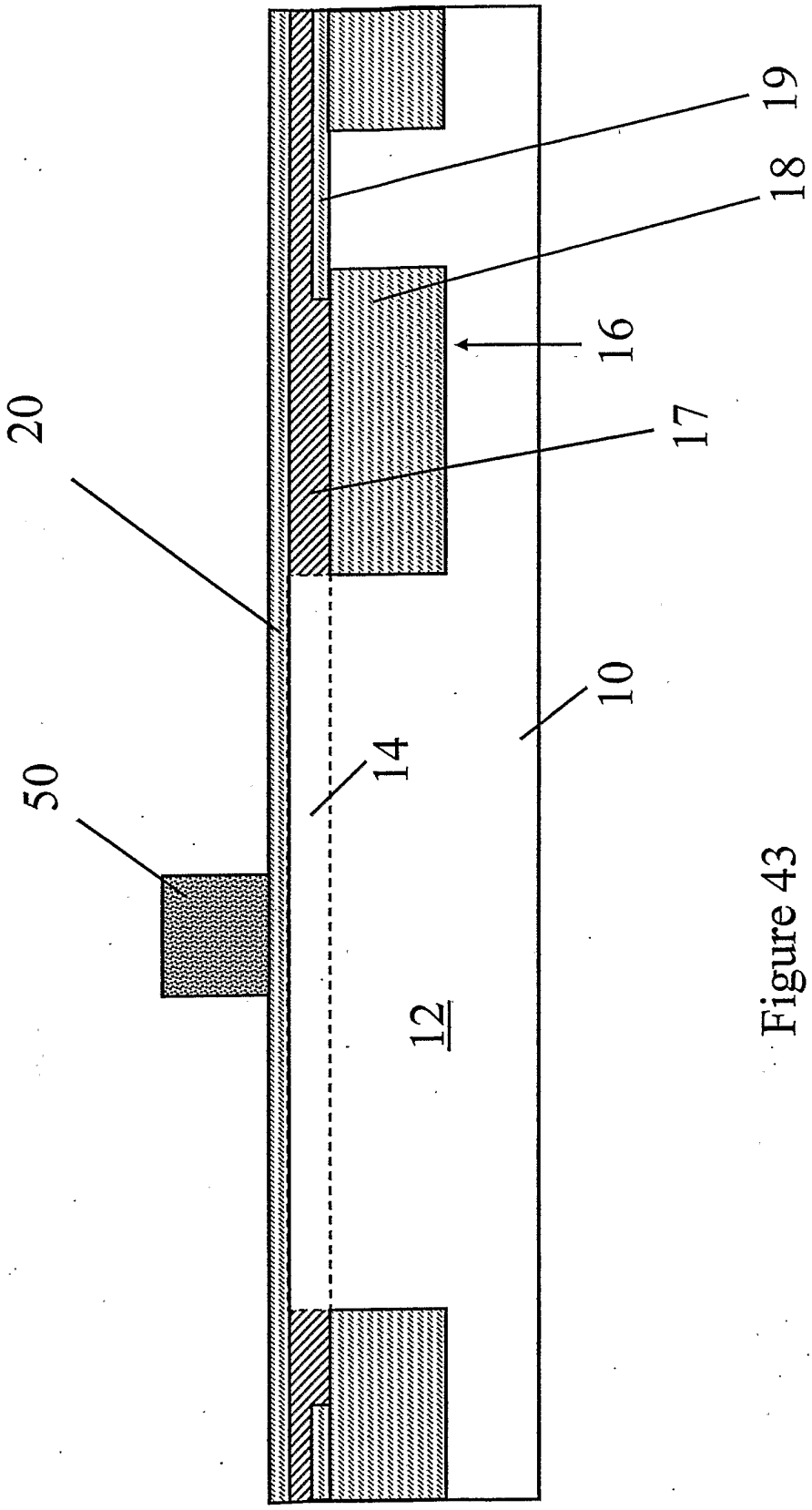


Figure 43

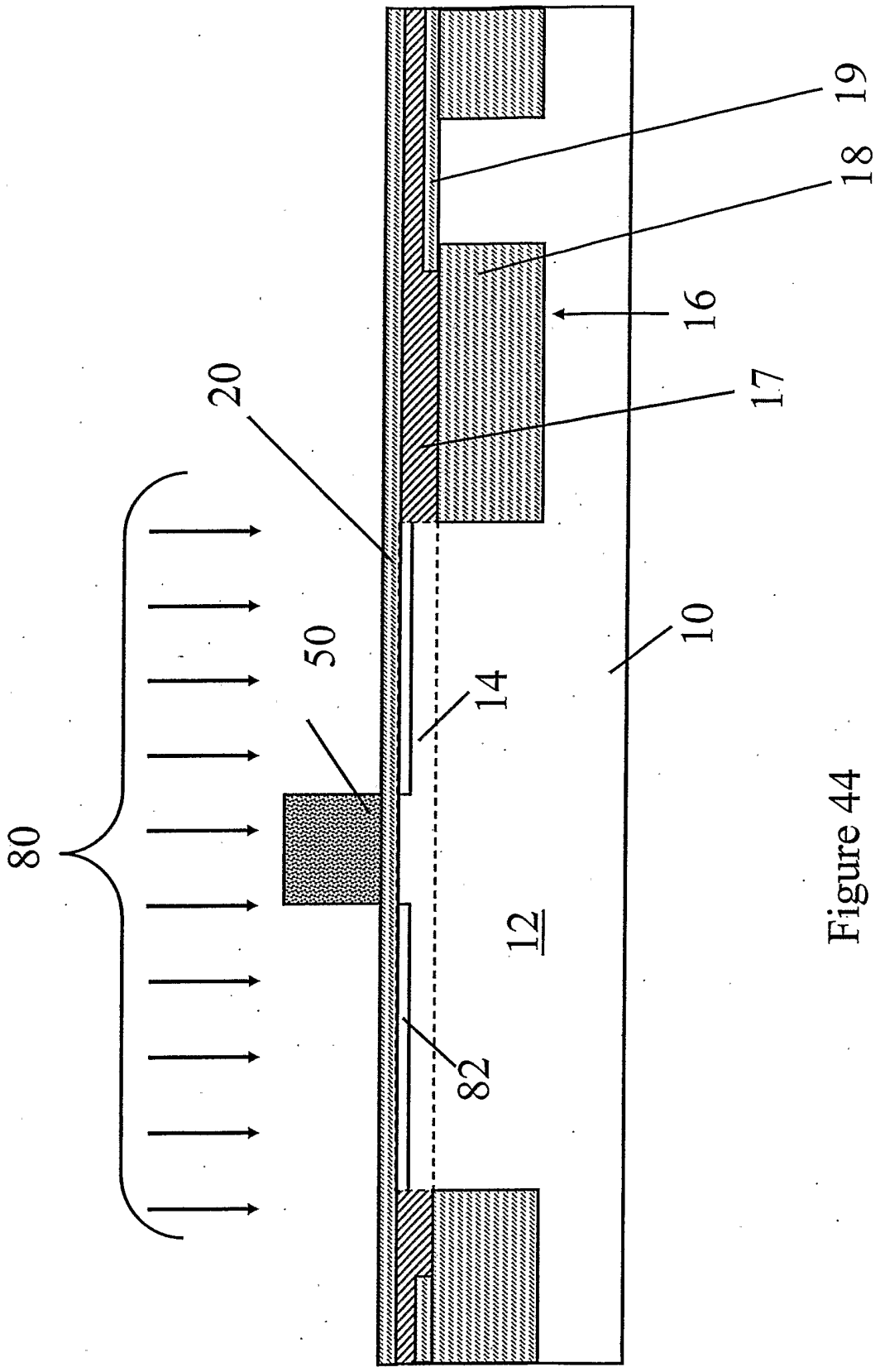


Figure 44

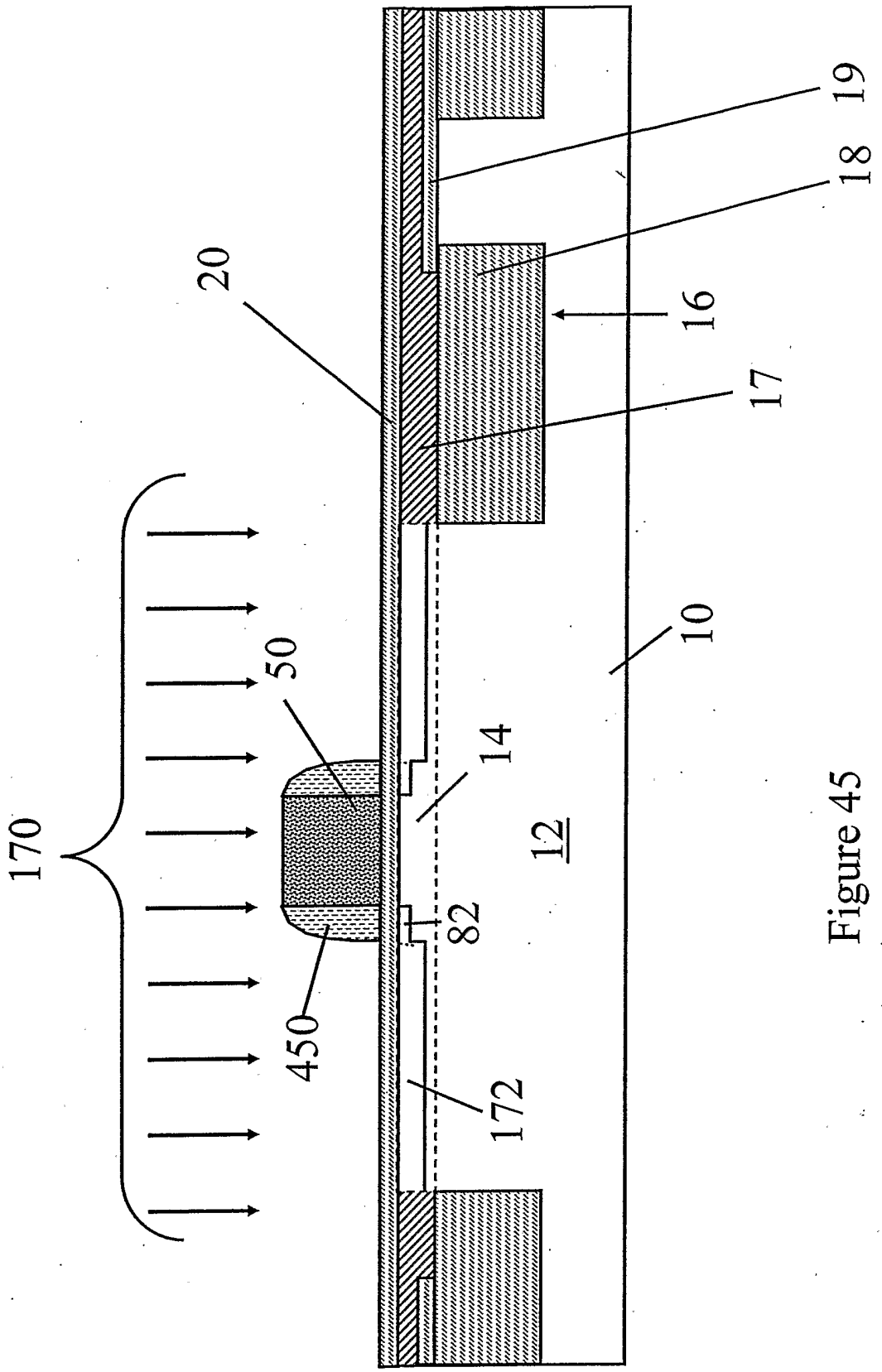


Figure 45

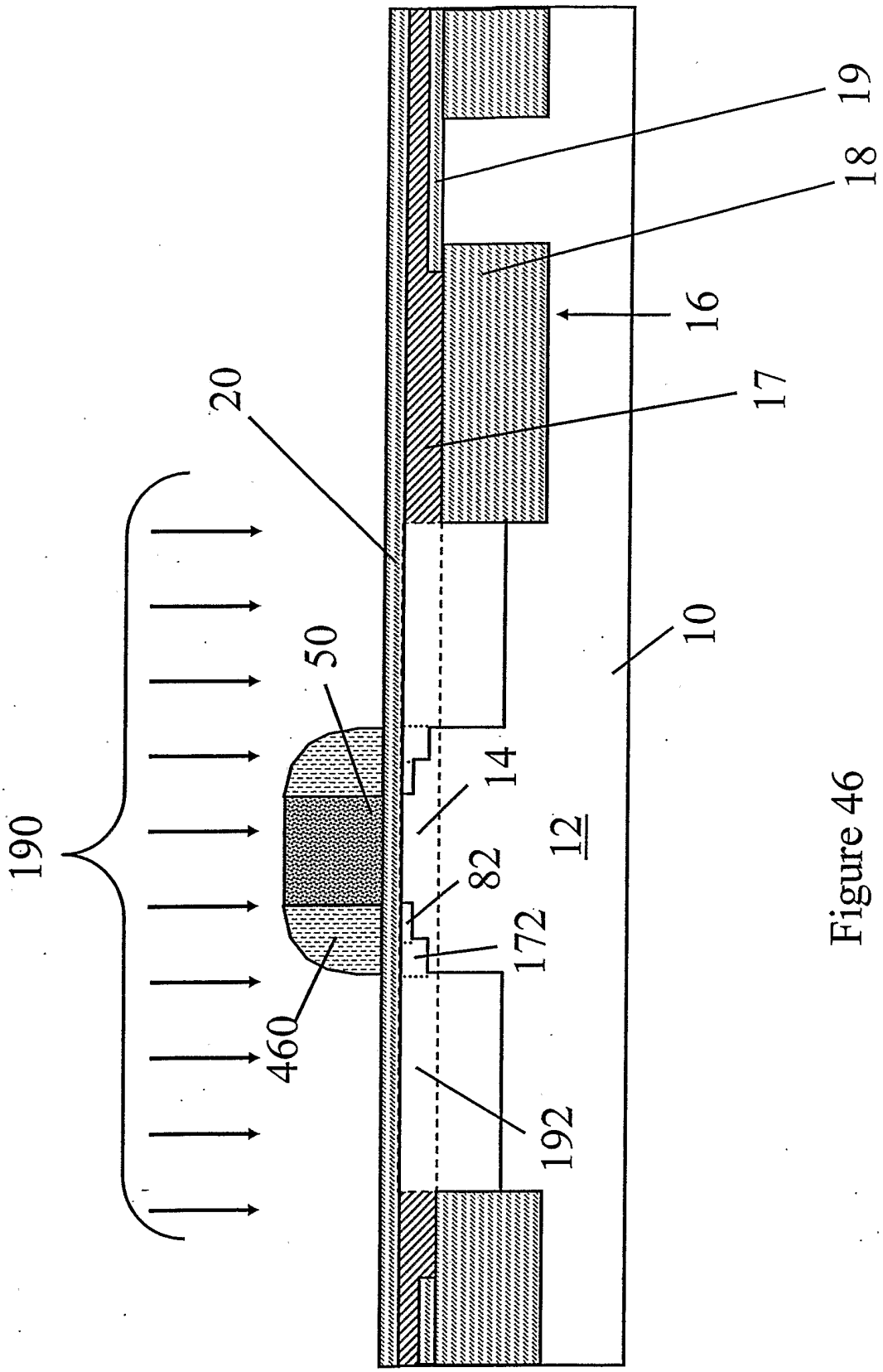


Figure 46

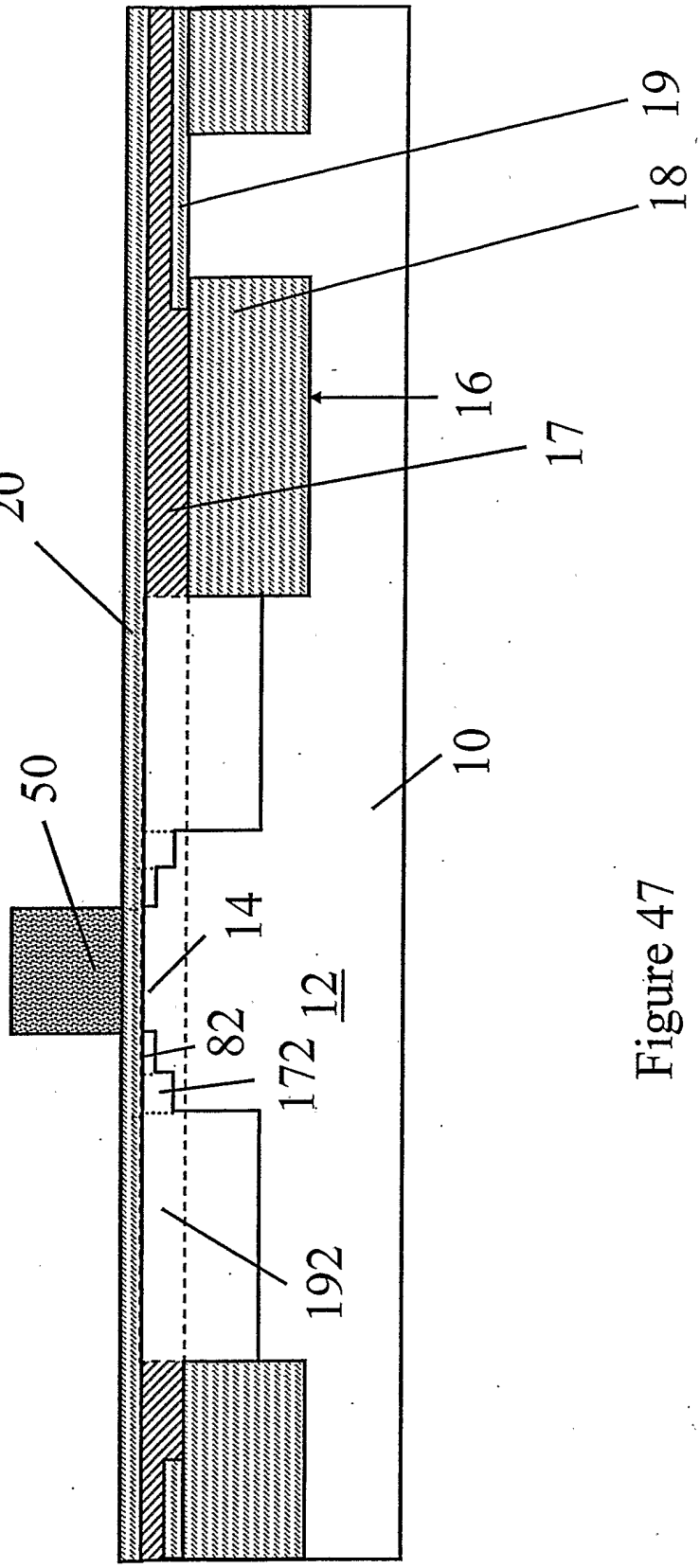


Figure 47

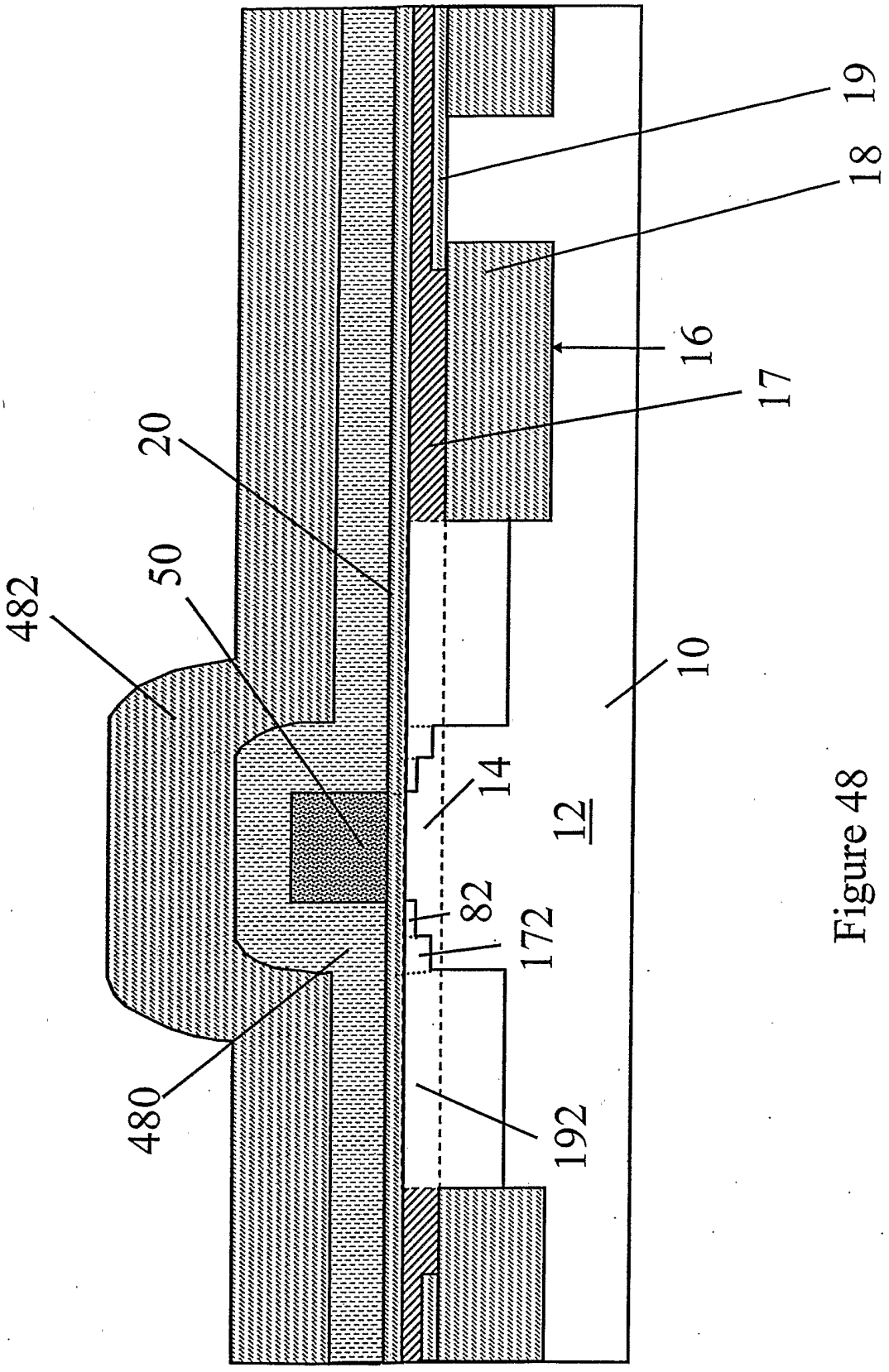


Figure 48

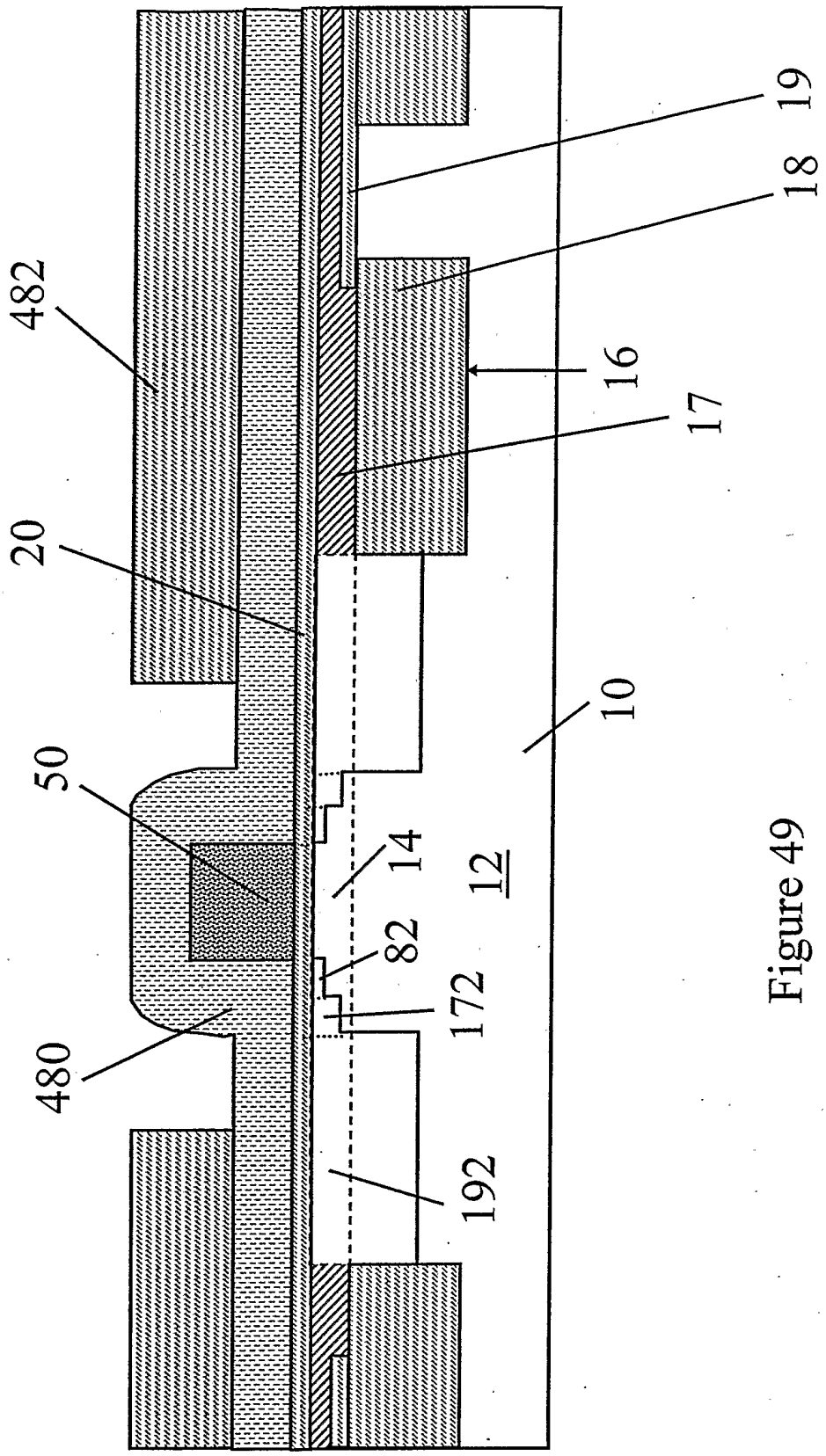


Figure 49

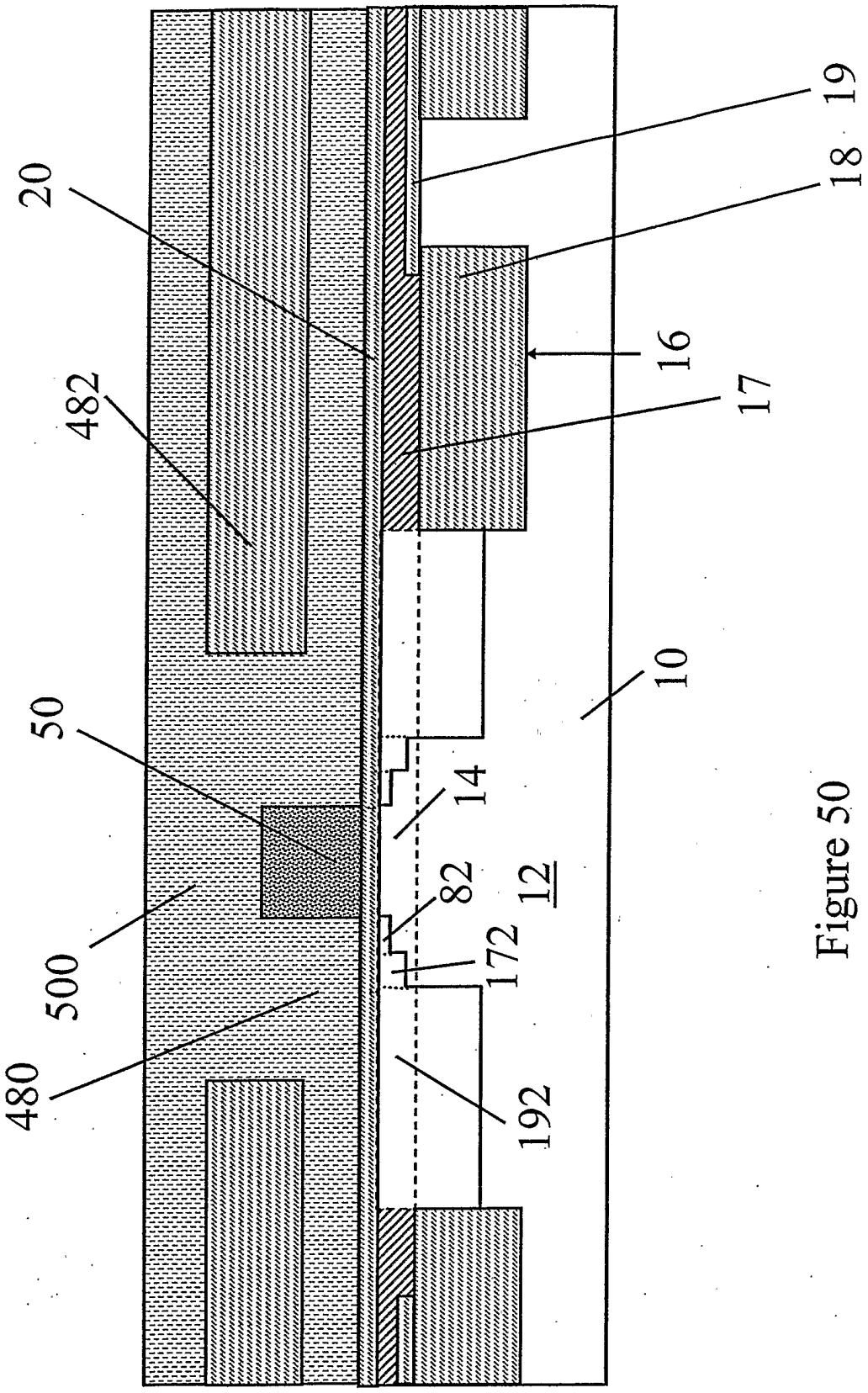


Figure 50

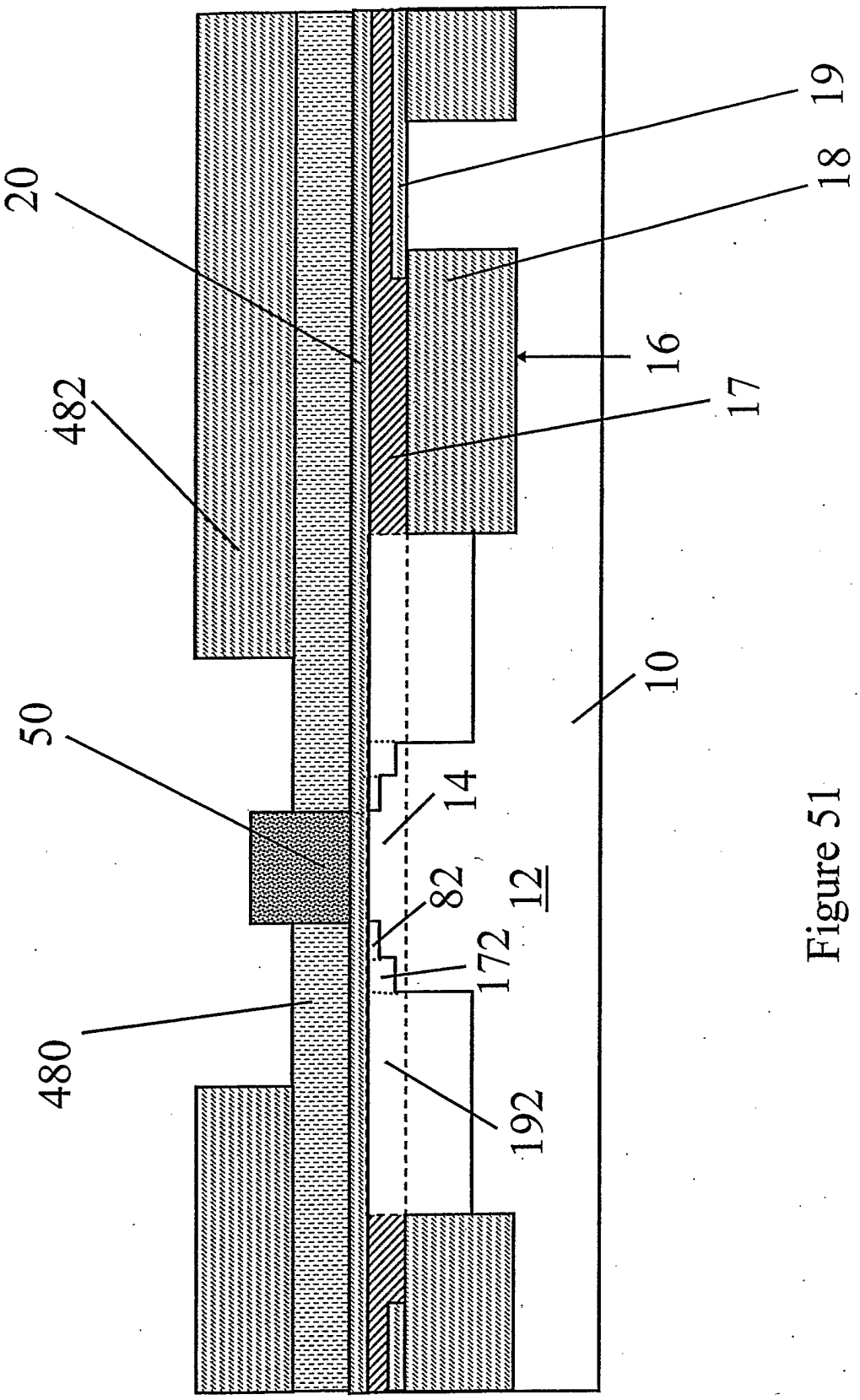


Figure 51

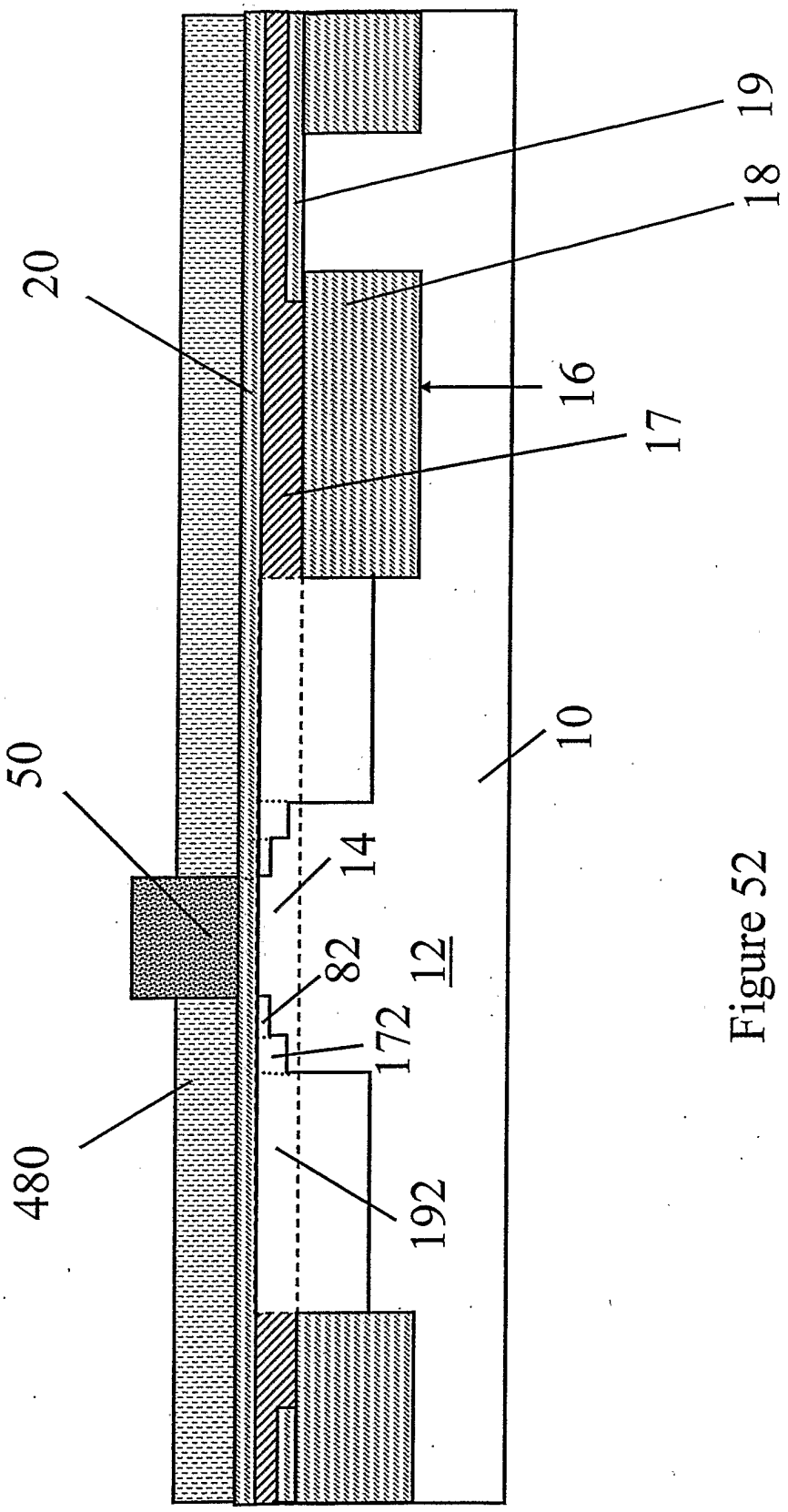


Figure 52

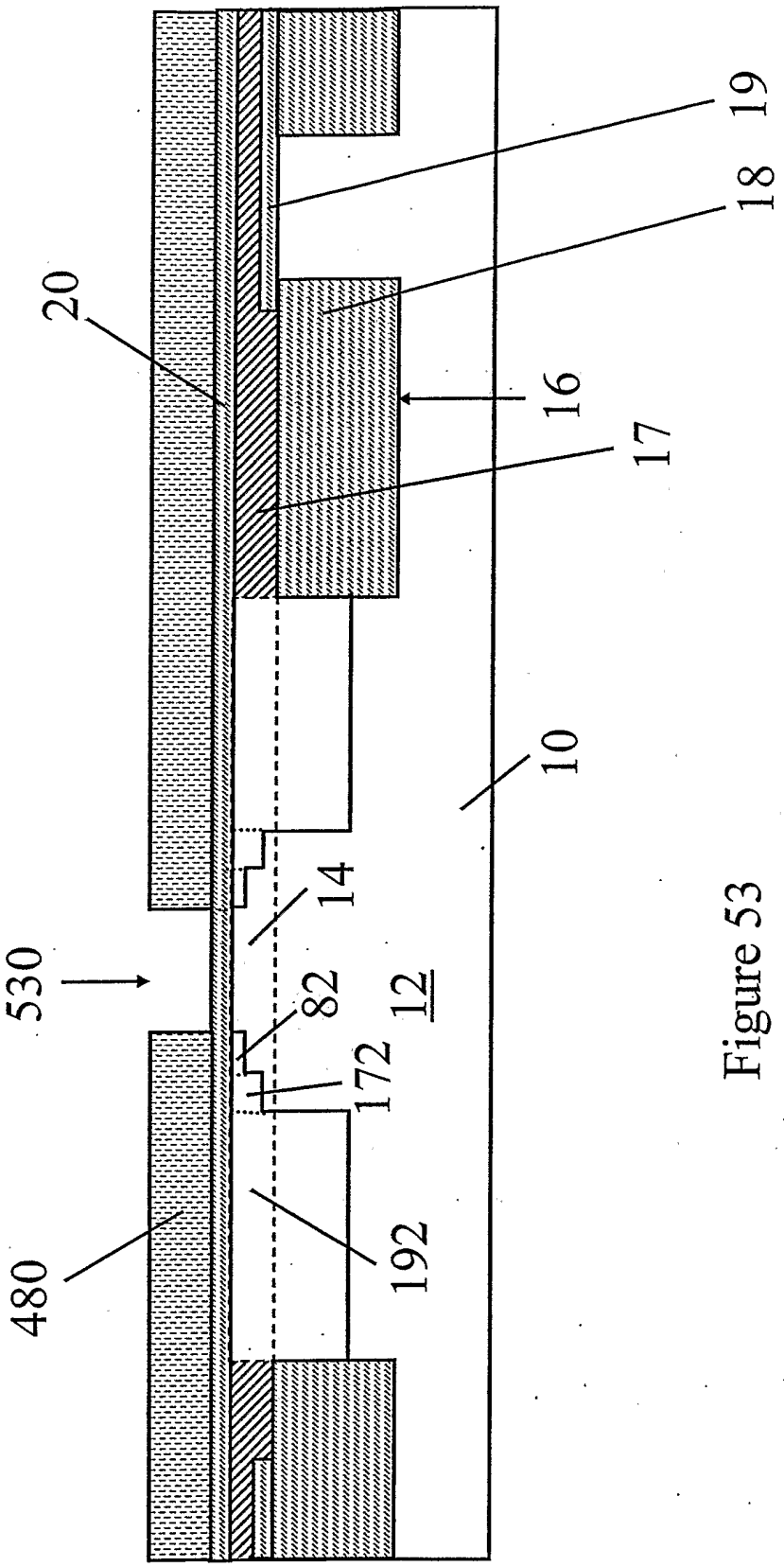


Figure 53

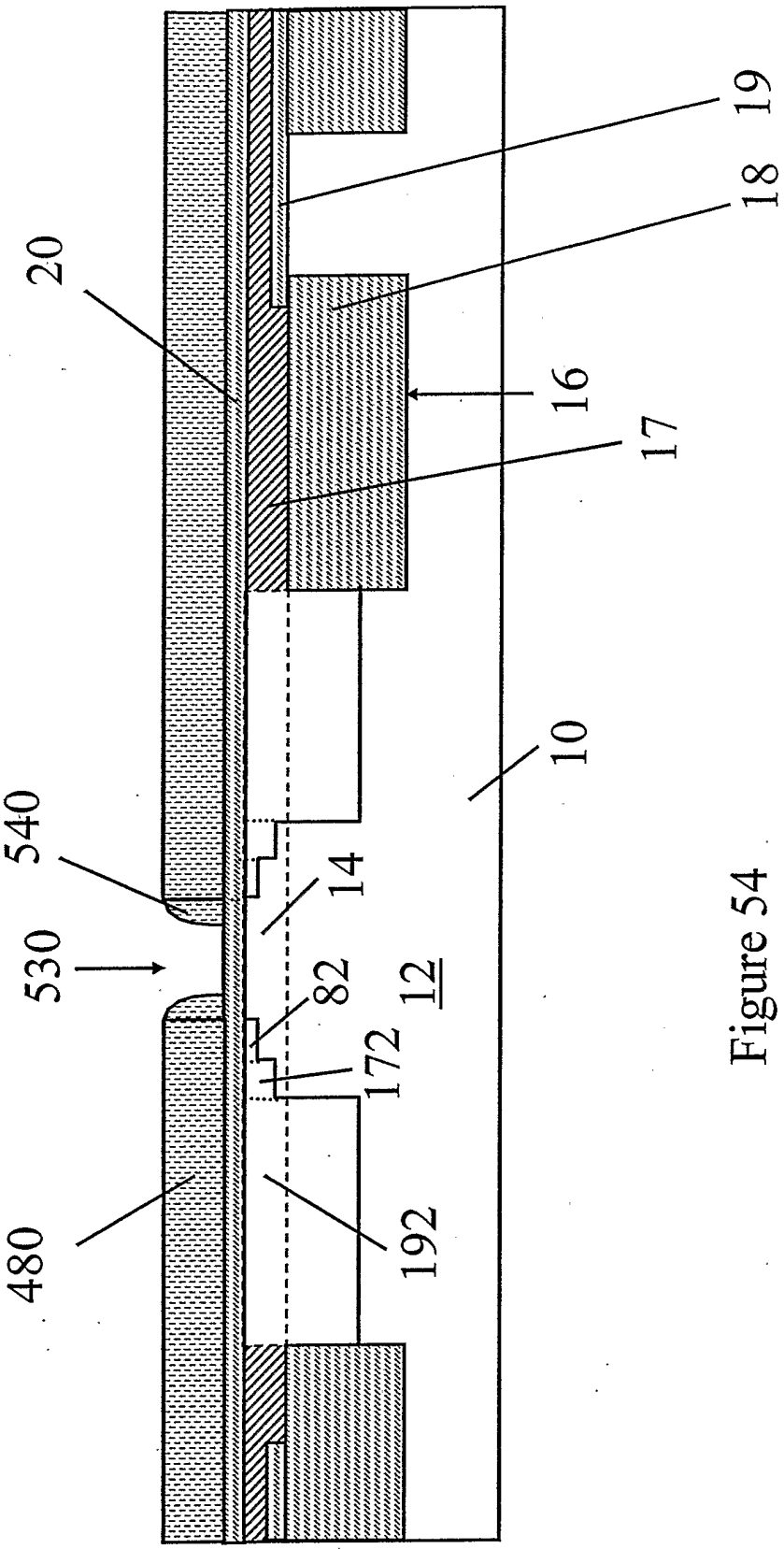


Figure 54

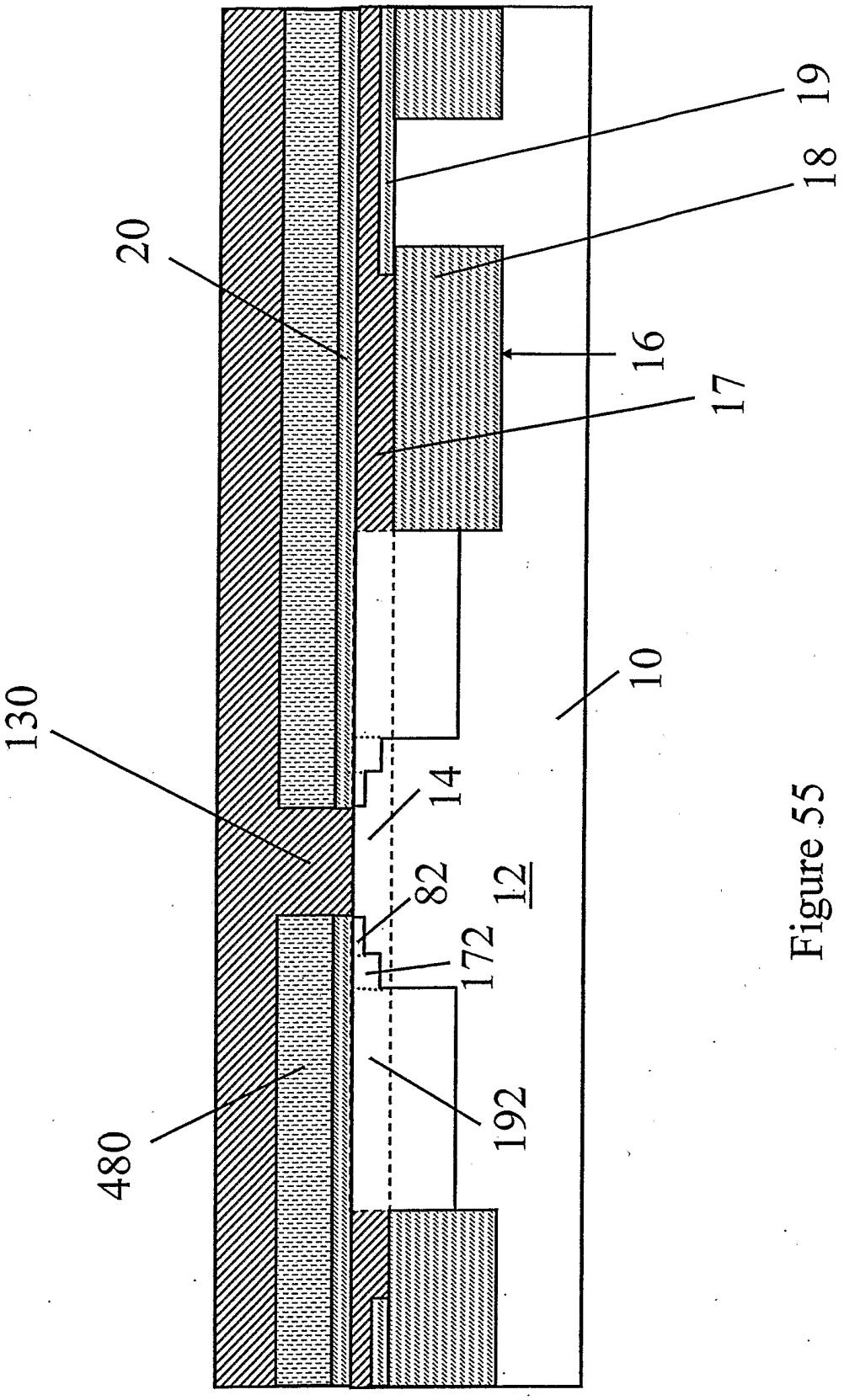


Figure 55

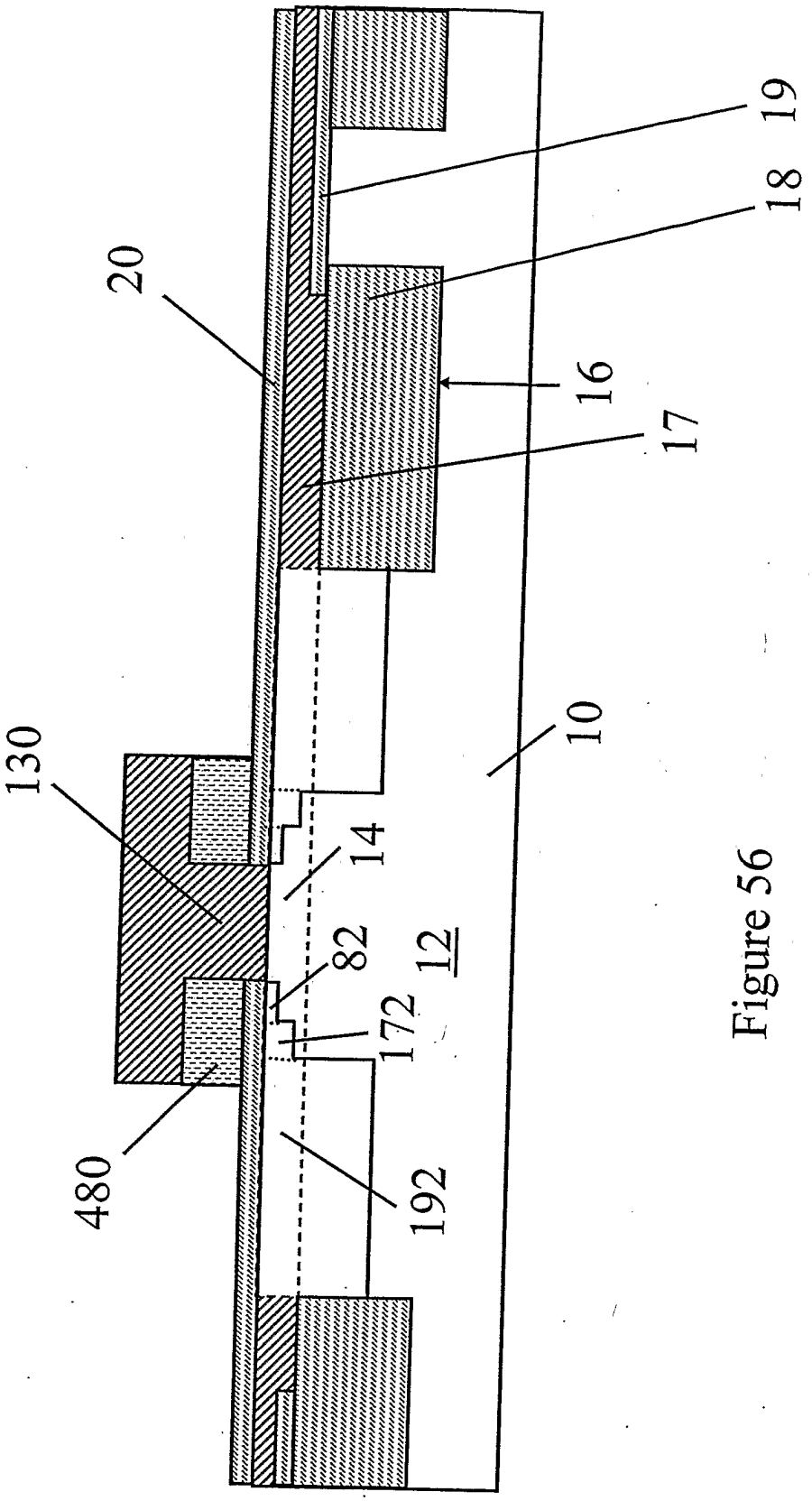


Figure 56

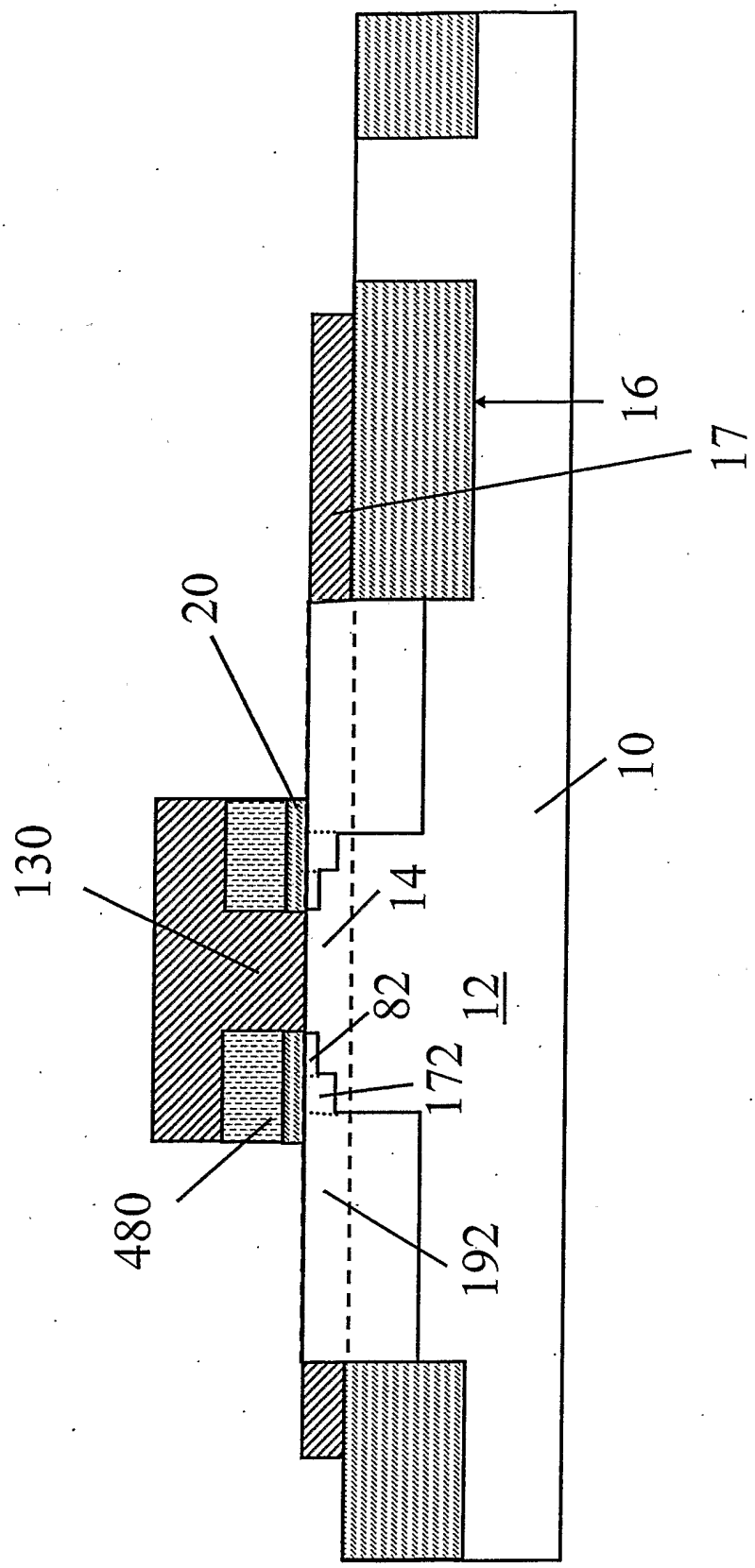


Figure 57

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/41049

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) : H01 L27/082; H01L 21/331
US CL : 257/565; 438/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/565; 438/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
x	US 6,551,891 (Chantre et al.) 22 April 2003 (22.04.2003), column 2, lines 21-25, column 3, lines 3-7, figure. 12	1-15
A	US 6,846,710 (Yi et al.) 25, Januray 2005 (25.01.05)	1-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
08 February 2006 (08.02.2006)

Date of mailing of the international search report
08 MAR 2006

Name and mailing address of the ISA/US
Mail Stop PCT, Attn: ISA/US
Commissioner of Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
Facsimile No. (571) 273-3201

Authorized officer
Zandra V Smith

Telephone No. (571) 272 ****

Form PCT/ISA/210 (second sheet) (July 1998)