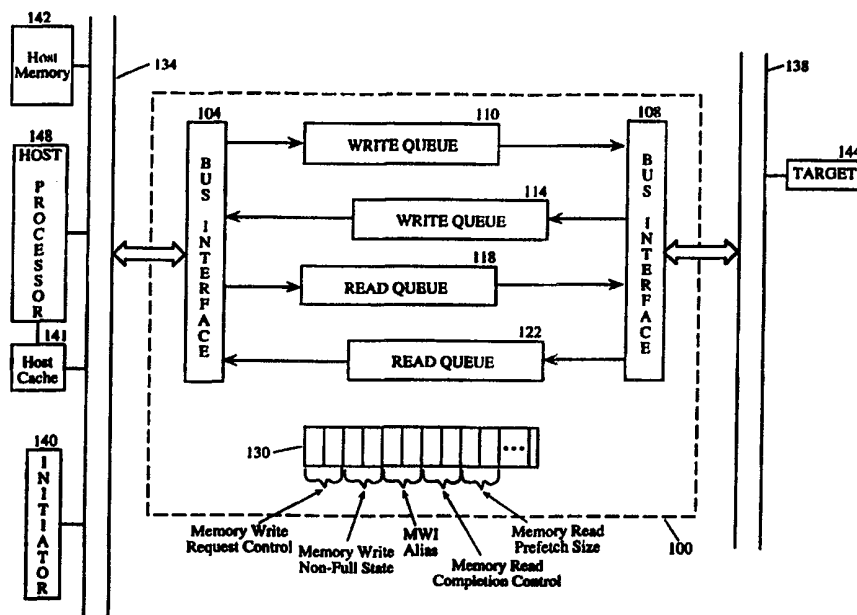




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(54) Title: TRIGGER POINTS FOR PERFORMANCE OPTIMIZATION IN BRIDGES



(57) Abstract

Method and apparatus for tuning the performance of bridge devices (100), including PCI-to-PCI bridges as well as PCI local bus bridges (or host bridges). The embodiments of the invention permit a multiple-bus computer system to be tuned in view of the application and the bridge queue sizes. Such applications include those concerned with raw bandwidth (such as disk storage), and those that are sensitive to latency (such as networking and videoconferencing). The embodiments of the invention feature a control register (130) that specifies storage conditions to be met by the read and write queues (110, 114, 118, 120) of the bridge (100). The programmed storage conditions are trigger points which cause the bridge (100) to transfer data into or remove data from the queues (110, 114, 118, 120) during read and write transactions in order to promote the performance desired from the bridge (100).

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

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US CL : 710/129

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 710/129, 126, 128, 130, 52

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
STN

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P	US 5,732,094 A (PETERSEN et al) 24 March 1998, col. 2-4 and figure 2.	1-23

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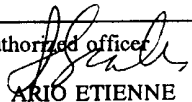
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