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(72) **Inventors; and**

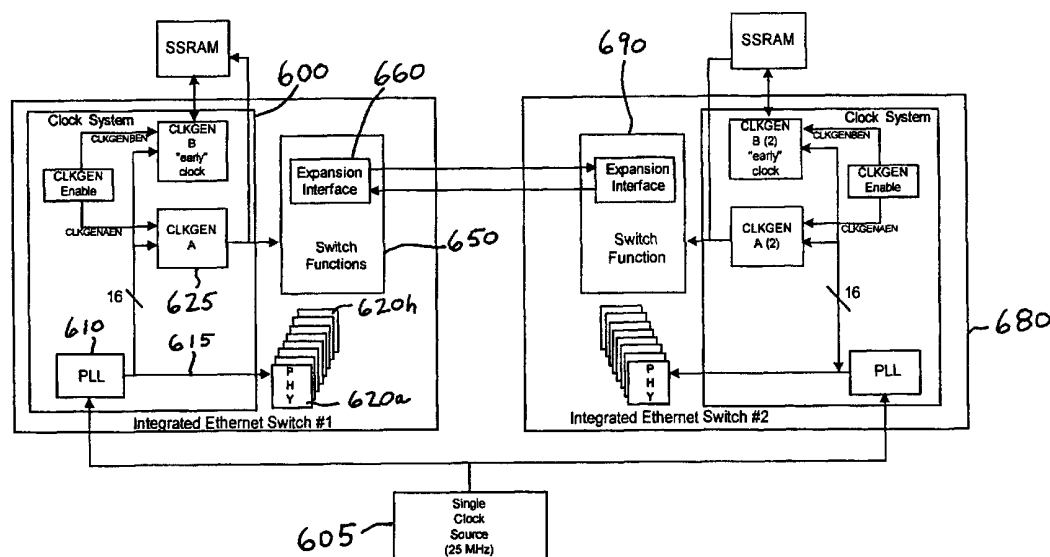
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[Continued on next page]

(54) **Title: INTEGRATED ETHERNET SWITCH**



(57) **Abstract:** A network switch having PHY integrated with the switch. The switch also integrates MAC with PHY. The PHY, MAC, and switch are integrated onto a single VLSI component. The network switch implements an IEEE Standard 802.3 communication protocol which may include autonegotiation, flow control, and duplexing. The communication protocol can include a 10Base-T communication protocol and a 100Base-T communication protocol. The switch includes an Address Resolution Table using associative memory. A free buffer pool, Transmit Descriptor Table, a Packet Storage Table, and combinations thereof also may reside with the Address Resolution Table in a shared memory block. Each PHY/MAC pair in the switch employs only a single Link Partner Capability Register. The switch uses a common system clock which is driven by a single clock source. The PLL that drives the PHY also drives the switch functions through a first clock generator. A second clock generator is used to drive devices external to the switch, such as memory.



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7 June 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 00/08637

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04L12/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GOLDBERG L: "24-PORT SWITCH-ON-A-CHIP SLASHES THE COST OF FAST ETHERNET" ELECTRONIC DESIGN,US,PENTON PUBLISHING, CLEVELAND, OH, vol. 45, no. 14, 7 July 1997 (1997-07-07), pages 31-32,34-35, XP000732577 ISSN: 0013-4872	1,4,26, 27
Y	the whole document	2,3,9, 15-18, 28,33, 39,40
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

° Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- * & * document member of the same patent family

Date of the actual completion of the international search

19 March 2001

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 00/08637

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>GALLES M: "SPIDER: A HIGH-SPEED NETWORK INTERCONNECT"</p> <p>IEEE MICRO,US,IEEE INC. NEW YORK, vol. 17, no. 1, 1997, pages 34-39, XP000642694</p> <p>ISSN: 0272-1732</p> <p>page 34, right-hand column, line 23 -page 35, left-hand column, line 13</p> <p>figure 1</p> <p style="text-align: center;">---</p>	<p>1,2, 23-25</p>
Y	<p>EP 0 505 695 A (IBM)</p> <p>30 September 1992 (1992-09-30)</p>	<p>2,3,9, 28,33, 39,40</p>
A	<p>column 1, line 39 -column 3, line 1</p> <p style="text-align: center;">---</p>	<p>34-38, 41-50</p>
A	<p>FONTAINE J A: "CONTROLLER AND MICRO TEAM UP FOR SMART ETHERNET MODE"</p> <p>COMPUTER DESIGN,US,PENNWELL PUBL. LITTLETON, MASSACHUSETTS, vol. 23, no. 2, February 1984 (1984-02), pages 215-216,218,220-223, XP000811014</p> <p>ISSN: 0010-4566</p> <p>page 223; figure B</p> <p style="text-align: center;">---</p>	<p>5-7, 10-14, 19-22, 29-32</p>
Y	<p>EP 0 869 643 A (HEWLETT PACKARD CO)</p> <p>7 October 1998 (1998-10-07)</p> <p>column 1, line 8 -column 2, line 33</p> <p style="text-align: center;">---</p>	<p>15-18</p>
A	<p>H.W. JOHNSON: "Fast Ethernet. Dawn of a new network" , PRENTICE HALL PTR , USA</p> <p>XP002148538</p> <p>page 41 -page 69</p> <p style="text-align: center;">-----</p>	<p>1-4,8,9, 26-28, 33-50</p>

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 00/08637

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-4,8,9,26-28,33-50

Common clock system for a transceiver(PHY) coupled to a switch

2. Claims: 5-7,10-14,19-22,29-32

Memory shared between a packet storage table and an address resolution table.

3. Claims: 15-18

Data register containing data representative of a communications protocol in a PHY

4. Claims: 23-25

Monolithic VLSI component comprising a switch and a PHY

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 00/08637

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0505695 A	30-09-1992	EP 0505779 A	30-09-1992
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