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(54) **FUSE OF A SEMICONDUCTOR MEMORY DEVICE AND REPAIR PROCESS FOR THE SAME**

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(57) **ABSTRACT**

Disclosed herein is a fuse of a semiconductor memory device and a repair process for the same. The fuse includes a lower conductive film of a multilayer interconnection formed on a lower structure of a semiconductor substrate, an upper conductive film of the multilayer interconnection spaced apart upward from the lower conductive film to define a predetermined vertical space therebetween, and a contact electrode, which vertically connects the upper and lower conductive films to each other and forms a fuse body. The lower conductive film includes a form not coinciding with that of the upper conductive film. With such a configuration, the device can achieve a stable minimization in the length of the fuse and the distance between adjacent fuses in consideration of a laser beam irradiation region for the high integration of the semiconductor memory device. In this way, the device performs the repair process of cutting the contact electrode and/or upper conductive film using a laser beam.

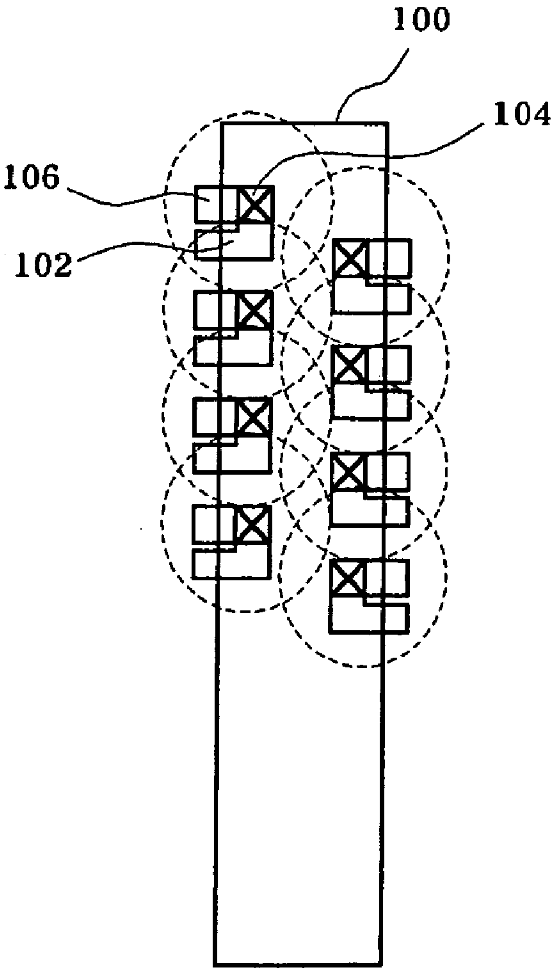


Fig. 1
(PRIOR ART)

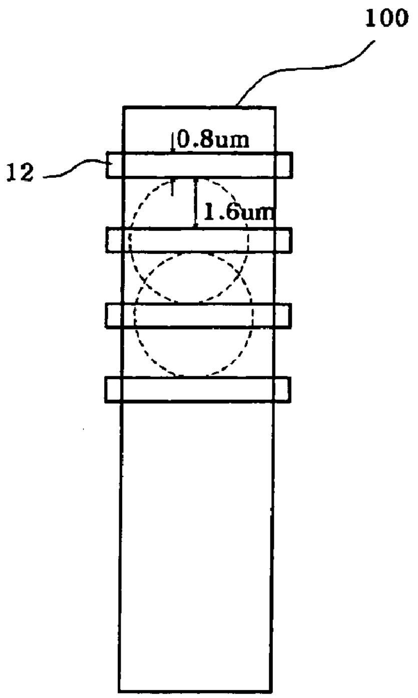


Fig. 2

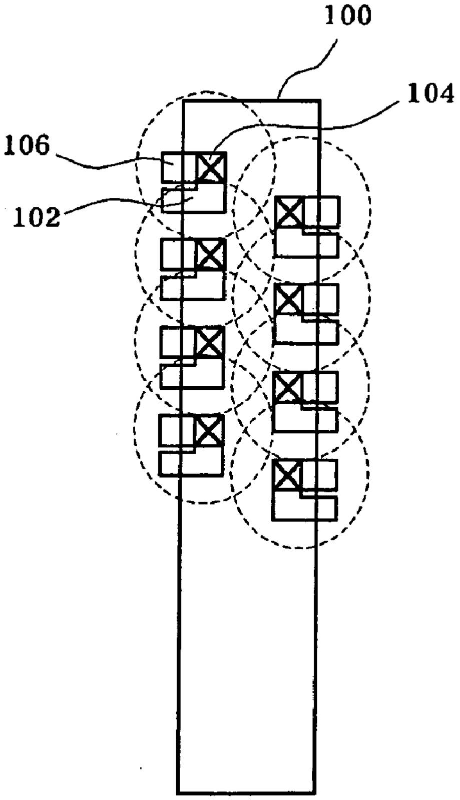


Fig. 3a

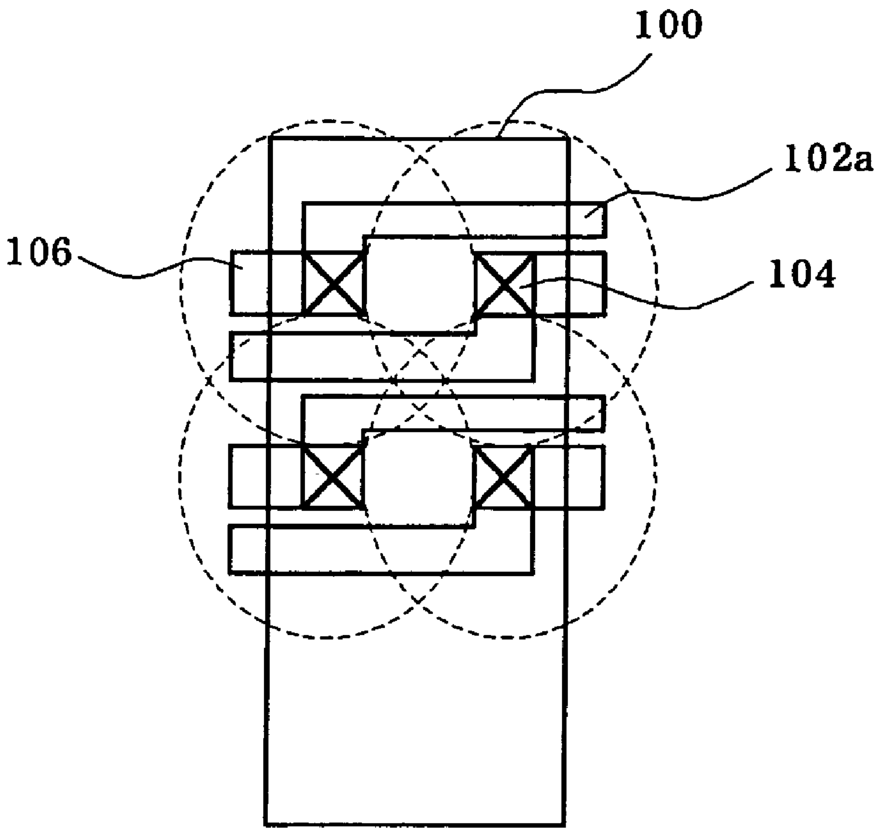


Fig. 3b

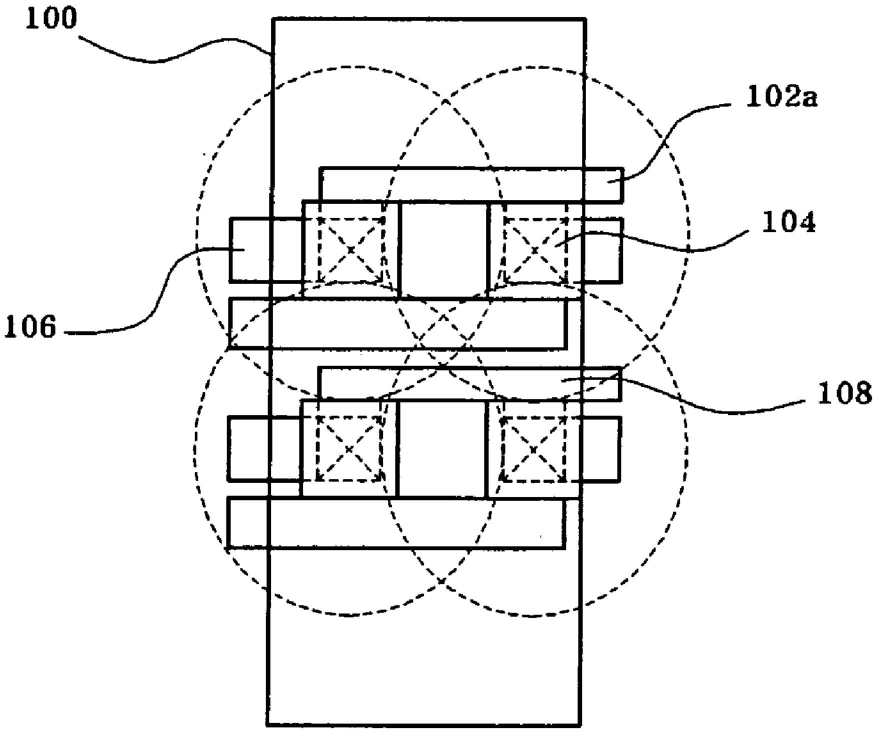


Fig. 4a

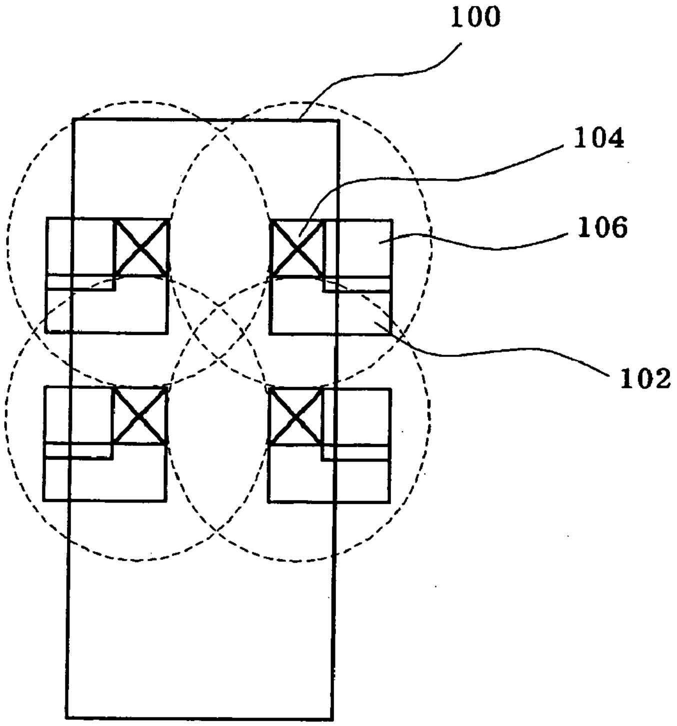


Fig. 4b

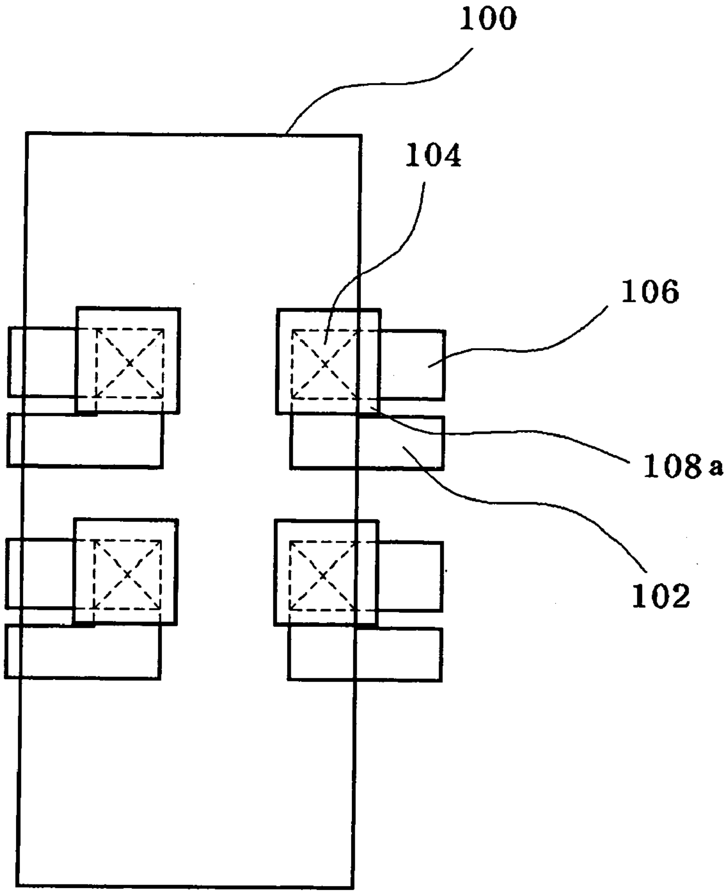


Fig. 5a

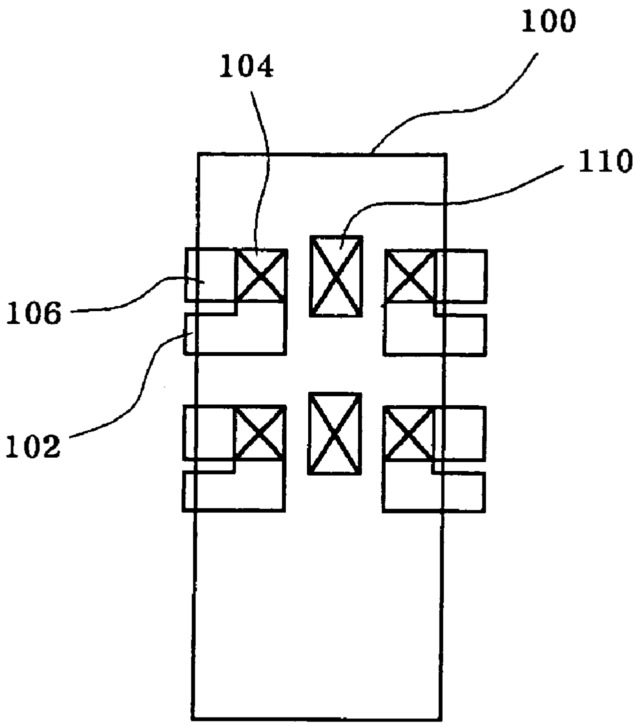


Fig. 5b

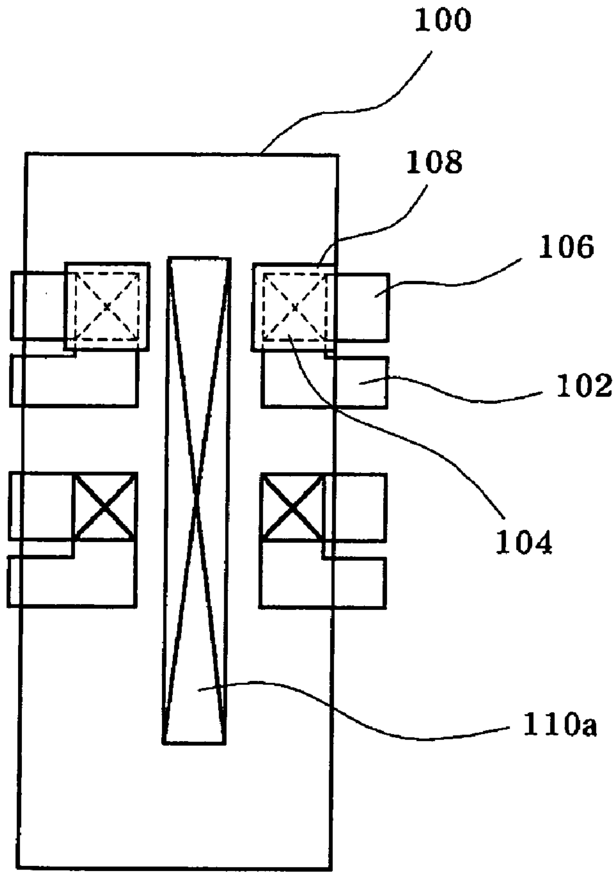


Fig. 6

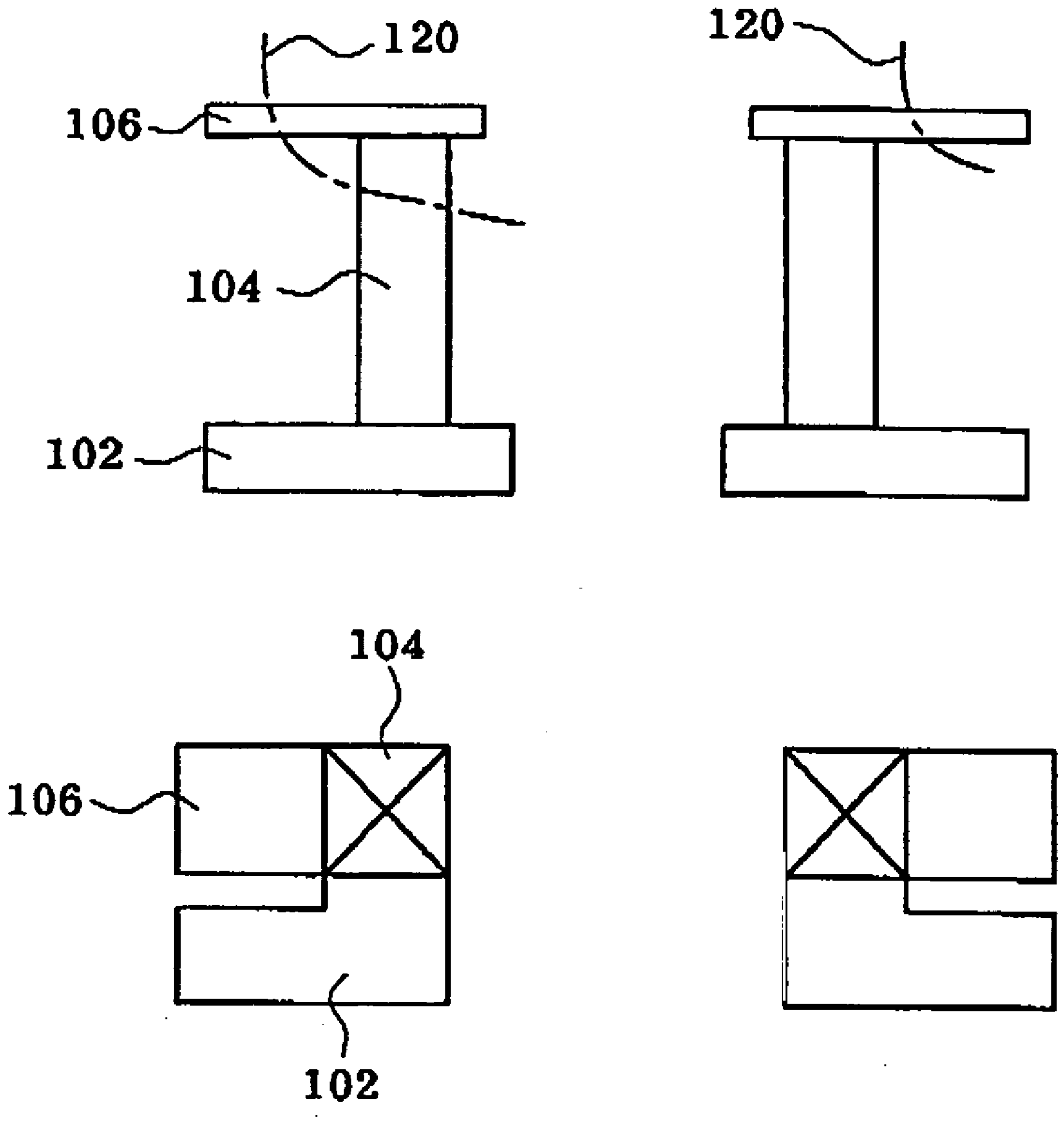


Fig. 7

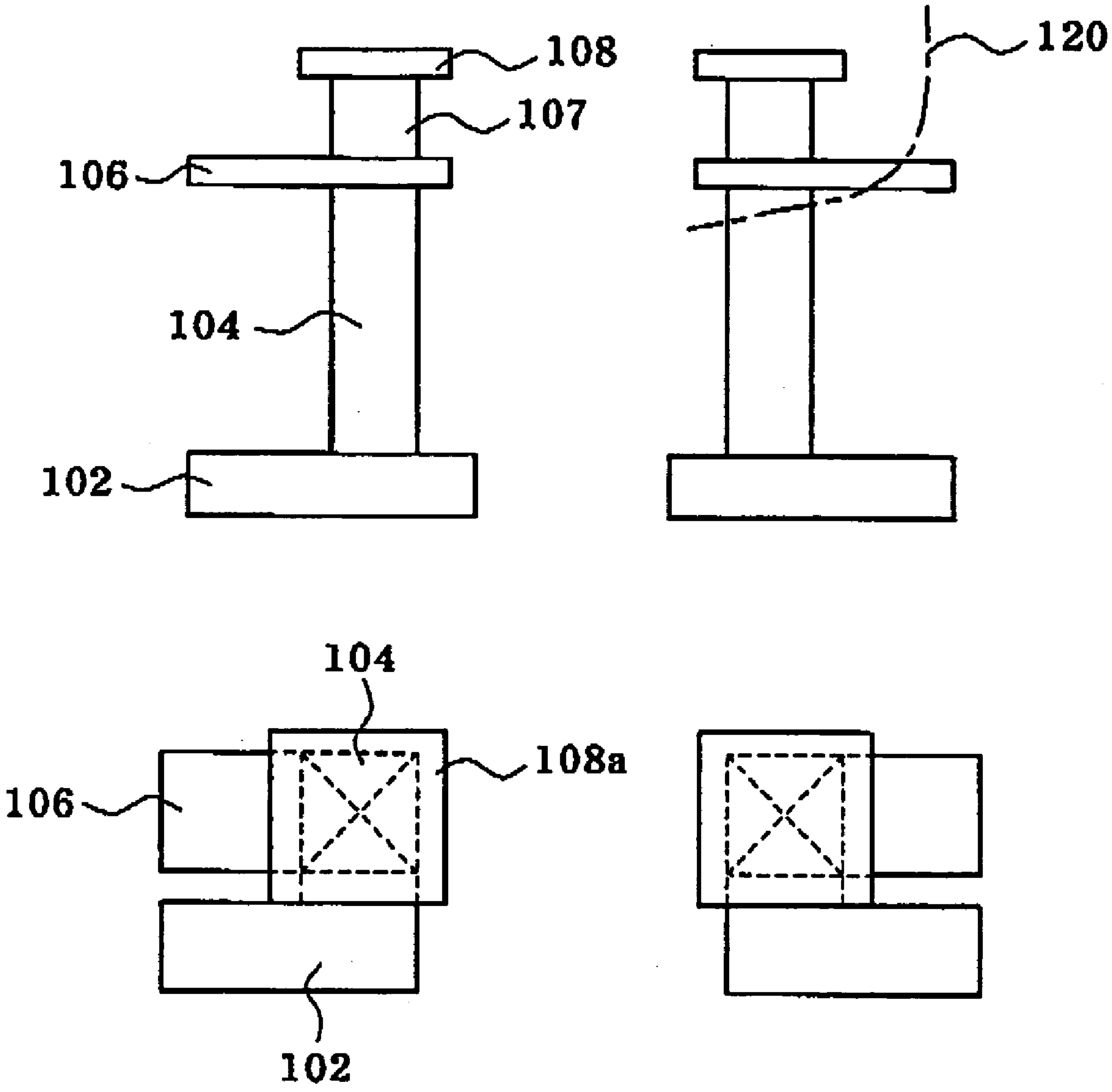
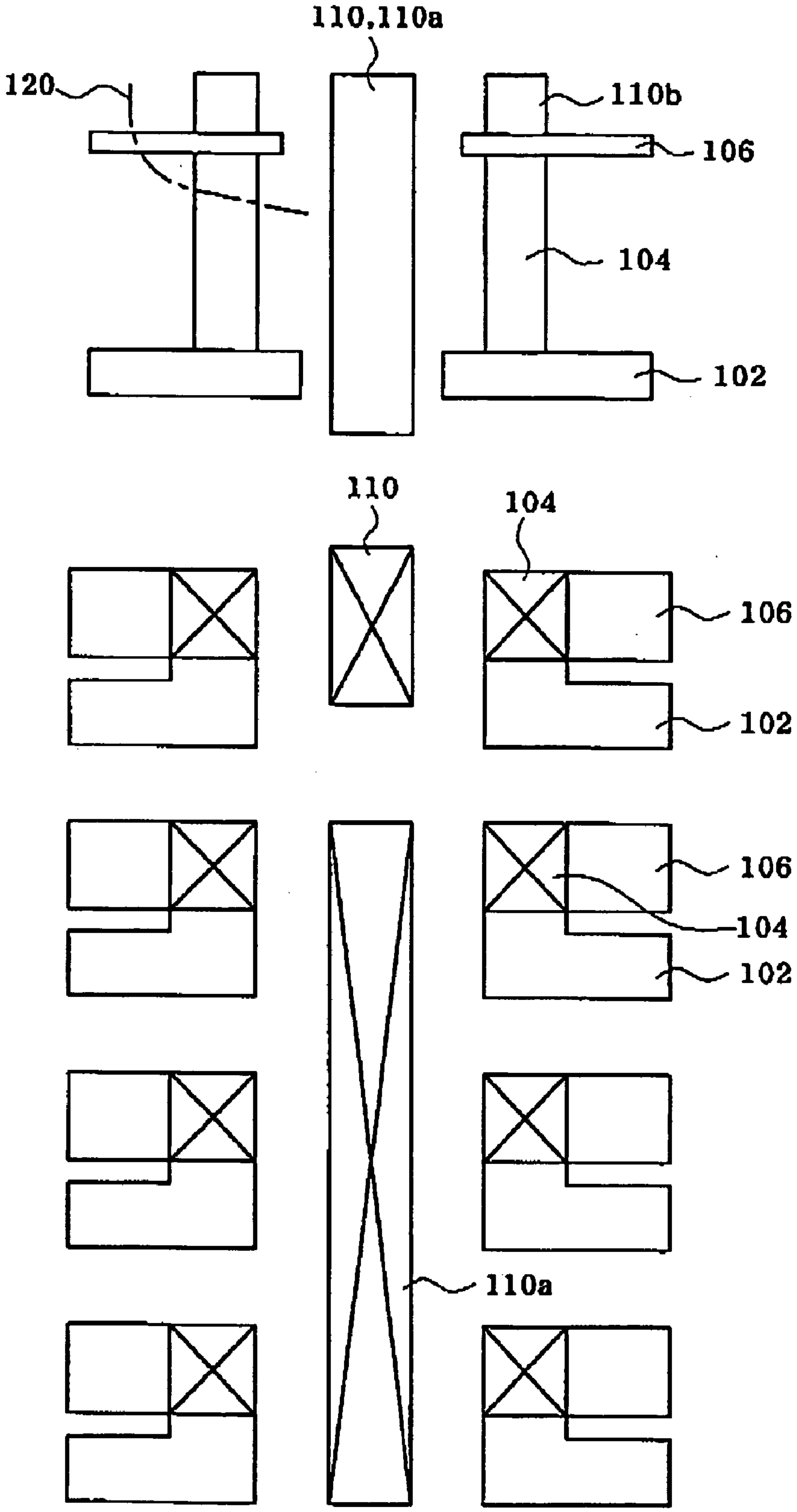


Fig. 8



FUSE OF A SEMICONDUCTOR MEMORY DEVICE AND REPAIR PROCESS FOR THE SAME

FIELD OF THE TECHNOLOGY

[0001] This disclosure relates generally to a semiconductor memory device, and, more particularly, to a fuse for use in a repair process of a semiconductor memory device and the repair process.

BACKGROUND

[0002] In Dynamic Random Access Memory (DRAM), the most widely used memory device, some memory cells included in a manufactured DRAM chip tend to show partial malfunction. Therefore, through a repair process, these defective memory cells are replaced with redundant cells, which are previously prepared in the course of manufacturing the chip, so as not to have any negative effects upon operation of the resulting chip. In conclusion, use of the repair process contributes to an increased chip yield.

[0003] In the repair process, a program for selecting respective defective memory cells and replacing an address signal corresponding to the defective memory cell with an address signal of the redundant cell is performed in an internal circuit. Thereby, if an address signal corresponding to a line of the defective memory cell is input, the selected line of the defective memory cell is replaced with a line of the redundant cell. In order to realize the program, a laser beam has conventionally been used to cut a fuse. Here, the fuse is an interconnection to be cut by the laser beam, and the region occupied by the fuse is referred to as a fuse box.

[0004] The fuse is mainly made of polysilicon, and is formed simultaneously with the formation of word lines of a first polysilicon layer or bit lines of a second polysilicon layer, rather than being formed through an additional process. Recently, according to an increase in an integration density and processing speed of semiconductor memory devices, the fuse is now increasingly being made of metal, instead of the polysilicon.

[0005] **FIG. 1** is a layout illustrating conventional fuses included in a semiconductor memory device. Referring to **FIG. 1**, a respective one of the fuses **12** takes the form of a single-layered conductive line (made of polysilicon or metal), and, as stated above, is formed simultaneously with the formation of the word lines, bit lines, or metal interconnections. In this case, if the width of the fuse **12** is 0.8 micrometers, the distance between adjacent fuses **12** must be doubled to 1.6 micrometers in order to ensure stability in the fuse repair process using the laser beam.

[0006] However, in the fuses of the conventional semiconductor memory device, as a result of horizontally arranging a plurality of the fuses, in the form of single-layered conductive lines, on a semiconductor substrate, it is necessary to reduce the distance between the fuses **12** as the integration density of the semiconductor memory device increases. Such a reduction in the distance between the fuses **12**, however, correspondingly decreases a laser beam irradiation area, resulting in the risk of cutting unintended fuses by the laser beam.

SUMMARY

[0007] In one aspect, the invention is directed to a fuse of a semiconductor memory device which may include a lower conductive film of a multilayer interconnection formed on a lower structure of a semiconductor substrate, an upper conductive film of the multilayer interconnection spaced apart upward from the lower conductive film to define a predetermined vertical space there between, and a contact electrode, which vertically connects the upper and lower conductive films to each other and forms a fuse body, wherein the lower conductive film has a form not coinciding with that of the upper conductive film.

[0008] In another aspect, the invention is directed to a repair process for a fuse of a semiconductor memory device, the fuse comprising a lower conductive film of a multilayer interconnection formed on a lower structure of a semiconductor substrate, an upper conductive film of the multilayer interconnection spaced apart upward from the lower conductive film to define a predetermined vertical space therebetween, and a contact electrode vertically connecting the upper and lower conductive films to each other and forming a fuse body, comprising: cutting one or more of the following using a laser beam: the contact electrode or the upper conductive film of the fuse.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **FIG. 1** is a layout illustrating conventional fuses of a semiconductor memory device;

[0010] **FIG. 2** is a layout illustrating a first example of fuses of a semiconductor memory device;

[0011] **FIGS. 3*a*** and **3*b*** are layouts illustrating a second example of fuses of the semiconductor memory device;

[0012] **FIGS. 4*a*** and **4*b*** are layouts illustrating a third example of fuses of the semiconductor memory device;

[0013] **FIGS. 5*a*** and **5*b*** are layouts illustrating a fourth example of fuses and contact electrodes of the semiconductor memory device;

[0014] **FIG. 6** is a view depicting a first example of a repair process for cutting the fuse using a laser beam;

[0015] **FIG. 7** is a view depicting a second example of a repair process for cutting the fuse using the laser beam, in a state wherein a pad is added to the fuse; and

[0016] **FIG. 8** is a view depicting a third example of a repair process for cutting the fuse using the laser beam in a state wherein a contact electrode is interposed between the adjacent fuses.

DETAILED DESCRIPTION

[0017] **FIG. 2** is a layout illustrating an example of fuses of a semiconductor memory device.

[0018] Referring to **FIG. 2**, the fuse, in the form of a multilayer interconnection, includes a lower conductive film **102** formed on an interlayer insulating film, which is a lower structure **100** of a semiconductor substrate, an upper conductive film **106** spaced apart upward from the lower conductive film **102** so as to define a predetermined vertical space there between, and a contact electrode **104** vertically connecting the lower and upper conductive films **102** and **106** to each other. Here, the lower and upper conductive films **102** and **106** are made of metal, and the vertical contact electrode **104**, connecting the lower and upper conductive films **102** and **106**, forms a fuse body.

[**0019**] In the example of **FIG. 2**, in order to provide a laser beam irradiation space for a repair process, the upper conductive film **106** has a horizontal line form, and the lower conductive film **102** has an L-shaped or a 90°-rotated L-shaped form. The reason why the lower conductive film **102** is formed to have the L-shaped or a 90°-rotated L-shaped form, rather than the horizontal line form, is for defining a predetermined space between the lower conductive film **102** and the contact electrode **104**, in order to prevent the lower conductive film **102** from being cut by a laser beam.

[**0020**] In the example of **FIG. 2**, a plurality of fuses are formed and are asymmetrically arranged in two rows, providing a sufficient laser beam irradiation space for the repair process.

[**0021**] With such a configuration, a semiconductor memory device or other semiconductor device is provided using a repair fuse with the plurality of highly integrated fuses having vertical contact electrodes. When it is desired to reduce the entire size of the semiconductor device for achieving the high integration density thereof, a region occupied by the fuses, namely, a fuse box is correspondingly reduced. In connection with this, a significant reduction in the overall size of the fuses is enabled through the use of the vertical contact electrode **104**. Thereby, the fuses or fuse box can be integrated even in a reduced narrow area while ensuring a sufficient layout stability of the fuses, resulting in an improvement in the productivity of the semiconductor device.

[**0022**] **FIGS. 3***a* and **3***b* are layouts illustrating a second example of fuses of the semiconductor memory device.

[**0023**] Referring to **FIG. 3***a*, a lower conductive film **102***a*, connected to the vertical contact electrode **104** has a clockwise or counterclockwise 90°-rotated L-shaped form. Referring to **FIG. 3***b*, the fuse may further include a metal pad **108**, which is connected to the upper metal film **106** by means of contact electrodes (not shown). In this case, the metal pad **108** is larger than the contact electrode **104** as the fuse body.

[**0024**] In the example of **FIGS. 3***a* and **3***b*, the plurality of fuses is symmetrically arranged in two rows.

[**0025**] **FIGS. 4***a* and **4***b* are layouts illustrating a third example of fuses of the semiconductor memory device.

[**0026**] Referring to **FIG. 4***a*, the plurality of fuses has the same arrangement as that of **FIG. 2** except for the fact that they are symmetrically arranged. Referring to **FIG. 4***b*, a metal pad **108***a* can be added to one of the fuses symmetrically arranged in two rows. Similarly, the metal pad **108***a* is connected to the upper metal film **106** by means of contact electrodes (not shown).

[**0027**] In the examples shown in **FIGS. 3***b* and **4***b*, even if the size of the contact electrode **104** is invisible to the naked eye, the metal pad **108**; **108***a* added to the fuse enables the contact electrode **104** to be easily confirmed with the naked eye in the repair process.

[**0028**] **FIGS. 5***a* and **5***b* are layouts illustrating a fourth example of the fuses and additional contact electrodes of the semiconductor memory device.

[**0029**] Referring to **FIG. 5***a*, the fourth example is similar to the example of **FIGS. 4***a* and **4***b* except that two or more contact electrodes **110**, which are spaced apart from each other, are added in the space defined between the two rows of the fuses. In this case, each of the contact electrodes **110** has a size equal to or similar to that of the contact electrode **104** used as the fuse body. Alternatively, referring to **FIG. 5***b*, a single contact electrode **110***a* may be formed in the space defined between the two rows of the fuses. The single contact electrode **110***a* has a size equal to the size of the two or more fuses.

[**0030**] As a result of adding the two or more contact electrodes **110** spaced apart from each other or the single contact electrode **110***a* in the space between the two rows of the fuses **104**, the fourth example can prevent corrosion of some fuses aligned in a row from having a negative effect upon other fuses aligned in the other row.

[**0031**] **FIG. 6** is a view depicting an example of the repair process for cutting the fuse using the laser beam.

[**0032**] Referring to **FIG. 6**, in the repair process, the contact electrode **104** of the fuse, vertically connecting the lower and upper conductive films **102** and **106**, is cut by the laser beam. In this case, the upper conductive film **106** of the fuse is cut by the laser beam, along with the contact electrode **104** or alone.

[**0033**] **FIG. 7** is a view depicting a second example of a repair process for cutting the fuse using the laser beam, in a state wherein the metal pad **108***a* is added to the fuse.

[**0034**] Referring to **FIG. 7**, in the repair process related to the fuse having the metal pad **108***a* for facilitating confirmation of the fuse **104** with the naked eye, the contact electrode **104** and the upper conductive film **106** of the fuse, as the subject of repair, are cut by the laser beam as shown by the dash-dotted line **120**. A contact pad **107** connects the metal pad **108***a* to the upper conductive film **106**.

[**0035**] **FIG. 8** is a view depicting a third example repair process for cutting the fuse using the laser beam, in a state wherein the electrode(s) **110**; **110***a* is added in the space defined between the two rows of the fuses.

[**0036**] Referring to **FIG. 8**, in the repair process related to the fuse having the contact electrode(s) **110**; **110***a* located in the space between the two rows of the fuses, the contact electrode **104** and the upper conductive film **106** of the fuse, as the subject of repair, are cut by the laser beam as shown by the dash-dotted line **120**. In this case, it is necessary to take precautions so as not to cut the contact electrode(s) **110**; **110***a* by the laser beam. A contact pad **107** is connected with the upper conductive film **106**.

[**0037**] As apparent from the above description, this disclosure provides a fuse of a semiconductor memory device wherein, in the manufacture of a multilayer interconnection of the semiconductor memory device, a contact electrode, which vertically connects upper and lower interconnections to each other, is formed as a fuse body, thereby being capable of achieving a stable minimization of the fuse and the distance between adjacent fuses in consideration of a laser beam irradiation region for the high integration of the semiconductor memory device, and a repair process for the same.

[**0038**] Although certain examples of methods and apparatus constructed in accordance with the teachings of the invention have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all embodiments of the teachings of the invention fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A fuse of a semiconductor memory device comprising:

a lower conductive film of a multilayer interconnection formed on a lower structure of a semiconductor substrate;

an upper conductive film of the multilayer interconnection spaced apart upward from the lower conductive film to define a predetermined vertical space there between; and

a contact electrode, which vertically connects the upper and lower conductive films to each other and forms a fuse body,

wherein the lower conductive film comprises a form not coinciding with that of the upper conductive film.

2. The fuse according to claim 1, wherein the upper conductive film comprises a horizontal line form, and the lower conductive film comprises an L-shaped or 90° rotated L-shaped form.

3. The fuse according to claim 1, wherein the upper conductive film comprises a horizontal line form, and the lower conductive film comprises a clockwise or counterclockwise 90° rotated L-shaped form.

4. The fuse according to claim 1, further comprising:

a metal pad vertically connected to the upper conductive film by a second contact electrode.

5. The fuse according to claim 4, wherein the metal pad is larger than the second contact electrode or the contact electrode as the fuse body.

6. The fuse according to claim 1, wherein a plurality of the fuses, each comprising the upper and lower conductive films and the contact electrode, are asymmetrically arranged in plural rows.

7. The fuse according to claim 6, further comprising one or more of the following:

a plurality of contact electrodes spaced apart from one another, or a single contact electrode installed in a space defined between the plural rows of the fuse units.

8. The fuse according to claim 1, wherein a plurality of the fuses, each comprising the upper and lower conductive films and the contact electrode, are symmetrically arranged in plural rows.

9. The fuse according to claim 8, further comprising one or more of the following:

a plurality of contact electrodes spaced apart from one another, or a single contact electrode installed in a space defined between the plural rows of the fuse units.

10. A repair process for a fuse of a semiconductor memory device, the fuse comprising a lower conductive film of a multilayer interconnection formed on a lower structure of a semiconductor substrate, an upper conductive film of the multilayer interconnection spaced apart upward from the lower conductive film to define a predetermined vertical space therebetween, and a contact electrode vertically connecting the upper and lower conductive films to each other and forming a fuse body, comprising:

cutting one or more of the following using a laser beam: the contact electrode; or the upper conductive film of the fuse.

11. The process according to claim 10, wherein the fuse further comprises a metal pad connected to the upper conductive film by a contact electrode.

* * * * *