ABSTRACT
A semiconductor device includes a substrate, an electrode layer disposed on the substrate, and a tri-layered gate-control stack sandwiched between the substrate and the electrode layer. The tri-layered gate-control stack includes a ferroelectric layer disposed on the substrate, a mid-gap metal layer sandwiched between the ferroelectric layer and the substrate, and an anti-ferroelectric layer. The anti-ferroelectric layer is sandwiched between the substrate and the mid-gap metal layer. Alternatively, the ferroelectric layer and the mid-gap metal layer are sandwiched between the anti-ferroelectric layer and the substrate.
SEMICONDUCTOR DEVICE

SUMMARY OF THE INVENTION

[0005] According to an aspect of the present invention, a semiconductor device is provided. The semiconductor device includes a substrate, an electrode layer disposed on the substrate, and a tri-layered gate-control stack sandwiched between the substrate and the electrode layer. The tri-layered gate-control stack further includes a ferroelectric (FE) layer disposed on the substrate, an anti-ferroelectric (AFE) layer sandwiched between the FE layer and the substrate, and a mid-gap metal layer sandwiched between the FE layer and the AFE layer.

[0006] According to another aspect of the present invention, a semiconductor device is provided. The semiconductor device includes a substrate, an electrode layer disposed on the substrate, and a tri-layered gate-control stack sandwiched between the substrate and the electrode layer. The tri-layered gate-control stack further includes an AFE layer disposed on the substrate, a mid-gap metal layer sandwiched between the AFE layer and the substrate, and a FE layer sandwiched between the AFE layer and the mid-gap metal layer.

[0007] According to still another aspect of the present invention, a semiconductor device is provided. The semiconductor device includes a substrate, an electrode layer disposed on the substrate, and a tri-layered gate-control stack sandwiched between the substrate and the electrode layer. The tri-layered gate-control stack further includes an amorphous dielectric layer, a mid-gap metal layer disposed between the amorphous dielectric layer and the substrate, and a polycrystalline dielectric layer. The mid-gap metal layer directly contacts the amorphous dielectric layer. And the amorphous dielectric layer and the polycrystalline dielectric layer both include hafnium oxide materials.

[0008] According to the semiconductor devices provided by the present invention, the tri-layered gate-control stack is provided between the electrode layer and the substrate, and the tri-layered gate-control stack includes the FE layer, the AFE layer and the mid-gap metal layer. It is noteworthy that in the tri-layered gate-control stack, the mid-gap metal layer is always sandwiched between the FE layer and the substrate while the AFE layer is disposed on or under the dual-layered structure consisting of the FE layer and the mid-gap metal layer. The FE layer is provided to enhance electric fields created by the electrode layer and the mid-gap metal layer is provided to homogenize the enhanced electric fields. Furthermore, the AFE layer is provided to render negative capacitance effect. The tri-layered gate-control stack is therefore used to replace conventional high-k gate dielectric layer according to the present invention, and the semiconductor device provided by the present invention therefore obtains smaller subthreshold swing.

[0009] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a schematic drawing illustrating a semiconductor device provided by a first preferred embodiment of the present invention, and
FIG. 2 is a schematic drawing illustrating a semiconductor device provided by a second preferred embodiment of the present invention.

DETAILED DESCRIPTION

Please refer to FIG. 1, which is a schematic drawing illustrating a semiconductor device provided by a first preferred embodiment of the present invention. As shown in FIG. 1, a semiconductor device 100 includes a substrate 102 such as silicon substrate, silicon-containing substrate, or silicon-on-insulator (hereinafter abbreviated as SOI) substrate. A plurality of isolation structures (not shown) is formed in the substrate 102. The isolation structures can be shallow trench isolations (STIs), but not limited to this. The isolation structures are used to define a plurality of active regions for accommodating p-type FET (hereinafter abbreviated as pFET) devices and/or n-type FET (hereinafter abbreviated as nFET) devices, and to provide electrical isolation. In some preferred embodiments of the present invention, a semiconductor layer such as a fin structure involved in fin field effect transistor (FinFET) approach can be provided. The fin structure can be formed by patterning a single crystalline silicon layer of a SOI substrate or a bulk silicon substrate by photolithographic etching pattern (PEP) method, multi patterning method, or, preferably, spacer self-aligned double patterning (SADP), also known as sidewall image transfer (SIT) method. And the fin structure can be taken as the substrate 102 in the preferred embodiment.

An electrode layer 110 is disposed on the substrate 102. In the preferred embodiment, metal gate approach is integrated. Accordingly, the electrode layer 110 includes at least a work function metal layer 110a, and the work function metal layer 110b includes various metal materials depending on the conductivity type of the semiconductor device 100 to be formed. In some embodiments of the present invention, the semiconductor device 100 is a p-type semiconductor device, and the work function metal layer 110b includes any suitable metal material having a work function between about 4.8 eV and about 5.2 eV such as titanium nitride (TiN), tantalum nitride (TaN), titanium carbide (TiC), tantalum carbide (TaC), tungsten carbide (WC), or aluminum nitride (AlN), but not limited to this. Alternatively, in some embodiments of the present invention, the semiconductor device 100 is a n-type semiconductor device, and the work function metal layer 110b includes any suitable metal material having a work function between about 3.9 eV and about 4.3 eV such as zirconium oxide (ZrO2), zirconium alumina (ZrAl2), hafnium oxide (HfO2), or hafnium nitride (HfN), but not limited to this. Additionally, the work function metal layer 110b can be a single-layered structure or a multi-layered structure. The electrode layer 110 further includes a gap-filling metal layer 110a, and the gap-filling metal layer 110b can be a single metal layer or a multiple metal layer including superior gap filling ability, such as Al, Ti, Ta, W, Nb, Mo, Cu, TiN, TiC, TaN, Ti/W, or Ti/TiN, but not limited to this. Furthermore, it is well-known to those skilled in the art that a bottom barrier layer, an etch stop layer, and/or a top barrier layer can be included in the electrode layer 110 if required. As shown in FIG. 1, a bottom barrier layer 112 is sandwiched between the electrode layer 110 and the substrate 100, and an etch stop layer 114 is sandwiched between the electrode layer 110 and the bottom barrier layer 112. Additionally, a top barrier layer (not shown) can be sandwiched between the work function metal layer 110a and the gap-filling metal layer 110b. The etch stop layer 114 preferably includes material including etching rate different from the bottom barrier layer 112. For example, but not limited to, the bottom barrier layer 112 can be a TiN layer and the etch stop layer 114 can be a TaN layer.

Please still refer to FIG. 1. The semiconductor device 100 provided by the preferred embodiment further includes a tri-layered gate-control stack 120 sandwiched between the substrate 102 and the electrode layer 110. The tri-layered gate-control stack 120 includes a FE layer 122 disposed on the substrate 102, an AFE layer 126 sandwiched between the FE layer 122 and the substrate 102, and a mid-gap metal layer 124 sandwiched between the FE layer 122 and the AFE layer 126. In some embodiments of the present invention, the FE layer 122 includes a material selected from the group consisting of lead zirconate titanate (PbZrTiO3, PZT), lead lanthanum zirconate titanate (PbLa (TiZrO3, PLZT), strontium bismuth tantalate (SrBi2Ta2O9, SBT), bismuth lanthanum titanate (BiLa3TiO32, BLT), and barium strontium titanate (BaSrTiO3, BST). The AFE layer 126 includes a material selected from the group consisting of lead indium niobate (Pb(InNb)O3), niobium oxide (Nb2O5), zirconate (ZrO2), lead lanthanum zirconate titanate (PbLa (TiZrO3, PLZT), ammonium dihydrogen phosphate (NH4H2PO4, ADP), and ammonium dihydrogen arsenate (NH4H2AsO4, ADA). It is noteworthy that the FE layer 122 and the AFE layer 126 can include the same elementary material but with different crystalline morphologies and/or composition ratio. For example, both of the FE layer 122 and the AFE layer 126 can include hafnium oxide material such as HfZrO2, but the FE layer 122 includes amorphous HfZrO2, while the AFE layer 126 includes polycrystalline HfZrO2. It is noteworthy that hafnium oxide material can still include other elementary material such as Zr in accordance with the present invention. In other words, in some embodiments of the present invention, the FE layer 122 is taken as an amorphous or a fractionally crystalized dielectric layer and the AFE layer 126 is taken as a polycrystalline dielectric layer. The mid-gap metal layer 124 includes metal having a work function between valence band and conduction band. The mid-gap metal layer 124 includes metal nitride such as, for example but not limited to, TiN, TaN, titanium nitride (TiN), tantalum nitride (TaN), or molybdenum nitride (MoN). In other embodiments of the present invention, the mid-gap metal layer 124 can include nickel silicide (NiSi2), tungsten silicide (WSi2), cobalt silicide (CoSi2), or titanium tungsten (TiW), but not limited to this.

It is noteworthy that since an antiferromagnetic state will transfer to a paramagnetic state at a temperature over the Neel temperature, high-k last approach is adopted in the preferred embodiments of the present invention in order to avoid the above mentioned issue. It is well-known to those skilled in the art that in the high-k last approach, a dummy gate or a replacement gate (not shown) is formed on the substrate 102 and followed by forming elements of a FET device such as light doped areas (LDDs) 106, a spacer 104, and a source/drain 108. The dummy gate includes a dielectric layer (not shown), a conductive layer such as a polysilicon layer (not shown), and a patterned hard mask (not shown). The spacer 104 can be a single-layered struc-
ture or a multi-layered structure, but not limited to this. Furthermore, selective strain scheme (SSS) can be used to form the source/drain. When the semiconductor device 100 is the p-type transistor, epitaxial silicon layers of SiGe are used to form the source/drain. When the semiconductor device 100 is the n-type transistor, epitaxial silicon layers of SiC or SiP are used to form the source/drain. Additionally, sacrifices (not shown) can be formed on the source/drain 108. After forming the semiconductor device 100, an etch liner such as a contact etch stop layer (hereinafter abbreviated as CESL) (not shown) is selectively formed on the substrate 100, and an interlayer dielectric (hereinafter abbreviated as ILD) layer 130 is subsequently formed. Next, a planarization process such as chemical mechanical polishing (CMP) process is performed to planarize the ILD layer 130 and the CESL. The patterned hard mask is then removed to expose the conductive layer of the dummy gate and followed by removing the conductive layer and the dielectric layer of the dummy gate. Consequently, a gate trench (not shown) is formed on the substrate 102. In some preferred embodiments of the present invention, an oxide layer 128 can be formed in the gate trench and followed by forming the tri-layered gate-control stack 120 in the gate trench. After forming the tri-layered gate-control stack 120, the abovementioned metal layers are formed. Accordingly, the tri-layered gate-control stack 120 includes a U shape in the preferred embodiments. The oxide layer 128 serves as an interfacial layer (IL), and the interfacial layer provides a superior interface between the substrate 102 and the tri-layered gate-control stack 120. Additionally, the bottom barrier layer 112 and the etch stop layer 114 are sandwiched between the tri-layered gate-control stack 120 and the electrode layer 110 as shown in FIG. 1. It should be easily understood that those skilled in the art that in still other preferred embodiments of the present invention, high-k first approach can be adopted and thus the tri-layered gate-control stack 120 includes a flat shape in those preferred embodiments.

According to the semiconductor device 100 provided by the preferred embodiment, the tri-layered gate-control stack 120 sandwiched between the electrode layer 110 and the substrate 102 is provided. The FE layer 122 (or, the material layer including the ferroelectric characteristic due to its amorphous or fractionally crystallized morphology, such as the amorphous or fractionally crystallized dielectric layer) of the tri-layered gate-control stack 120 is used to enhance the electric fields created by the electrode layer 110. However, it is found the electric fields enhanced by the FE layer 122 are inhomogeneous. Therefore, the mid-gap metal layer 124 sandwiched between the FE layer 122 and the substrate 102 is provided. The mid-gap metal layer 124 directly contacts the FE layer (the amorphous or fractionally crystallized dielectric layer) and homogenizes the electric fields enhanced by the FE layer 122. Furthermore, the AFE layer 126 (the material layer including anti-ferroelectric characteristic due to its polycrystalline morphology, such as the polycrystalline dielectric layer) is provided to render negative capacitance effect. Consequently, the subthreshold swing is reduced. Compared with the device including the conventional high-k gate dielectric layer, the subthreshold swing of the semiconductor device 100 provided by the present invention is significantly reduced from 60 mV/dec to 10 mV/dec, which is beyond the physical limit. And thus both leakage current and power consumption are reduced.

Please refer to FIG. 2, which is a schematic drawing illustrating a semiconductor device provided by a second preferred embodiment of the present invention. It should be noted that elements the same in the first and second preferred embodiments can be formed by the same method with the same material, thus those details are omitted in the interest of brevity. As shown in FIG. 2, a semiconductor device 200 is proved by the preferred embodiment, and the semiconductor device 200 includes a substrate 202. A plurality of isolation structures (not shown) is formed in the substrate 202. The isolation structures are used to define a plurality of active regions for accommodating pFET devices and/or nFET devices, and to provide electrical isolation. Furthermore, a semiconductor layer such as a fin structure involved in FinFET approach can be provided and taken as the substrate 202 in some preferred embodiments of the present invention. An electrode layer 210 is disposed on the substrate 202. In the preferred embodiment, metal gate approach is integrated. Accordingly, the electrode layer 210 includes at least a work function metal layer 210a, and the work function metal layer 210a includes various metal materials depending on the conductivity type of the semiconductor device 200 to be formed: In some embodiments of the present invention, the semiconductor device 200 is a p-type semiconductor device, and the work function metal layer 210a includes any suitable metal material having a work function about 4.8 eV and about 5.2 eV. Alternatively, in some embodiments of the present invention, the semiconductor device 200 is an n-type semiconductor device, and the work function metal layer 210a includes any suitable metal material having a work function between about 3.9 eV and about 4.3 eV. Additionally, the work function metal layer 210a can be a single-layered structure or a multi-layered structure. The electrode layer 210 further includes a gap-filling metal layer 210b, and the gap-filling metal layer 210b can be a single metal layer or a multiple metal layer including superior gap filling ability. Furthermore, it should be easily understood that those skilled in the art that a bottom barrier layer, an etch stop layer, and/or a top barrier layer can be included in the electrode layer 210 if required. As shown in FIG. 2, a bottom barrier layer 212 is sandwiched between the electrode layer 210 and the substrate 200 while an etch stop layer 214 is sandwiched between the electrode layer 210 and the bottom barrier layer 212. Additionally, a top barrier layer (not shown) can be sandwiched between the work function metal layer 210a and the gap-filling metal layer 210b. And the etch stop layer 214 preferably includes material including etching rate different from the bottom barrier layer 212.

Please still refer to FIG. 2. The semiconductor device 200 provided by the preferred embodiment further includes a tri-layered gate-control stack 220 sandwiched between the substrate 202 and the electrode layer 210. The tri-layered gate-control stack 220 includes an AFE layer 226 disposed on the substrate 202, a mid-gap metal layer 224 sandwiched between the AFE layer 226 and the substrate 202, and a FE layer 222 sandwiched between the AFE layer 226 and the mid-gap metal layer 224. As mentioned above, the FE layer 222 and the AFE layer 226 can include different materials, or the same elementary material but with different crystalline morphologies and/or composition ratio.
words, the FE layer 222 can be taken an amorphous or a fractionally crystallized dielectric layer while the AFE layer 226 can be taken as a polycrystalline dielectric layer.

[0020] As mentioned afore, since an antiferromagnetic state will transfer to a paramagnetic state at a temperature over the Neel temperature, high-k last approach is adopted in preferred embodiments of the present invention in order to avoid the above mentioned issue. It is well-known to those skilled in the art that in the high-k last approach, a dummy gate or a replacement gate (not shown) is formed on the substrate 202 and followed by forming elements of a FET device such as LDDs 206, a spacer 204, and a source/drain 208. And after forming a CESL (not shown) and an ILD layer 230, the dummy gate is removed to form a gate trench (not shown) on the substrate 202. In some preferred embodiments of the present invention, an oxide liner 228 can be formed in the gate trench and followed by forming the tri-layered gate-control stack 220 in the gate trench. And after forming the tri-layered gate-control stack 220, the abovementioned metal layers are formed. Accordingly, the tri-layered gate-control stack 220 includes a U shape in the preferred embodiments. The oxide liner 228 serves as an interfacial layer, and the interfacial layer provides a superior interface between the substrate 202 and the tri-layered gate-control stack 220. Additionally, the bottom barrier layer 212 and the etch stop layer 214 are sandwiched between the tri-layered gate-control stack 220 and the electrode layer 210 as shown in FIG. 2. It should be easily understood to those skilled in the art that in still other preferred embodiments of the present invention, high-k first approach can be adopted and thus the tri-layered gate-control stack 220 includes a flat shape in those preferred embodiments.

[0021] According to the semiconductor device 200 provided by the preferred embodiment, the tri-layered gate-control stack 220 sandwiched between the electrode layer 210 and the substrate 202 is provided. The FE layer 222 (or the amorphous or fractionally crystallized dielectric layer) of the tri-layered gate-control stack 220 is used to enhance the electric fields created by the electrode layer 210. However, it is known the electric fields enhanced by the FE layer 222 are inhomogeneous. Therefore, the mid-gap metal layer 224 sandwiched between the FE layer 222 and the substrate 202 is provided. The mid-gap metal layer 224 directly contacts the FE layer (the amorphous or fractionally crystallized dielectric layer) and homogenizes the electric fields enhanced by the FE layer 222. Furthermore, the AFE layer 226 (the polycrystalline dielectric layer) is provided to render negative capacitance effect. Consequently, the subthreshold swing is reduced. Compared with the device including the conventional high-k gate dielectric layer, the subthreshold swing of the semiconductor device 200 provided by the present invention is significantly reduced to be lower than 60 mV/dec, which is still beyond the physical limit. And thus both leakage current and power consumption are reduced.

[0022] According to the semiconductor devices provided by the present invention, the tri-layered gate-control stack is provided between the electrode layer and the substrate, and the tri-layered gate-control stack includes the FE layer (or the amorphous or fractionally crystallized dielectric layer in some conditions), the AFE layer (or the polycrystalline dielectric layer in some conditions), and the mid-gap metal layer. It is noteworthy that in the tri-layered gate-control stack, the mid-gap metal layer is always sandwiched between the FE layer and the substrate while the AFE layer is disposed on or under the dual-layered structure consisting of the FE layer and the mid-gap metal layer. Preferably, the mid-gap metal layer directly contacts the FE layer. The FE layer is provided to enhance electric fields of the electrode layer and the mid-gap metal layer is provided to homogenize the enhanced electric fields. Furthermore, the AFE layer is provided to render negative capacitance effect. The tri-layered gate-control stack is therefore used to replace conventional high-k gate dielectric layer according to the present invention, and the semiconductor device provided by the present invention obtains smaller subthreshold swing, and thus both leakage current and power consumption are reduced.

[0023] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A semiconductor device comprising:
an electrode layer disposed on the substrate; and
a tri-layered gate-control stack sandwiched between the substrate and the electrode layer, the tri-layered gate-control stack comprising:
an anti-ferroelectric (AFE) layer disposed on the substrate;
a mid-gap metal layer sandwiched between the AFE layer and the substrate; and
a ferroelectric layer sandwiched between the AFE layer and the mid-gap metal layer.

2. The semiconductor device according to claim 1, wherein the electrode layer comprises at least a work function metal layer.

3. The semiconductor device according to claim 1 further comprising an oxide liner layer sandwiched between the mid-gap metal layer of the tri-layered gate-control stack and the substrate.

4. The semiconductor device according to claim 1, wherein the ferroelectric layer comprises a material selected from the group consisting of lead zirconate titanate (Pb(Zr,Ti)O₃, PZT), lead lanthanum zirconate titanate (PbLa(Ti,Zr)O₃, PLZT), strontium bismuth tantalite (SrBi₂Ta₂O₉, SBT), bismuth lanthanum titanate ((BiLa)₂Bi₂O₅₂, BLT), and barium strontium titanate (BaSrTiO₃, BST).

5. The semiconductor device according to claim 1, wherein the mid-gap metal layer comprises metal nitride.

6. The semiconductor device according to claim 1, wherein the AFE layer comprises a material selected from the group consisting of lead indium niobate (Pb(InNb)O₃), niobium-sodium oxide (NbNaO₃), lead zirconate (ZrPbO₃), lead lanthanum zirconate titanate (Ti(Zr,La)₂Pb₃O₁₂), lead zirconate titanate (TiZrO₃), ammonium dihydrogen phosphate (NH₄H₂PO₄, ADP), and ammonium dihydrogen arsenate (NH₄I₂AsO₄, ADA).

7. The semiconductor device according to claim 1, further comprising a bottom barrier layer and an etch stop layer sandwiched between the tri-layered gate-control stack and the electrode layer.
8. The semiconductor device according to claim 1, wherein the tri-layered gate-control stack comprises a U shape.

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