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[Continued on next page]

(54) Title: MULTIPLE PIN PROBES WITH SUPPORT FOR PERFORMING PARALLEL MEASUREMENTS

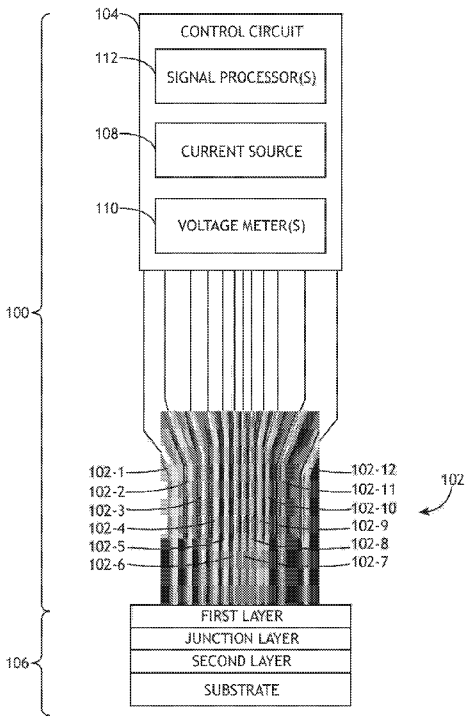


FIG.1

(57) Abstract: Multiple pin probes and methods for controlling such multiple pin probes to support parallel measurements are disclosed. The method may include: establishing electrical contact between a multiple pin probe and a subject of measurement; selecting two pins out of a plurality of pins included in the multiple pin probe as current-carrying pins; selecting more than two additional pins out of the plurality of pins included in the multiple pin probe as voltage-metering pins; injecting a current through the current-carrying pins; simultaneously measuring voltage signals through the voltage-metering pins; calculating a simulated a voltage distribution curve at least partially based on the voltage signals simultaneously measured through the voltage-metering pins; and determining one or more processor monitor parameters of the subject of measurement at least partially based on the simulated voltage distribution curve.

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MULTIPLE PIN PROBES WITH SUPPORT FOR PERFORMING PARALLEL MEASUREMENTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Application Serial No. 62/154,233, filed April 29, 2015. Said U.S. Provisional Application Serial No. 62/154,233 is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The disclosure generally relates to the field of measurement devices, and particularly to measurement devices using multiple pin probes.

BACKGROUND

[0003] A multiple pin probe is a probe that includes multiple pins. A measurement technique commonly referred to as current in-plane tunneling, or CIPT, uses multiple pin probes to take measurements of magnetic tunnel junction resistance.

[0004] More specifically, current in-plane tunneling takes measurements in multiple measurement steps. Each measurement step commences by selecting four of the pins in a multiple pin probe. Two of the selected pins are coupled to current sources and the other two of the selected pins are coupled to voltage meters. Current is passed through the two current-carrying pins and voltage is measured through the two voltage-metering pins. This measurement step is then repeated multiple times (with different selection/coupling of four pins in each measurement step) to extract the magnetic tunnel junction resistance.

[0005] It is noted that the repetitive nature of the current in-plane tunneling measurement process means that the measurement steps are performed at different times. It also requires a relative long period of time to complete the measurement process (e.g., in eight or more measurement steps), during which the pins may change positions, leading to measurement variations and inaccuracies.

SUMMARY

[0006] An embodiment of the present disclosure is directed to a system. The system may include a multiple pin probe having N-number of pins, where N is greater than four. The system may also include a control circuit configured to measure a subject of measurement utilizing the multiple pin probe. The control circuit may be configured to: select two current-carrying pins out of the N-number of pins included in the multiple pin probe; select more than two voltage-metering pins out of the N-number of pins included in the multiple pin probe; inject a current through the two current-carrying pins; simultaneously measure voltage signals through the more than two voltage-metering pins; calculate a simulated voltage distribution curve at least partially based on the voltage signals simultaneously measured through the more than two voltage-metering pins; and determine one or more processor monitor parameters of the subject of measurement at least partially based on the simulated voltage distribution curve.

[0007] A further embodiment of the present disclosure is directed to a system. The system may include a multiple pin probe having N-number of pins, where N is greater than four. The system may also include a control circuit configured to measure junction parameters of a subject of measurement utilizing the multiple pin probe. The control circuit mya be

configured to: select two current-carrying pins out of the N-number of pins included in the multiple pin probe; select more than two voltage-metering pins out of the N-number of pins included in the multiple pin probe; inject a current through the two current-carrying pins; simultaneously measure voltage signals through the more than two voltage-metering pins; calculate a simulated voltage distribution curve at least partially based on the voltage signals simultaneously measured through the more than two voltage-metering pins; and extracting one or more junction parameters of the subject of measurement at least partially based on the simulated voltage distribution curve.

[0008] An additional embodiment of the present disclosure is directed to a method. The method may include: establishing electrical contact between a multiple pin probe and a subject of measurement; selecting two pins out of a plurality of pins included in the multiple pin probe as current-carrying pins; selecting more than two additional pins out of the plurality of pins included in the multiple pin probe as voltage-metering pins; injecting a current through the current-carrying pins; simultaneously measuring voltage signals through the voltage-metering pins; calculating a simulated a voltage distribution curve at least partially based on the voltage signals simultaneously measured through the voltage-metering pins; and determining one or more processor monitor parameters of the subject of measurement at least partially based on the simulated voltage distribution curve.

[0009] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not necessarily restrictive of the present disclosure. The accompanying drawings, which are incorporated in and constitute a part of the

specification, illustrate subject matter of the disclosure. Together, the descriptions and the drawings serve to explain the principles of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The numerous advantages of the disclosure may be better understood by those skilled in the art by reference to the accompanying figures in which:

FIG. 1 is a block diagram depicting a measurement system configured in accordance an embodiment of with the present disclosure;

FIG. 2 is another block diagram depicting the measurement system configured in accordance an embodiment of with the present disclosure; and

FIG. 3 is a flow diagram depicting a measurement method configured in accordance an embodiment of with the present disclosure.

DETAILED DESCRIPTION

[0011] Reference will now be made in detail to the subject matter disclosed, which is illustrated in the accompanying drawings.

[0012] Embodiments in accordance with the present disclosure are directed to multiple pin probes and methods for controlling such multiple pin probes to support parallel measurements. It is contemplated that performing parallel measurements helps improve measurement efficiency and accuracy.

[0013] Referring generally to FIGS. 1 and 2, simplified block diagrams of a measurement system 100 configured in accordance with an embodiment of the present disclosure are shown. It is noted that the block diagrams shown

in FIGS. 1 and 2 have been simplified for illustrative purposes. It is to be understood that the measurement system 100 may utilize various types of amplifiers, filters, signal converters, and/or gain controllers along the signal paths as needed without departing from the spirit and scope of the present disclosure.

[0014] The measurement system 100 configured in accordance with an embodiment of the present disclosure includes a multiple pin probe 102 communicatively coupled with a control circuit 104. The multiple pin probe 102 includes N-number of pins, where N is greater than 4. In some embodiments, the multiple pin probe 102 may include 12 pins denoted as pins 102-1 through 102-12 in FIG. 1. The distances between adjacent pins in the multiple pin probe 102 may be non-uniform and may vary from relatively narrow (e.g., in the order of 1 μm) to relatively wide (e.g., in the order of 10 μm or greater). It is to be understood that the 12-pin configuration depicted in FIG. 1 is merely exemplary and is not meant to be limiting. It is contemplated that the multiple pin probe 102 may include different number of pins, and the pins may be spaced at various distances apart from each other, without departing from the spirit and scope of the present disclosure.

[0015] While specific implementations of the multiple pin probe 102 may vary, it is noted that the pins of the multiple pin probe 102 are configured in a manner that allows them to simultaneously contact a subject of measurement (e.g., a wafer) 106 during a measurement process. Allowing the pins of the multiple pin probe 102 to simultaneously contact the wafer 106 enables the multiple pin probe 102 to support parallel measurements of the wafer 106. Performing multiple measurements in parallel may lead to improved measurement efficiency and accuracy.

[0016] In some embodiments, the control circuit 104 of the multiple pin probe 102 is configured (e.g., using a multiplexer or the like) to select two of the N-number of pins as current-carrying pins. The control circuit 104 may couple the two current-carrying pins to a current source 108 and couple the rest of the pins (up to N-2 of them) to multiple voltage meters 110 (with respect to a common ground, or a common pin). This coupling allows the voltages to be measured simultaneously at multiple voltage meters 110 when a current is injected, effectively performing multiple measurements in parallel.

[0017] More specifically, for illustrative purposes, suppose the pins 102-5 and 102-8 shown in FIG. 1 are selected to be current-carrying pins. The control circuit 104 may couple the pins 102-5 and 102-8 to the current source 108 and couple the other ten pins (102-1 through 102-4, 102-6, 102-7, and 102-9 through 102-12) to their respective voltage meters 110. It is noted that because the pins 102-1 through 102-4, 102-6, 102-7, and 102-9 through 102-12 (collectively referred to as voltage-metering pins) are distributed at variable distances away from the current-carrying pins (with some voltage-metering pins very close to the current-carrying pins and some far away from the current-carrying pins), the voltages measured at the various voltage meters 110 may provide adequate information to help a signal processor 112 (which may include one or more dedicated processing devices, application-specific integrated circuits (ASICs), digital signal processors (DSPs), field-programmable gate arrays (FPGAs), or various other types of processors or processing devices) to extract tunneling junction resistance of the top (first) layer, the junction layer, and/or the bottom (second) layer of the wafer 106 all at once.

[0018] FIG. 3 is a more detailed flow diagram depicting the parallel measurement process/method 300 performed using the multiple pin probe

102. As shown in FIG. 3, electrical contact between the multiple pin probe 102 and the surface of the wafer 106 is established in a step 302. Two of the pins in the multiple pin probe 102 are selected as current-carrying pins, which are coupled to the current source 108 in a step 304. At least some (or all) of the rest of the pins in the multiple pin probe are selected as voltage-metering pins, which are coupled to one or more voltage meters 110 in a step 306. In some embodiments, the voltage meters may include one or more lock-in amplifiers. It is contemplated, however, that the implementations of the voltage meters may vary without departing from the spirit and scope of the present disclosure.

[0019] With the current-carrying pins and the voltage-metering pins selected, a predefined current can be injected through the current-carrying pins in a step 308. Voltage signals can be metered in a step 310, and the voltage signals in terms of amplitude and phase angle (I,Q) can be read out simultaneously for the various voltage-metering pins distributed around the current-carrying pins. The results obtained in the step 310 can then be utilized in a step 312 to calculate a simulated voltage distribution curve with junction parameters (e.g., resistance of the top layer, the junction layer, and/or the bottom layer), probe parameters (e.g., spacing, spacing deviation, contact size and contact conductivity), as well as various other types of parameters (e.g., including test pad parameter indicating whether it is a monitor wafer without pad size limitation, or it is a limited pad size or the like). Values of some of these parameters (e.g., the junction parameters) can be determined based on the simulated voltage distribution curve and reported as process monitor parameters in a step 314.

[0020] It is noted that by effectively performing multiple measurements in parallel, the measurement method 300 is able to shorten the measurement time. The measurement method 300 is also able to reduce measurement

errors caused by probe spacing vibrations. The measurement method 300 may further prolong the lifetime of the multiple pin probe (due to reduced contact time) and may reduce the current distribution range requirement for measurement on small pads.

[0021] It is noted that the measurement method 300 can also be configured to repeat the steps 304 through 312 more than once. In some embodiments, different current-carrying pins and voltage-metering pins are selected when the steps 304 through 312 are repeated to obtain one or more additional voltage distribution curves. These additional voltage distribution curves can be used for arbitrary probe position error correction in the fitting process, which may further improve the measurement accuracy. In some embodiments, pins that are selected as current-carrying pins are also selected as voltage-metering pins at some point during the measurement process.

[0022] Furthermore, in some embodiments, selection of the current-carrying pins is limited to be around the middle pins of the multiple pin probe 102. Such a limitation may help reduce the voltage distribution area, allowing the multiple pin probe 102 to be better suited for measuring a finite size pad on a patterned wafer. Alternatively, in some embodiments, pins that are spaced farther apart from each other may be selected as the current-carrying pins, and the pins located between the current-carrying pins may be selected as the voltage-metering pins. In some embodiments, sample size effect and probe contact size effect can be simulated and utilized to modify the voltage distribution, which may help further improve the measurement accuracy and prolong the lifetime of the multiple pin probe 102.

[0023] It is contemplated that the advantages provided by the measurement systems and the measurement methods configured in accordance with the present disclosure may be appreciated in various applications. It is contemplated that while some of the examples above referred to certain specific parameters (e.g., the junction parameters), the systems and methods configured in accordance with the present disclosure are applicable to obtain measurements of other types of parameters without departing from the spirit and scope of the present disclosure. In addition, it is contemplated that the term wafer used in the present disclosure may include a thin slice of semiconductor material used in the fabrication of integrated circuits and other devices, as well as other thin polished plates such as magnetic disc substrates, gauge blocks and the like.

[0024] It is contemplated that the measurement methods configured in accordance with the present disclosure may be implemented in various measurement tools as sets of instructions executed by one or more processors, through a single production device, and/or through multiple production devices. Further, it is understood that the specific order or hierarchy of steps in the methods disclosed are examples of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the method can be rearranged while remaining within the scope and spirit of the disclosure. The accompanying method claims present elements of the various steps in a sample order, and are not necessarily meant to be limited to the specific order or hierarchy presented.

[0025] It is believed that the systems and methods of the present disclosure and many of its attendant advantages will be understood by the foregoing description, and it will be apparent that various changes may be made in

the form, construction and arrangement of the components without departing from the disclosed subject matter or without sacrificing all of its material advantages. The form described is merely explanatory.

CLAIMS

What is claimed is:

1. A system, comprising:

a multiple pin probe having N-number of pins, where N is greater than four; and

a control circuit configured to measure a subject of measurement utilizing the multiple pin probe, the control circuit configured to:

select two current-carrying pins out of the N-number of pins included in the multiple pin probe;

select more than two voltage-metering pins out of the N-number of pins included in the multiple pin probe;

inject a current through the two current-carrying pins;

simultaneously measure voltage signals through the more than two voltage-metering pins;

calculate a simulated voltage distribution curve at least partially based on the voltage signals simultaneously measured through the more than two voltage-metering pins; and

determine one or more processor monitor parameters of the subject of measurement at least partially based on the simulated voltage distribution curve.

2. The system of claim 1, wherein distances between adjacent pins included in the multiple pin probe are different.

3. The system of claim 1, wherein the more than two voltage-metering pins include all N-number of pins included in the multiple pin probe except for the two current-carrying pins.

4. The system of claim 3, wherein the multiple pin probe includes 12 pins.

5. The system of claim 1, wherein the control circuit comprises a plurality of voltage meters configured to simultaneously measure voltage signals through the more than two voltage-metering pins.

6. The system of claim 5, wherein the plurality of voltage meters includes a plurality of lock-in amplifiers operating in parallel.

7. The system of claim 1, wherein the control circuit is further configured to:

change selections of the two current-carrying pins and the more than two voltage-metering pins to repeat the measurement utilizing the multiple pin probe.

A system, comprising:

a multiple pin probe having N-number of pins, where N is greater than four; and

a control circuit configured to measure junction parameters of a subject of measurement utilizing the multiple pin probe, the control circuit configured to:

select two current-carrying pins out of the N-number of pins included in the multiple pin probe;

select more than two voltage-metering pins out of the N-number of pins included in the multiple pin probe;

inject a current through the two current-carrying pins;

simultaneously measure voltage signals through the more than two voltage-metering pins;

calculate a simulated voltage distribution curve at least partially based on the voltage signals simultaneously measured through the more than two voltage-metering pins; and

extracting one or more junction parameters of the subject of measurement at least partially based on the simulated voltage distribution curve.

8. The system of claim 8, wherein the subject of measurement is a semiconductor wafer, and wherein the one or more junction parameters include a resistance of a junction layer of the semiconductor wafer.

9. The system of claim 8, wherein distances between adjacent pins included in the multiple pin probe are different.

10. The system of claim 8, wherein the more than two voltage-metering pins include all N-number of pins included in the multiple pin probe except for the two current-carrying pins.

11. The system of claim 11, wherein the multiple pin probe includes 12 pins.

12. The system of claim 8, wherein the control circuit comprises a plurality of voltage meters configured to simultaneously measure voltage signals through the more than two voltage-metering pins.

13. The system of claim 13, wherein the plurality of voltage meters includes a plurality of lock-in amplifiers operating in parallel.

14. The system of claim 8, wherein the control circuit is further configured to:

change selections of the two current-carrying pins and the more than two voltage-metering pins to repeat the measurement utilizing the multiple pin probe.

15. A method, comprising:

establishing electrical contact between a multiple pin probe and a subject of measurement;

selecting two pins out of a plurality of pins included in the multiple pin probe as current-carrying pins;

selecting more than two additional pins out of the plurality of pins included in the multiple pin probe as voltage-metering pins;

injecting a current through the current-carrying pins;

simultaneously measuring voltage signals through the voltage-metering pins;

calculating a simulated a voltage distribution curve at least partially based on the voltage signals simultaneously measured through the voltage-metering pins; and

determining one or more processor monitor parameters of the subject of measurement at least partially based on the simulated voltage distribution curve.

16. The method of claim 16, wherein the multiple pin probe includes more than four pins.

17. The method of claim 17, wherein distances between adjacent pins included in the multiple pin probe are different.

18. The method of claim 18, wherein the voltage-metering pins include all of the pins included in the multiple pin probe except for the current-carrying pins.

19. The method of claim 16, further comprising:

selecting two different pins out of the plurality of pins included in the multiple pin probe as new current-carrying pins;

selecting more than two different additional pins out of the plurality of pins included in the multiple pin probe as new voltage-metering pins; and

repeating the injecting step, the measuring step, the calculating step, and the determining step utilizing the new current-carrying pins and the new voltage-metering pins.

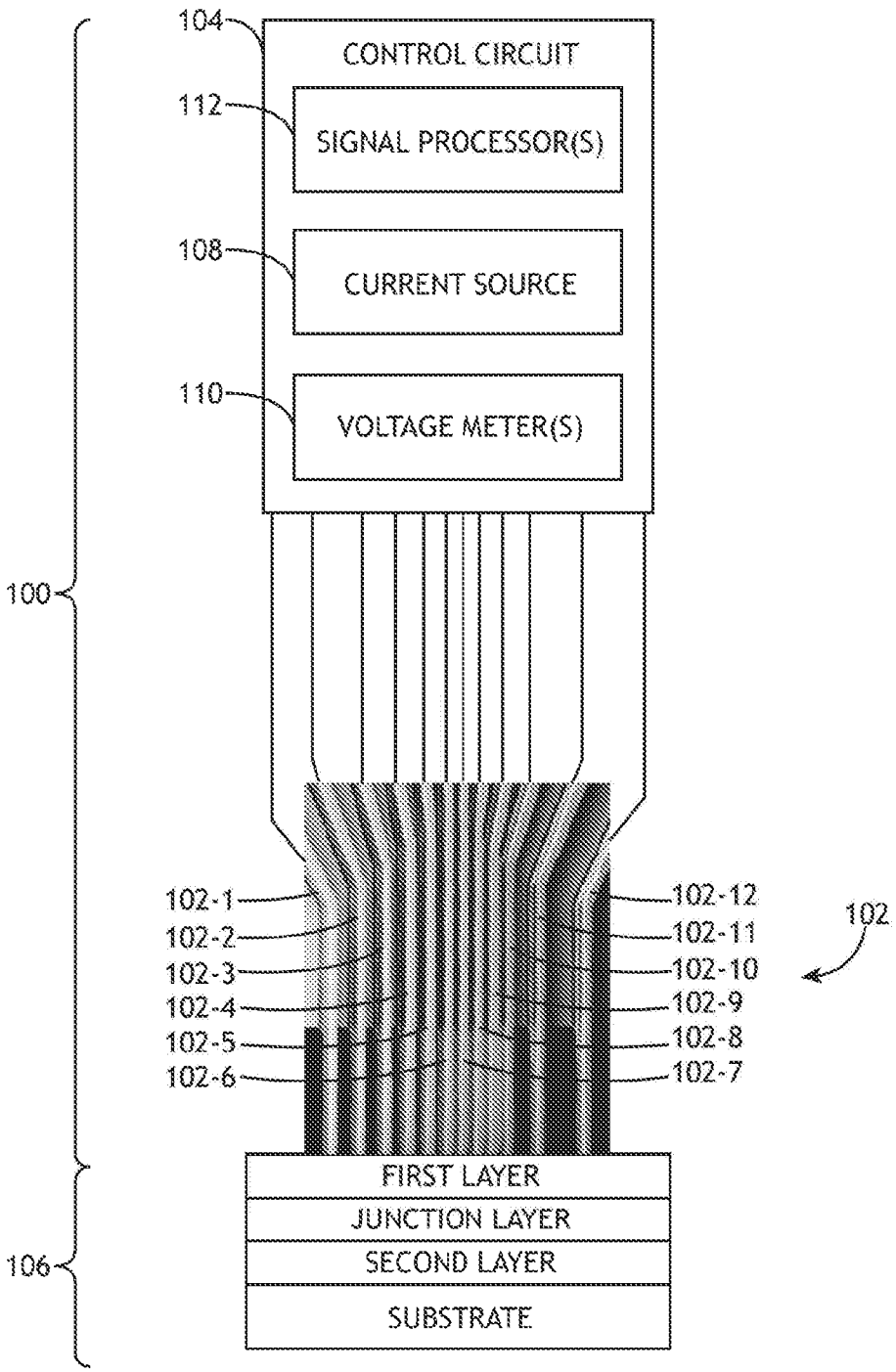

104
CONTROL CIRCUIT
112
SIGNAL PROCESSOR(S)
108
CURRENT SOURCE
110
VOLTAGE METER(S)
100
102-1
102-2
102-3
102-4
102-5
102-6
102-12
102-11
102-10
102-9
102-8
102-7
102
FIRST LAYER
JUNCTION LAYER
SECOND LAYER
SUBSTRATE
106

FIG.1

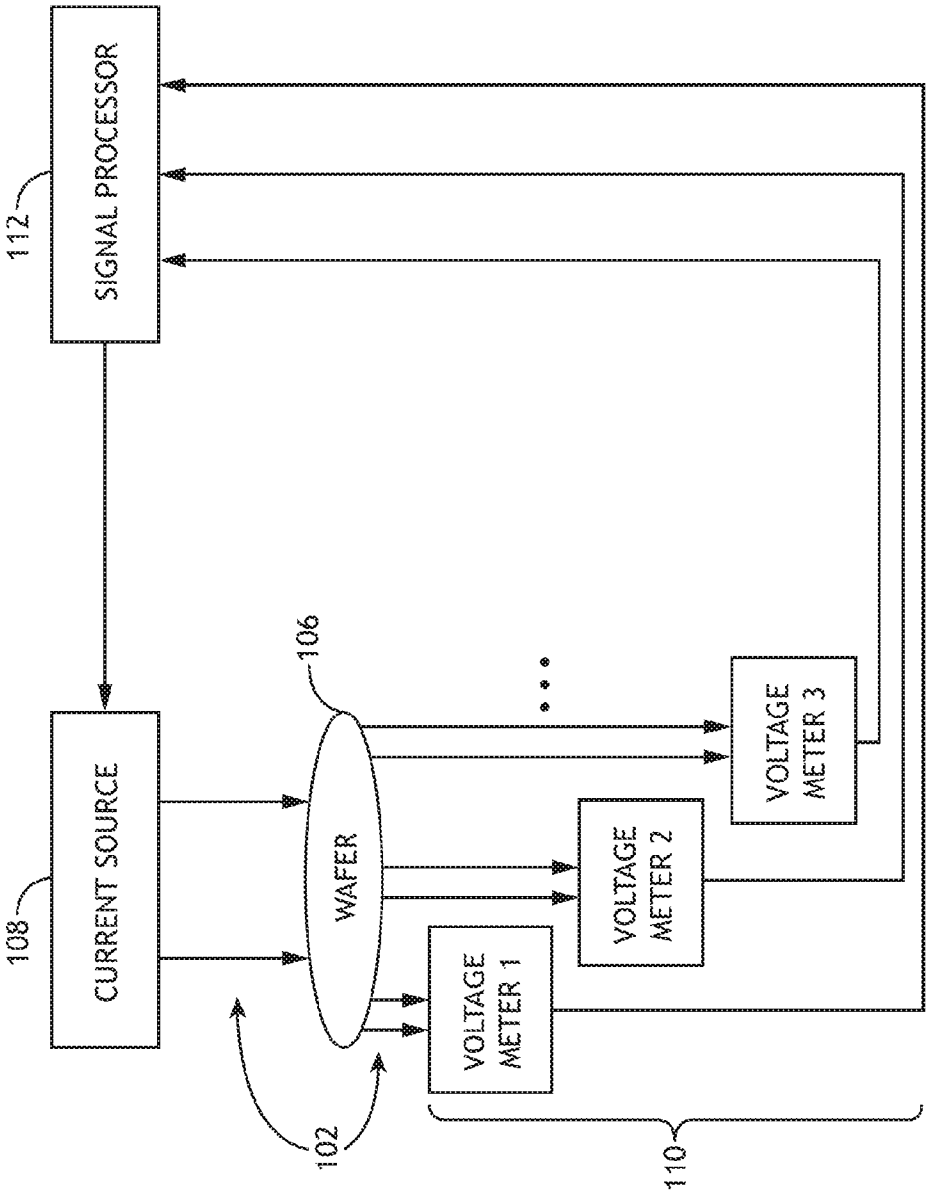

SIGNAL PROCESSOR
112
CURRENT SOURCE
108
WAFER
106
VOLTAGE METER 1
VOLTAGE METER 2
VOLTAGE METER 3
102
110

FIG. 2

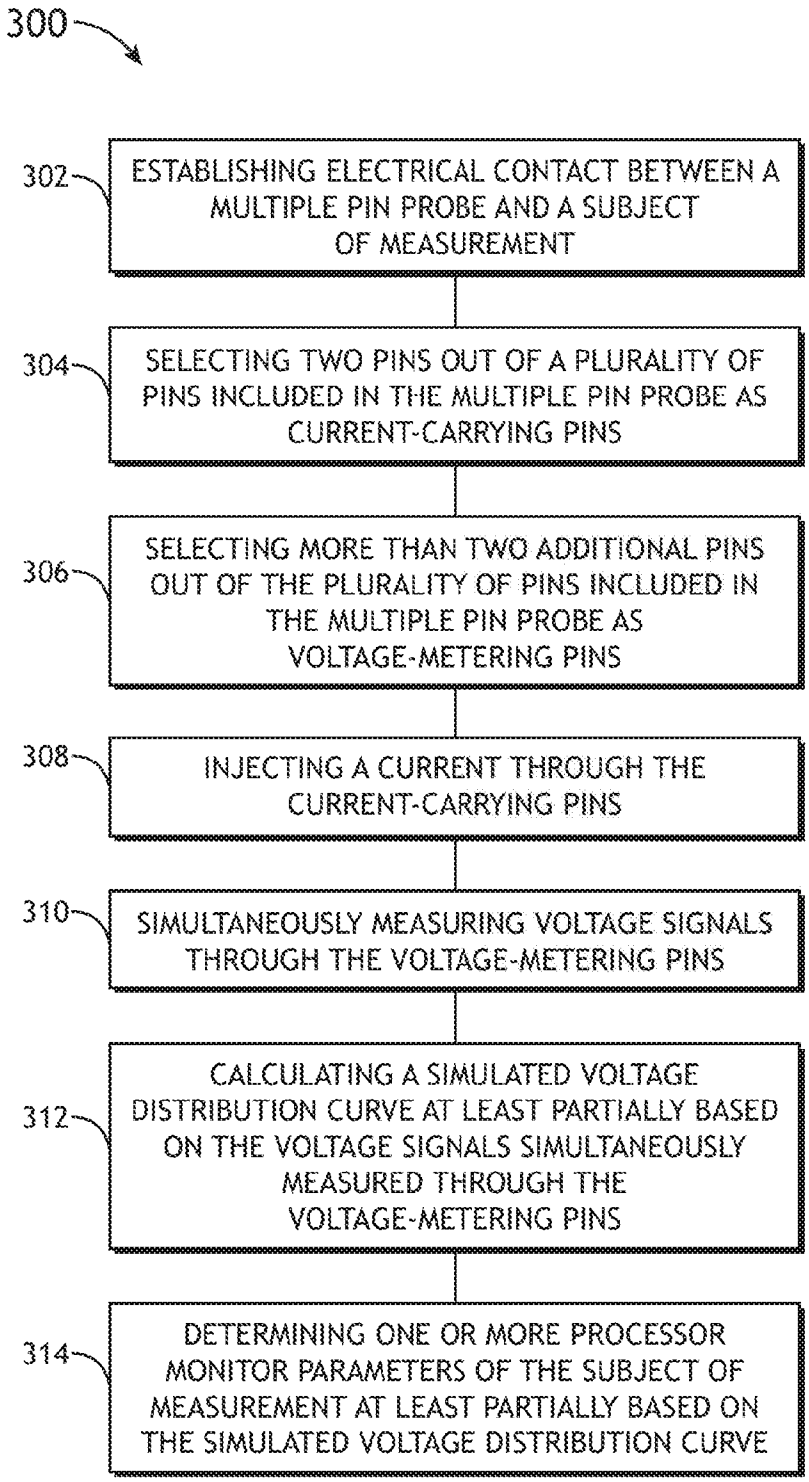

300
302
ESTABLISHING ELECTRICAL CONTACT BETWEEN A MULTIPLE PIN PROBE AND A SUBJECT OF MEASUREMENT
304
SELECTING TWO PINS OUT OF A PLURALITY OF PINS INCLUDED IN THE MULTIPLE PIN PROBE AS CURRENT-CARRYING PINS
306
SELECTING MORE THAN TWO ADDITIONAL PINS OUT OF THE PLURALITY OF PINS INCLUDED IN THE MULTIPLE PIN PROBE AS VOLTAGE-METERING PINS
308
INJECTING A CURRENT THROUGH THE CURRENT-CARRYING PINS
310
SIMULTANEOUSLY MEASURING VOLTAGE SIGNALS THROUGH THE VOLTAGE-METERING PINS
312
CALCULATING A SIMULATED VOLTAGE DISTRIBUTION CURVE AT LEAST PARTIALLY BASED ON THE VOLTAGE SIGNALS SIMULTANEOUSLY MEASURED THROUGH THE VOLTAGE-METERING PINS
314
DETERMINING ONE OR MORE PROCESSOR MONITOR PARAMETERS OF THE SUBJECT OF MEASUREMENT AT LEAST PARTIALLY BASED ON THE SIMULATED VOLTAGE DISTRIBUTION CURVE

FIG.3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/029818

A. CLASSIFICATION OF SUBJECT MATTER

G01R 1/073(2006.01)i, G01R 3/00(2006.01)i, G01R 15/12(2006.01)i, G01R 27/00(2006.01)i, G01R 33/09(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R 1/073; G01R 1/067; G01R 31/3181; G01R 31/02; G01R 33/02; G01R 3/00; G01R 15/12; G01R 27/00; G01R 33/09

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: multiple, pin, probe, voltage-metering, current-carrying, resistance, parameter

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008-0290882 A1 (ROGERS et al.) 27 November 2008 See paragraphs [25],[36],[63]-[72],[123],[136], claim 1 and figures 4,8,16,18.	1-20
Y	US 2009-0085592 A1 (COOPER et al.) 02 April 2009 See paragraph [39] and figures 9B,11A-11C.	1-20
A	WO 00-03252 A2 (CAPRES APS) 20 January 2000 See figure 7.	1-20
A	US 6246245 B1 (AKRAM et al.) 12 June 2001 See figures 5,6.	1-20
A	US 2012-0326712 A1 (TUDOSA et al.) 27 December 2012 See figures 2-3.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2016 (29.07.2016)	**29 July 2016 (29.07.2016)**

Name and mailing address of the ISA/KR
International Application Division
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Telephone No. +82-42-481-3325

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/029818

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