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Dawson et al.

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[54] **METHOD OF MANUFACTURING A PASSIVATING COMPOSITE COMPRISING A SILICON NITRIDE (Si_3N_4) LAYER AND A PHOSPHOSILICATE GLASS (PSG) LAYER FOR A SEMICONDUCTOR DEVICE LAYER**

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[73] Assignee: **RCA Corporation**, Princeton, N.J.

[21] Appl. No.: **304,347**

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Related U.S. Patent Documents

Reissue of:

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Issued: **Jun. 16, 1981**
Appl. No.: **917,106**
Filed: **Jun. 19, 1978**

[51] **Int. Cl.**[4] **H01L 21/473**

[52] **U.S. Cl.** **29/571**; 29/578; 148/187; 148/188; 148/189; 427/88; 427/94

[58] **Field of Search** 29/571, 578; 148/187, 148/188, 189; 427/94, 88

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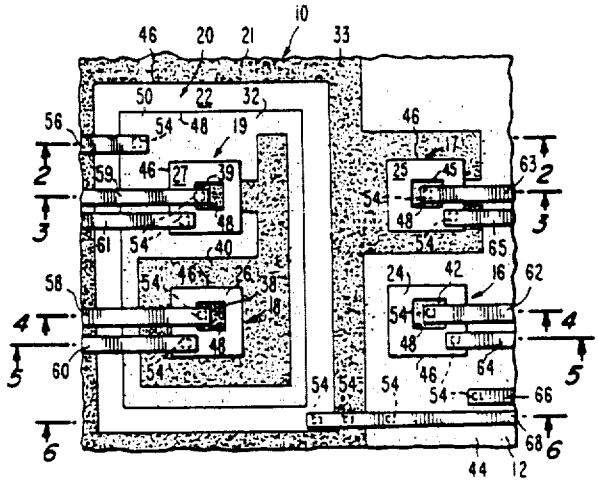
[57] **ABSTRACT**

The semiconductor device includes a layer of silicon nitride (Si_3N_4) beneath a phosphosilicate glass (PSG) layer. A silicon nitride impervious layer prevents the oxidation of underlying, exposed silicon regions during a "flow" step and any "reflow" step. Accordingly, the flow of the PSG layer can be conducted in an atmosphere containing steam, which means that the PSG layer can contain less than about 7% phosphorus by weight. The reduction of the phosphorus content of the PSG layer provides increased reliability for the semiconductor device. The method of manufacturing such a device is also disclosed.

7 Claims, 12 Drawing Figures



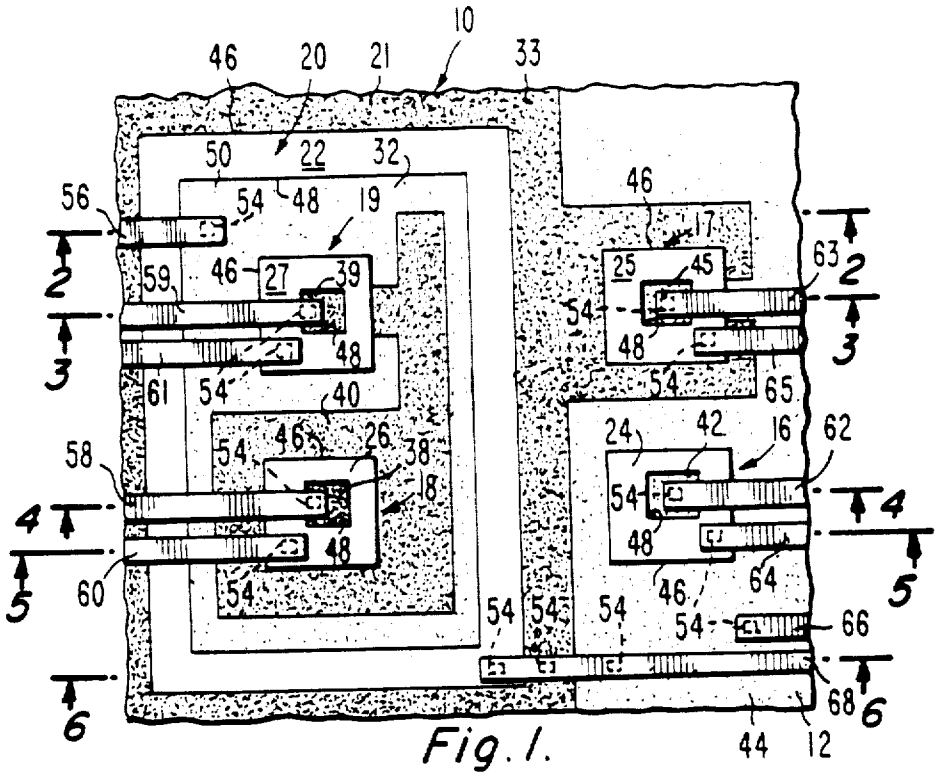


Fig. 1.

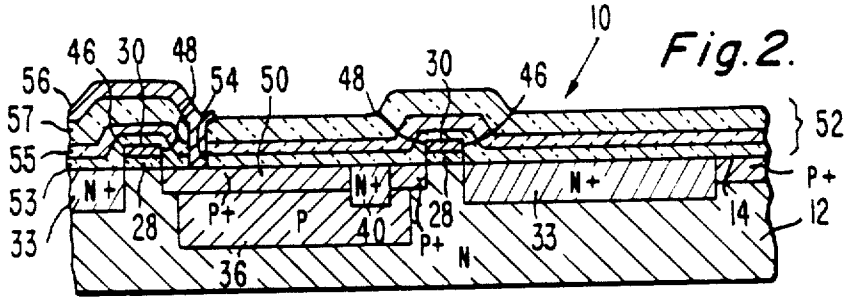


Fig. 2.

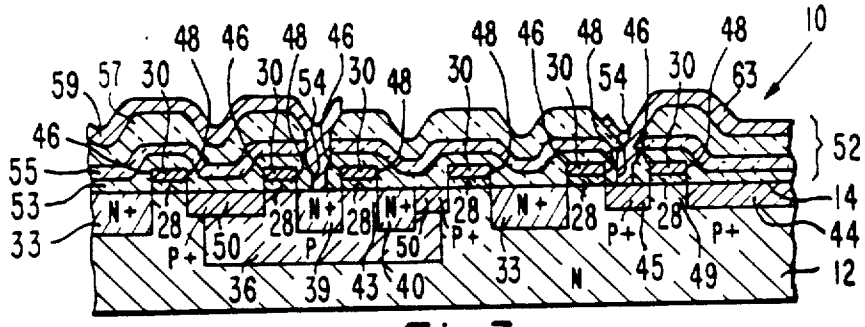


Fig. 3.

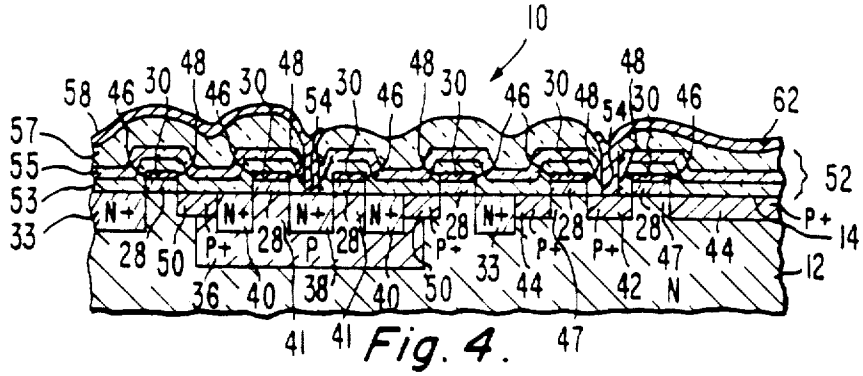


Fig. 4.

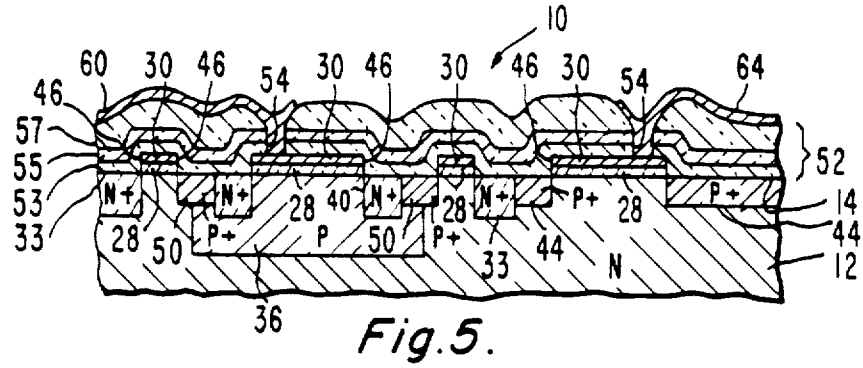


Fig. 5.

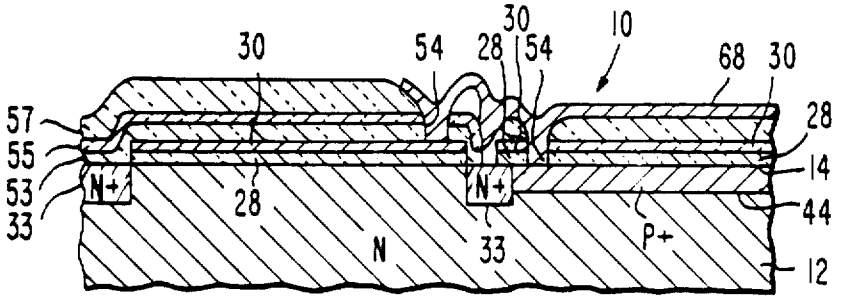


Fig. 6.

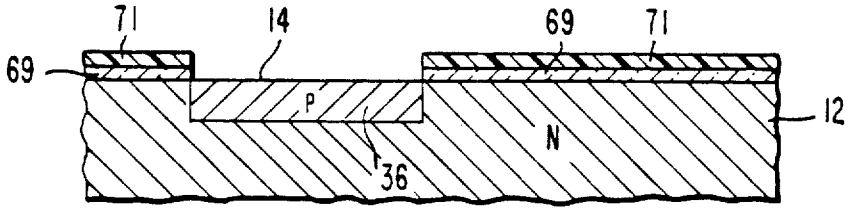


Fig. 7.

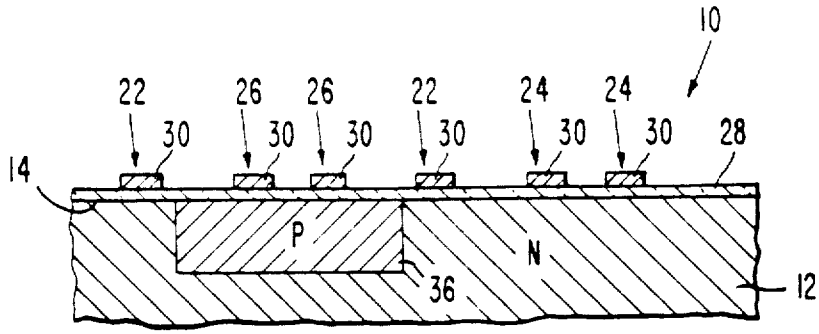


Fig. 8.

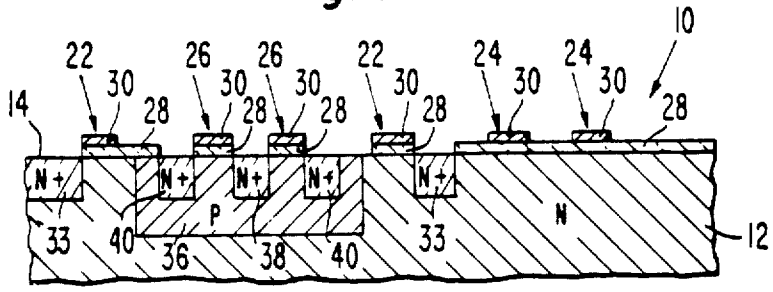


Fig. 9.

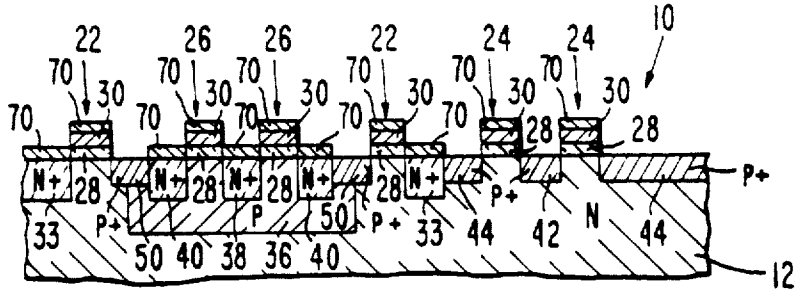


Fig. 10.

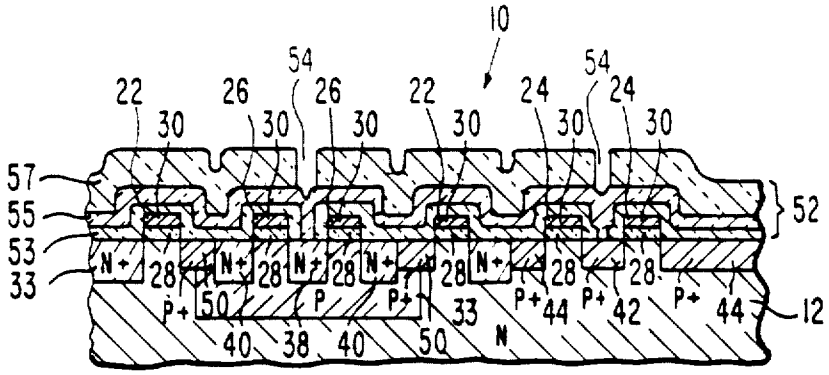

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Fig. 11.

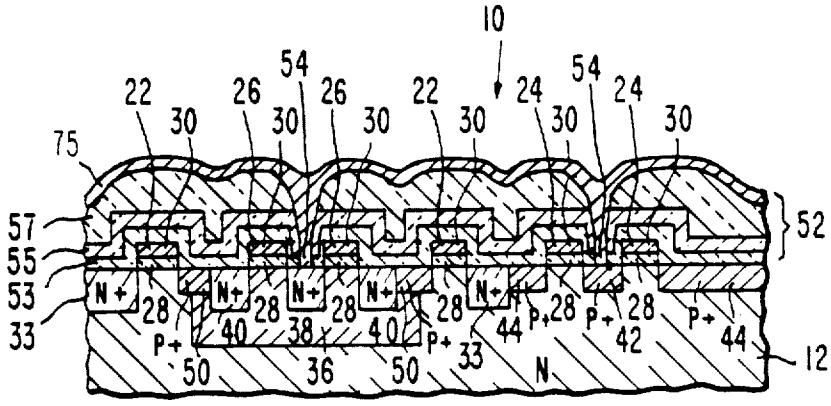
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Fig. 12.

METHOD OF MANUFACTURING A PASSIVATING COMPOSITE COMPRISING A SILICON NITRIDE (Si_3N_4) LAYER AND A PHOSPHOSILICATE GLASS (PSG) LAYER FOR A SEMICONDUCTOR DEVICE LAYER

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

The present invention relates to a composite semiconductor device including a [Si_3N4] *Si_3V_4* layer underlying a PSG layer and to the method of manufacturing such a device.

The use of a PSG layer, which is flowed over the surface of a semiconductor substrate during the manufacture of semiconductor devices, both before and after contact openings to the underlying doped semiconductor regions have been formed, has been known for several years in the semiconductor industry. Such doped, contoured, glass layers are commonly known as "reflow layers" or "reflow glasses" because of the processes used in forming such layers and after such layers have been formed. In general, the reflow glasses heretofore used have been doped with from 7–10% phosphorus, by weight. Such glasses are generally deposited onto the surface of the substrate by chemical vapor deposition and flowed over the surface of the substrate in a furnace heated to between about 1050° C. and 1075° C. into which phosphorus oxychloride ($POCl_3$) vapor is injected. During the flow step, the glass flows and sags into voids on the substrate to smooth the surface contour and round abrupt surface topologies.

As a result of the exposure to the $POCl_3$, the outer layer of glass is generally very rich in phosphorus content. Heretofore, the phosphorus rich outer layer has generally been removed by an etching step or by placing the substrate in boiling water.

Following the flow step, a photoresist layer is generally applied over the surface of the glass. The photoresist layer is then defined, and the glass is etched to form the contact openings resulting in steep walls having sharp edges at their top surface. In order to eliminate the sharp edges, a second flow step or "reflow step" is performed to smooth the sharp edges and round the steep walls in order that any metal which is deposited on the surface of the substrate will overlie smooth contours rather than sharp edges. The reflow step is usually performed in a non-oxidizing atmosphere, such as nitrogen, at temperatures between about 1050° C. and 1100° C. for a time between about 1 and 10 minutes. Higher temperatures and/or longer times are required to adequately flow PSG layers having a lower phosphorus content.

It is suspected that certain types of aluminum corrosion, which result in long term reliability problems in integrated circuit devices having aluminum metallization, are caused by phosphoric acid formed by dissolved phosphorus oxide in condensed water vapor. Accordingly, it is desirable to reduce the phosphorus doping concentration in the PSG films to below 7%. Heretofore, however, any reduction in the phosphorus doping concentration to below 7% did not provide adequate topological contouring because the PSG layer or "film" would not adequately flow.

It has been known, though, that PSG films become more fluid in the presence of water vapor. However, it has not heretofore been possible to use steam to aid in reflowing the PSG because the contact surfaces are exposed during the reflow step, and steam would cause extensive reoxidation of the silicon substrate exposed through the contact openings. In addition, any water vapor which permeated the doped glass or which reaches the silicon dioxide-silicon interface in the region of a MOS channel or field region could generate interface states which would be difficult to anneal out of the device. Accordingly, a method of making use of PSG films in which the percent of phosphorus, by weight, is less than 7%, has been desired.

The present invention relates to a method of providing PSG films having less than 7% phosphorus, by weight. Alternatively, the method can be employed in flowing PSG layers having more than 7% phosphorus, but with the flow being accomplished at lower temperatures. In accordance with the present invention, a silicon nitride layer is deposited over the surface of the semiconductor substrate prior to the deposition of the PSG film. The silicon nitride layer presents an impervious barrier to steam and prevents the oxidation of underlying semiconductor areas. Accordingly, a PSG film having a phosphorus content of less than 7%, by weight, can be applied over the surface of the silicon nitride layer and can be flowed with the aid of steam without allowing water vapor to penetrate to the silicon-silicon dioxide interface. Thus, the formation of adverse surface states and oxidation of the exposed silicon is prevented.

In addition to the advantages enumerated above, experimental results have shown that an additional synergistic advantage of providing a silicon nitride film beneath the PSG film relates to the fact that PSG films tend to have defects which lead to shorts between the aluminum metallization over them and the underlying substrate. The silicon nitride film underlying the PSG film prevents such shorts from occurring.

Another synergistic advantage which has been observed is that steam leaches the outer surface of the PSG film reducing the phosphous content thereby further reducing the possibility of a corrosion problem.

In the drawing:

FIG. 1 is a plan view of a portion of an integrated circuit device illustrating the construction of two N-channel and two P-channel insulated gate field effect transistors therein;

FIG. 2 is a cross-section taken along the line 2—2 of FIG. 1;

FIG. 3 is a cross-section taken along the line 3—3 of FIG. 1;

FIG. 4 is a cross-section taken along the line 4—4 of FIG. 1;

FIG. 5 is a cross-section taken along the line 5—5 of FIG. 1;

FIG. 6 is a cross-section taken along the line 6—6 of FIG. 1; and [p]

FIGS. 7–12 are a series of cross-sections illustrating the method of manufacturing the integrated circuit shown in FIG. 1.

In accordance with the present invention, semiconductor integrated circuits, particularly metal-oxide-semiconductor (MOS), complementary MOS (CMOS) and CMOS integrated circuits manufactured in the so-called silicon-on-sapphire (SOS) technology can be built. In addition, closed CMOS logic (C^2L) of the type

described in U.S. Pat. No. 4,063,274 issued on Dec. 13, 1977 to A. G. F. Dingwall and assigned to RCA Corporation, which patent is hereby incorporated by reference, can also be advantageously built. The advantages inherent in the present invention can therefore be employed successfully in the manufacture of MOS integrated circuits having either aluminum or other metal gates or having doped polycrystalline silicon gates of the type used in C^2L integrated circuits. In view of the fact that the present invention is intended to increase the manufacturing yield and reliability of C^2L integrated circuits and has been found to be highly beneficial in the manufacture of such integrated circuits, which employ doped polycrystalline silicon gates, the preferred embodiment of the present invention will be described with particular reference to the manufacture of a C^2L integrated circuit **10** shown in FIG. **1**. However, those skilled in the art will recognize that the present invention can be successfully employed with minor changes, which will be pointed out hereafter, in the manufacturing of integrated circuits other than C^2L, such as standard CMOS or bipolar linear integrated circuits.

The integrated circuit **10** comprises a body **12** of semiconductor material, such as silicon, which is initially of one conductivity type (N type in this example) and which has a surface **14** as shown in FIGS. **2–6**. In this example, the body **12** is bulk silicon, but other forms of semiconductor material may also be used. For example, the body **12** may be an epitaxial silicon layer on an insulating substrate as would be used in a silicon-on-sapphire (SOS) construction.

Means including the body **12**, that is source **44,40**, drains **42**, **45**, **38**, **39** and channel regions **47**, **49**, **41**, **43** in the body **12** and gate electrode means **24**, **25**, **26**, **27** on the surface **14** define two P-channel insulated gate field effect transistors (IGFETs) **16**, **17** and two N-channel IGFETs **18**, **19** together with means **20**, **21** for isolating the P-channel IGFETs **16**, **17** from the N-channel IGFETs **18**, **19**. These various means comprise a first frame-like structure **22**, hereinafter called a field shield, and other frame-like structures **24**, **25**, **26**, **27** each hereinafter called an active gate. Each of these frame-like structures includes a layer **28** (as shown in FIGS. **2–6**) of insulating material and a layer **30** of conductive material on the layer **28** of insulating material. Although the layers **28** and **30** in any one gate structure are separate from the corresponding layers in each of the other frame-like structures, the particular reference numeral is applied to each of the respective insulating and conductive layers **28**, **30** for convenience. The field shield **22** and each of the gate structures **24**, **25**, **26**, **27** has a closed geometry. However, only IGFETs **16** and **18** have channel regions which surround their drains **42**, **38**, respectively. The field shield **22** surrounds a first portion **32** of the surface **14** and is surrounded by a guardband **33** and by a second portion **21** of the surface **14**. The active gates **26**, **27** are disposed on the first portion **32** of the surface **14**.

A well region **36** of conductivity type opposite that of the body **12**, P-type in this example, is formed in the body **12** adjacent to the first portion **32** of the surface **14**. Regions **38**, **39** of N+ type conductivity are within the P-well region **36** adjacent to portions of the surface **14** which are surrounded by the active gates **26**, **27** respectively. Another region **40** of N+ type conductivity is within the P-well region **36** adjacent to a portion of the surface **14** which surrounds the active gate **26** and a portion of the active gate **27**. The regions **38** and **40** define the ends of a channel zone **41** of the IGFET **18** as shown in FIG. **4**, and the regions **39** and **40** define the ends of a channel zone **43** for the IGFET **19** as shown in FIG. **3**.

Regions **42**, **45** of P− type conductivity are in the body **12** adjacent to portions of the surface **14** which are surrounded by the active gates **24**, **25** and another region **44** of P+ type conductivity is in the body **12** adjacent to a portion of the surface **14** which surrounds the active gates **24**, **25**. The regions **42** and **44** define the ends of a channel zone **47** for the IGFET **16** as shown in FIG. **4**, and the regions **45** and **44** define the ends of a channel zone **49** for the IGFET **17** as shown in FIG. **3**. Each of the gate structures **24**, **25**, **26** and **27** and the field shield **22** has an inner peripheral boundary and an outer peripheral boundary. For convenience the outer peripheral boundaries of the frame-like structures are each designated by the reference numeral **46** and the inner peripheral boundaries of the frame-like structures are each designated by the reference numeral **48**. Each of the regions **32**, **21**, **38**, **39**, **42** and **45** has a surface in intercept boundary substantially contiguous to one or the other of an inner peripheral boundary **48** or an outer peripheral boundary **46**.

Means including a first portion **[42]** *32* of the surface **14** are provided for establishing ohmic contact to the well region **36**. In the preferred embodiment of the invention, the means includes a well contact region **50** of P+ conductivity having a doping concentration higher than the doping concentration of the well region **36**. The region **50** includes part of the first portion **32** of the surface **14** which lies between the field shield **22** and the active gates **26**, **27**. In this example, the region **50** surrounds the region **40** which in turn surrounds the active gate **26** but does not fully surround the active gate **27**. An insulating coating **52** overlies substantially all of the surface of the device **10** and contains apertures **54** therethrough for permitting contact to be made to the various regions and conductive layers. The coating **52**, which is the subject of the present invention comprises a three layer structure in the preferred embodiment of the invention. However, as will be more fully explained hereinafter, only two layers are necessary. In the preferred embodiment of the invention, the coating **52** comprises an insulating layer **53**, preferably of undoped silicon dioxide which overlies the surface **14** and the frame-like structures **22**, **24**, **25**, **26** and **27**. Overlying the undoped silicon dioxide layer **53** is an impervious layer **55** which cannot be penetrated by steam or oxygen. In the preferred embodiment of the invention the impervious layer **55** is comprised of silicon nitride. Overlying the silicon nitride layer **55** is a protective overcoat layer of material which provides smooth contours for the metallization pattern which will be used to interconnect the various IGFETs on the integrated circuit **10**. In the preferred embodiment of the invention, the protective overcoat layer is comprised of a PSG layer **57** having a phosphorus concentration of between 5% and 7% by weight as will be more fully explained hereinafter.

A source-substrate conductor **56** has a portion which extends through an opening **54** in contact with the P+ type region **50** as shown in FIGS. **1** and **2**. Drain conductors **58**, **59** have portions thereof extending through openings **54** into contact with the regions **38**, **39** shown in FIGS. **4** and **3** respectively. A gate conductor **60** extends through an opening **54** into contact with the

conductive layer 30 of the active gate 26 as shown in FIGS. 1 and 5, and a gate conductor 61 extends through an opening 54 and contacts the conductive layer 30 of the active gate 27. Similarly, drain conductors 62, 63 contact the regions 42, 45 of the IGFETs 16, 17 respectively as shown in FIGS. 1, 3 and 4 and gate conductors 64, 65 contact the conductive layers 30 of the active gates 24, 25, respectively, as shown in FIGS. 1 and 5. Finally, a source conductor 66 makes contact with the region 44.

The field shield 22 and the guardband 33 provide means for isolating the P-channel IGFETs 16, 17 from the N-channel IGFETs 18, 19. In the operation of the device 10, the guardband 33, the field shield 22, and the P− source plane 44 are all connected together and to the power supply V_{DD} by a power connector 68 shown in FIGS. 1 and 6, which electrically contacts the conductive layer 30 of the field shield 22, the N+ guardband 33 and the P− source plane 44 through openings 54 in the insulating coating 52. While the guardband 33 alone could provide isolation between the P-channel IGFET 16, 17 and the N-channel IGFETs 18, 19 the field shield 22 insures that if there is any break in the guardband 33 created during manufacture, the field shield 22 will act as the gate of a P-channel IGFET whose drain is the P+ region 50 and whose source is the P+ source plane 44 which is permanently biased off by the presence of the V_{DD} potential thereon through conductor 68.

The several conductors shown in FIGS. 1–6 do not interconnect IGFETs 16, 17, 18 and 19 together to perform any circuit function inasmuch as the circuit described therein is generally applicable to many different circuit configurations and is merely presented as the type of integrated circuit on which the present invention has been found to be highly beneficial.

FIGS. 7–12 illustrate the preferred embodiment of the method of manufacturing the present invention, particularly the application of the method to a bulk semiconductor body in the formation of C^2L integrated circuits. For convenience, each cross-section of FIGS. 7–12 shows only the configuration in the plane of the cross-section.

In this example, the process begins with a semiconductor body 12 of (100) silicon of N-type conductivity which has a surface 14. The first step in the present process is to grow a thermal oxide layer 69 on the surface 14. Preferably, the layer 69 is formed by heating the body 12 to a temperature of about 1100° C. in an atmosphere of steam for a time sufficient to grow the oxide layer 69 to a thickness of approximately 6000 Å.

Referring to FIG. 7, a layer of photoresist material 71 is applied over the oxide layer 69. The photoresist layer 71 is defined using a first photomask, and then the photoresist is developed to expose portions of the oxide layer 69. Next, the exposed portions of the oxide layer 69 are etched away to expose portions of surface 14. The body 12 is then placed in an ion implantation apparatus and an acceptor type impurity such as boron is implanted into the body 12. In the preferred embodiment of the invention, boron is implanted to a surface concentration of about 1.3×10^{13} atoms/cm^2, then the photoresist layer 71 is removed. Thereafter, the implanted boron is diffused into the body 12 in a furnace heated to about 1200° C. for about 16 hours in order to form the P-well region 36 which has a final acceptor concentration of about 2×10^{16} atoms boron/cm^3.

Next, the balance of the oxide layer 69 is stripped to expose the surface 14. A gate oxide layer 28 is then grown on the surface 14. Preferably, the gate oxide layer 28 is formed by heating the body 12 to a temperature of about 870° C. in an atmosphere of steam and a small quantity of HCl gas for a time sufficient to grow the oxide layer 28 to a thickness of approximately 1000 Å.

Following the growth of the oxide layer 28, the body 12 is placed in a deposition reactor and a layer 30 of [conductive] material, preferably polycrystalline silicon, is deposited thereon. Any known deposition reaction may be employed, such as the thermal decomposition of silane (SiH_4). The process is carried out for a time sufficient to form the layer 30 to a thickness of about 3500 Å. Using conventional photolithographic techniques involving a second photomask, the layer 30 is next defined into the pattern of the field shield structure 22 and the active gate structures 24, 25, 26 and 27, which remain after etching. The etch of the undesired polycrystalline material may take place in a plasma reactor containing a small amount of carbon tetrafluoride gas and nitrogen. Following the etch the remaining photoresist material is stripped, as shown in FIG. 8.

A new layer of photoresist is then applied on the surface of the wafer and a third photomask is used to define areas where N− regions will be formed. The photoresist is defined, exposed, and developed and the exposed portions of the gate oxide layer 28 are removed by etching to expose the surface 14 of the body 12. Then, the balance of the photoresist is removed, exposing the remaining polycrystalline silicon gates. The body 12 is then placed in a diffusion furnace containing phosphorus oxychloride dopant for about 5–8 minutes at 1050° C. in order to form the N+ regions 33, 38 and 40, as shown in FIG. 9 and to dope the polycrystalline silicon material 30 to N+ conductivity, making it conductive.

[The] *Referring to FIG. 10, the* portions of the oxide layer 28 which are not covered by polycrystalline silicon 30 are then removed [be] *by* etching using the polycrystalline silicon areas 30 as an etch mask. Next, the body 12 is placed in a furnace to grow a thermal oxide on the exposed surface. Oxides over N+ doped silicon grow faster than oxides over lightly doped silicon. Accordingly, in the time taken to grow a thermal oxide having a thickness of about 900 Å over the lightly doped areas, an oxide having a thickness of about 2500 Å is grown over the N+ doped areas.

Referring to FIG. [19] *10*, the oxide is then etched to remove the thinner portions and to leave a residual oxide 70 over the N+ doped areas and the polycrystalline silicon regions 30 as shown. The body 12 is then placed in a diffusion furnace heated to about 1000° C. and subjected to a boron nitride diffusion for approximately 20 minutes to form P+ regions 42, 44 and 50. The P+ diffusion is of a lower concentration than was the N+ diffusion and consequently the N+ doped polycrystalline silicon regions 30 remain N+ doped.

Following the P+ diffusion, the remaining portions of the residual oxide 70, over the N+ regions and on the polycrystalline silicon layers 30, are removed by etching. The body 12 is then placed in a furnace heated to about 870° C. in the presence of steam and HCl for about 15 minutes to reoxidize the polycrystalline silicon gates.

Next, the insulating coating 52, which includes the present invention, is formed. In forming the insulating

coating **52**, first an undoped silicon dioxide layer **53** is applied over the surface **14**. In the preferred embodiment of the invention, the undoped silicon dioxide layer is deposited by a chemical vapor deposition (CVD) to a thickness of about 1500 Å. Next, the CVD film is densified by heating it in a nitrogen (N_2) atmosphere at about 1000° C. for about 10 minutes. Using a layer of photoresist and a fourth photomask the contact openings **54** are defined and opened through the undoped silicon dioxide layer **53**.

Next, a layer of silicon nitride (Si_3N_4) **55** is deposited by the reaction of silane and ammonia at about 800° C. to a thickness of about 900 Å. The silicon nitride layer **55** is necessary to present an impervious barrier to prevent oxidation of the surface **14** which was exposed during the preceding etch step.

Following the deposition of the silicon nitride layer **55**, a PSG layer **57** having a phosphorus concentration between about 5 and 7% by weight is next deposited on the surface of the silicon nitride layer **55** at a temperature of about 400° C. The PSG layer is preferably deposited by the reaction between silane and phosphine. Following the deposition of the PSG layer **57**, contact openings **54** are formed therein coincident with the contact openings **54** previously formed in the undoped silicon dioxide layer **53**. The contact openings **54** in the PSG layer **57** are preferably etched using buffered hydrofluoric acid, which etch will essentially stop when the silicon nitride layer **55** is reached. Following the etch of the PSG layer **57**, the structure will be shown in FIG. **11** and will include sharp edges where the contact openings **54** have been formed through the PSG layer **57** and will have a topology where polycrystalline silicon lines are crossed which is very difficult to coat with metal. In order to remove the sharp edges from the PSG layer **57** and to improve the topology over the polycrystalline silicon lines, the PSG layer **57** is heated to about 1050° C. for about 15 minutes in an atmosphere containing steam. During this critical step in the processing the PSG "flows" resulting in smoothly contoured edges to which metal may be applied. It is only possible to use less than 7% phosphorus in the PSG layer **57** and still achieve adequate "flow" for relatively short time exposures at 1050° C. because of the presence of the steam in the atmosphere. It is only possible to use steam in that atmosphere because of the presence of the impervious Si_3N_4 layer **55** which prevents the thermal oxidation of contact areas lying beneath the openings **54** in the PSG layer **57**. Thus, the present invention provides a process by which a steam atmosphere may be used to flow a PSG layer which contains an adequate amount of phophorus for flow and getter purposes but which does not contain so much phosphorus that long term reliability problems, such as "black metal" problems will be created. An additional advantage of the steam flow of the PSG layer **57** is that impurities on the upper surface of the layer **57** are leached out of the layer **57** during the steam aided flow.

Following the steam aided flow step, the furnace is flushed with nitrogen [to] *for* about 5 minutes after which the body **12** is pulled into a so-called "white elephant", a tube at the end of the furnace, in which the body **12** is cooled in a nitrogen atmosphere.

Following the removal of the body **12** from the furnace, the portions of the silicon nitride layer **55** lying between the openings **54** in the undoped silicon dioxide layer **53** and the PSG layer **57** are removed by placing the body **12** into an etch solution comprising a mixture of phosphoric acid (H_3PO_4) into which there is mixed 10% or less sulfuric acid (H_2SO_4), which mixture is heated to about 180° C. for a time sufficient to extend the contact openings **54** through to the surface **14**.

Next, an anneal is performed in forming gas, a mixture of hydrogen and nitrogen, at about 740° C. for 16 hours. Following the forming gas anneal, the body **12** may be dipped into a buffered hydrofluoric acid to remove any oxide which may have formed on the surface **14**.

Next, a layer of metal [**59**] *75* such as aluminum, is evaporated over the surface of the insulating coating **52** to obtain the structure shown in FIG. **12**. Using a photolithographic process, the metal layer **59** is defined to form interconnects which connect the various IGFETs on the integrated circuit **10**. Then, a metal [protect] *protective* passivating oxide having a thickness of about 10,000 Å is formed over the surface of the entire body **12**, and bond pad openings are formed in the passivating oxide by a photolithographic process. The formation of the passivating oxide and of the bond pad openings are well known in the art and are not shown in the figures.

While the preferred embodiment of the invention has been described with reference to C^2L processing, it should be recognized that alterations to the preferred embodiment may be accomplished without departing from the spirit or scope of the invention. In particular, if additional contouring of the PSG layer **57** is desired in order to provide a smoother contour through the contact openings **54** in the silicon nitride layer **55**, the only alteration required in the process specified would be that the contact openings **54** through the undoped silicon dioxide layer **53** would not be formed until after the contact openings **54** were extended through the silicon nitride layer **55**. At that point, a reflow, i.e. a second flow of the PSG [would] *could* be performed without exposing any P+ areas to the phosphorus from the PSG layer **57**, because the undoped silicon dioxide layer **53** would act as a shield for the P+ regions. Following the reflow, the contact openings **54** could be extended through the undoped silicon dioxide layer **53** without additional photolithographic steps by placing the body into a buffered hydrofluoric acid solution and using the silicon nitride layer [**53**] *55* as an etch mask.

In view of the fact that the preferred embodiment of the present invention does not require the "reflow" step, the undoped silicon dioxide layer **53** is not absolutely required. However, by providing the layer **53**, various advantages are gained. For example, the layer **53** may be predefined in the manner discussed above to give greater control over the location of the contact openings **54** than would be provided by etching through the thick PSG layer **57**. In addition, the presence of the layer **53** provides a diffusion barrier if a "reflow" of the PSG layer is desired following the openings of the contact holes **54** through the silicon nitride layer **55**. In the event that such a "reflow" step is desired, the predefinition of the contact openings **54** through the undoped layer **53** prior to the deposition of the silicon nitride layer **55** would not be accomplished.

It is also possible to accomplish a reflow step without the use of the undoped silicon dioxide layer **53**, by following the steps enumerated above and heating the body **12** to a temperature sufficient to grow oxide on any exposed portions of the surface **14** but not sufficient to cause a reflow of the PSG layer **57**. Again, that could be accomplished without the use of the undoped silicon dioxide layer **53**.

While the reflow step is not utilized in the preferred embodiment of the invention, there may well be other processes which would be employed in the manufacturing of NMOS, PMOS or bipolar integrated circuits in which the reflow, which the present invention is capable of providing would be desirable. It should be recognized by those skilled in the art that the shield which the silicon dioxide layer **53** is capable of providing or which could alternatively be provided by the thermal oxidation portions of the surface **14** exposed through openings formed in the silicon nitride layer **55** in the manner specified above, i.e. at a temperature inadequate to cause the PSG to reflow, is only required to protect exposed regions having a P type conductivity from being counterdoped by phosphorus from the PSG layer **57**. Thus, if the present invention is being used exclusively for the purpose of making NMOS devices there would be no exposed P type regions so that the possibility of counterdoping would not exist.

In addition to the embodiments described above, and the reasons discussed heretofore for utilizing the present invention, those skilled in the art will recognize that the present invention may be used to solve other problems in the manufacture of semiconductor devices. For example, the invention may be used to contour otherwise abrupt topologies of the type which may occur in bipolar integrated [crcuits] *circuits* employing dielectric isolation. In such structures, a trench is formed in the dielectric isolation during the processing step in which the oxide overlying the finished device is stripped. While certain metals, such as gold or silver, may be electroplated consistently over such trenches, applications exist where it is beneficial to evaporate aluminum over such structures. The present invention can be used to provide contoured surfaces to which evaporated aluminum provides a more consistent covering than was heretofore possible.

The invention may also be used to contour the step which occurs in aluminum gate MOS processing. A step is formed between the thick field oxide in the field regions and the active device areas which are substantially thinner.

The invention should also be beneficial in the manufacture of high frequency transistors of the type which employ narrow metallization lines leading to small bond pads which are disposed from the surface to the semiconductor material by a thick oxide. Heretofore, a problem with such structures has involved running metallization from the high bond pads down to the narrow metallization lines along the steep walls of the oxide on which the bond pads are located. By using the present invention, a contoured region can be provided over which the metallization can be applied and delineated.

While the present invention has been discussed with regard to the advantages which it provides in allowing a PSG layer with reduced phosphorus content to be flowed, it would be obvious to those skilled in the art that while the presence of steam acts to reduce the phosphorus content required to flow a PSG layer at a given temperature, it also acts to lower the temperature at which PSG with a given phosphorus content will flow. Accordingly, the present invention is also useful in the manufacture of radiation hardened integrated circuits in which the temperature at which the integrated circuits are manufactured is kept as low as possible. Accordingly, radiation hardened integrated circuits can have a flowed PSG layer which is flowed at a temperature less than 1000° C. by providing the PSG layer with a sufficient amount of phosphorus to enable it to flow at a lower temperature in the presence of steam. For example, a PSG layer containing 10% phosphorus by weight can be flowed at about 950° C. While the 10% phosphorus content is higher than the content heretofore discussed, the invention provides a flowed PSG layer at the low temperature required for the processing of radiation hardened integrated circuits. Also, PSG layers can be provided on bipolar integrated circuits where they can be flowed at relatively low temperatures to avoid undesired lateral diffusions.

The invention is also beneficial in the manufacture of other integrated circuits which require smooth contours. An example of such integrated circuits would be those which utilize both polycrystalline gates and/or interconnects over which gold metallization is electroplated. Without the contoured surfaces provided by the invention, gold has a tendency to adhere to the steep walls of the dielectric which covers the polycrystalline [silicone] *silicon* in places where no metallization is desired. In addition, the presence of the impervious silicon nitride layer allows metallization techniques which have a relatively high degree of contamination, either in the metal or the technique of deposition, to be used in the manufacture of integrated circuits. Examples are "hot metal" deposition, i.e. the evaporation of aluminum in which the substrate is heated or "solution plating" processes.

What is claimed is:

1. An improved method of passivating an integrated circuit device of the type comprising a substrate of semiconductor material having semiconductor devices formed therein, said semiconductor devices being covered by a first layer of insulating material, the improvement comprising the steps of:

(a) forming contact openings through said first layer of insulating material;

(b) covering said first layer of insulating material [which] *with* an impervious layer of silicon nitride; then

(c) covering said impervious layer with a phosphosilicate glass layer *that contains less than about 7%* phosphorus by weight; then

(d) forming contact openings through said phosphosilicate glass layer which align with said contact openings formed through said first layer of insulating material; then

(e) heating said phosphosilicate glass layer in the presence of steam at a temperature sufficient to cause the edges of said contact openings formed in said phosphosilicate glass layer to become rounded, said temperature not being sufficient to affect said impervious layer; then

(f) extending said contact openings through those portions of said impervious layer which are exposed through the contact openings formed in the phosphosilicate glass layer; and

(g) applying a metal over the surface of said phosphosilicate glass layer, whereby said metal will extend through said contact openings to make electrical contact to underlying portions of the semiconductor material which are exposed through said contact openings.

2. The method of claim 1 further comprising the step of covering said body with a layer of material different from the material comprising said impervious layer prior to covering said body with said impervious layer.

said impervious layer capable of being preferentially etched relative to said different material.

3. The method of claim 2 further comprising the step of heating said phosphosilicate glass layer in the presence of steam at a temperature sufficient to cause said phosphosilicate glass layer to flow over the edges of said contact openings which have been formed through said impervious layer after [which such] *said* step of extending said contact openings through said impervious layer.

[4. The method of claim 1 in which said phosphosilicate glass layer contains more than about 7% phosphorus by weight and said step of heating is conducted at less than about 1000° C.]

5. The method of claim 1 wherein [said phosphosilicate glass layer contains less than about 7% phosphorus by weight and] said step of heating takes place at a temperature greater than about 950° C.

6. The method of claim 1 further comprising the steps of:

(a) heating said body in an oxidizing atmosphere after said step of extending said contact openings, said body being heated to a temperature sufficient to grow an oxide over the portions of said substrate exposed through said contact openings but insufficient to cause said phosphosilicate to flow, said oxide being grown for a time insufficient to cause it to exceed the thickness of the impervious layer; then

(b) heating said body to a higher temperature in an atmosphere containing [stem] *steam* in order to cause said phosphosilicate glass layer to flow over the [edge] *edges* of said contact openings in said impervious layer; then

(c) removing the portions of semiconductor oxide grown in step (a).

7. The method of claim 1 wherein said impervious layer is a silicon nitride layer and said step of covering said body with an impervious layer comprises the step of a chemical vapor deposition of silicon nitride at a temperature of about 800° C.

8. The method of claim 1 wherein said step of heating said phosphosilicate glass layer is conducted at a temperature of about 1050° C.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : Re. 32,351

DATED : Feb. 17, 1987

INVENTOR(S) : Robert H. Dawson et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Title - remove "$SI_1 3N_4$" and insert --Si_3N_4--.

- after "SEMICONDUCTOR DEVICE" remove --LAYER--.

Claim 1, line 44, "phosphorus by weight" should be in italics.

Signed and Sealed this

Twenty-sixth Day of April, 1988

Attest:

Attesting Officer

DONALD J. QUIGG

Commissioner of Patents and Trademarks