United States Patent

Kadow

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[54] MEMORY ARRANGEMENT

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[30] **Foreign Application Priority Data**

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[51] **Int. Cl.** **G11c 7/00**, G11c 11/06

[58] **Field of Search** ..... 340/174 M

[56] **References Cited**

UNITED STATES PATENTS

3,439,352	4/1969	Fischer	340/174
3,579,209	5/1971	Gilligan	340/174 M
3,110,888	11/1963	Kluck	340/174 M
3,436,750	4/1969	Bakker	340/174 M
3,492,664	1/1970	Klett	340/174 M

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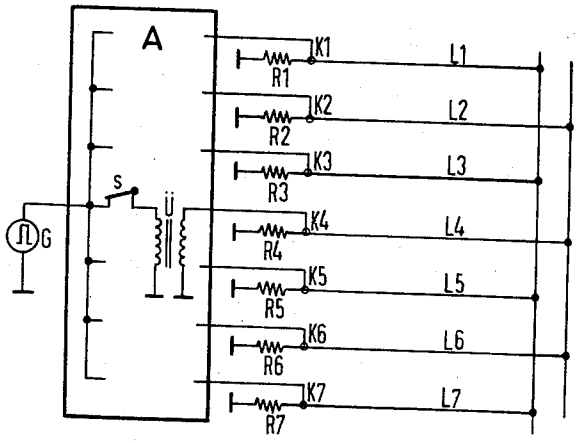
[57] **ABSTRACT**

A memory system having a plurality of control lines, to individual lines of which impulses from a source of constant current may be selectively applied, each line being provided with inductive feed, and having a termination at the feed end thereof at least corresponding approximately with its wave resistance, the other ends of the parallel control lines being interconnected at least in groups with return flow being effected over other of associated lines whereby such connecting points are not led to a ground or other specific return line to improve the characteristics of the control lines as wave conductors and shorten the buildup processes associated with the return current, and thereby achieve an increase in operating speeds.

6 Claims, 3 Drawing Figures



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2 Sheets-Sheet 1

FIG. 1

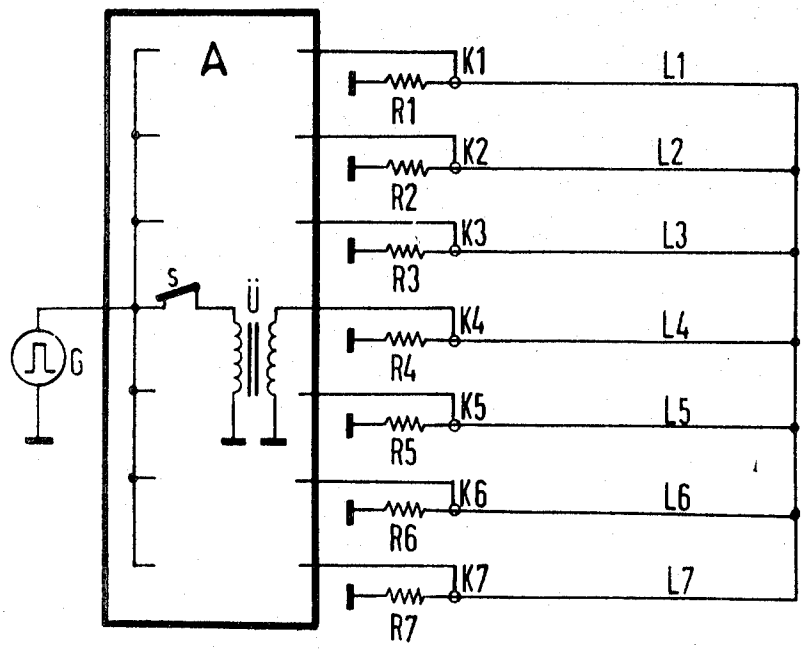

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Fig. 2

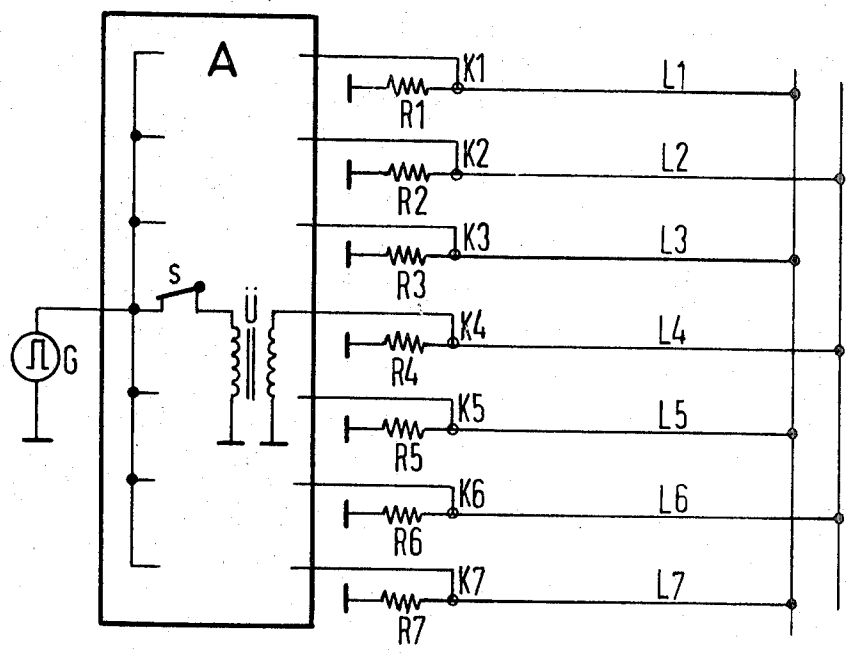
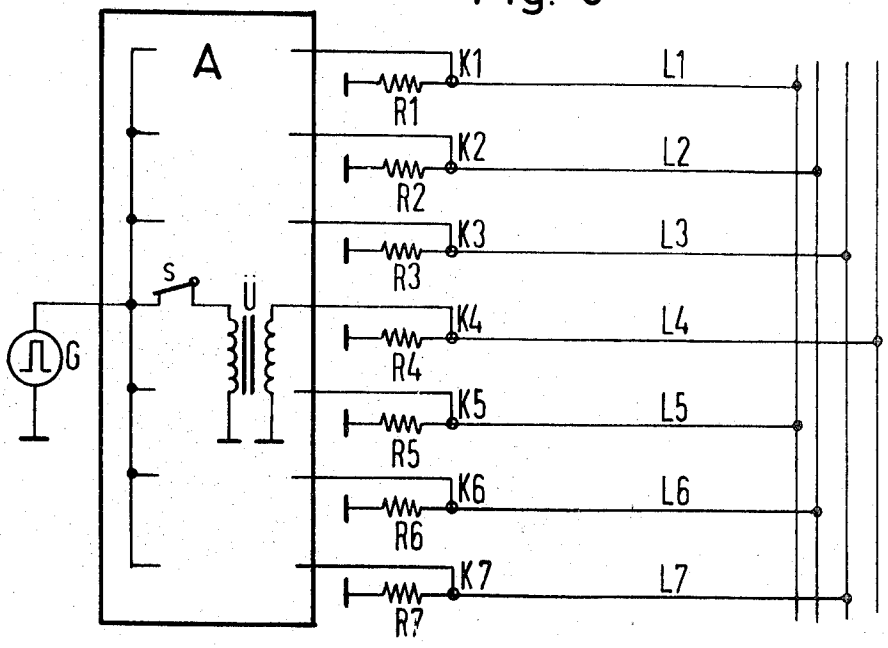


Fig. 3



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MEMORY ARRANGEMENT

BACKGROUND OF THE INVENTION

Maximum operating speeds achievable by memory arrangements or systems depend not only on the switching time of the memory elements but to a very important extent also upon the conduction characteristics of the control lines. A predetermined wave resistance will be associated with each of such lines and by terminating the lines with a resistance corresponding to the wave resistance, instead of a direct connection to a common ground return line or the like, a considerable reduction of the overswing of the control impulses can be achieved.

This procedure, however, is subject to the disadvantage that during the entire duration of the control impulses a relatively high output power must be produced, which is converted, primarily in the terminal resistance of the line being controlled, into heat. It has been previously suggested to move the terminal resistances to the feed or supply side of the control circuits and to obtain the control impulses from a source of constant current. While this results in a slight worsening of the buildup characteristics, the terminal resistance of the line being controlled in each case operates practically only during the impulse surge as an output-dissipating shunt, due to the fact that during the buildup condition only the very much smaller resistance of the control circuit plays any part.

Research has disclosed that in the case of a matrix arrangement, whose linear dimensions usually are so large that the propagation time of the control impulses is approximately equal to or larger than their rise time, considerable return currents occur in the lines parallel to the controlled line, which of course primarily affects the immediately adjacent lines. Only once the "impulse wave" has reached the end of the control line can the return current begin over the common ground return line, which results in additional prolongation of the buildup process.

The invention is directed to the problem of effecting measures to shorten the buildup process and improve the wave conduction behavior of the control lines of a memory system and thereby effect an increase in the operating speed thereof.

BRIEF SUMMARY OF THE INVENTION

The invention thus is directed to a memory system utilizing a plurality of control lines selectively and individually subjected to impulses from a source of constant current, with each of the lines being provided with inductive feed and having a termination at the feed or supply end thereof at least corresponding approximately to its wave resistance, the other ends of the parallel control lines being interconnected at least in groups, with return flow being effected over other of the associated lines whereby the connecting points of a group are not connected directly to a ground or other specific return line.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of the invention will be readily apparent from the following description of certain preferred embodiments thereof, taken in conjunction with the accompanying drawing, although variations and modifications may be effected without departing from the spirit and scope of the novel concepts of the disclosure, and in which:

FIG. 1 schematically presents a circuit diagram of only that portion of a memory arrangement necessary for an understanding of the invention;

FIG. 2 is a similar circuit diagram illustrating a modification of the circuit of FIG. 1; and

FIG. 3 is a similar circuit diagram illustrating another modification of the circuit of FIG. 1.

DETAILED DESCRIPTION

Referring to the drawings, and more particularly to FIG. 1 reference numerals L1–L7 designate respective control lines

of a memory system as for example, row lines extending in parallel relation and associated with a plurality of storage elements, for example magnetic ring cores having an approximately rectangular hysteresis loop with the lines L1–L7 thus forming control lines in one coordinate of the matrix memory.

The right hand ends of the control lines, as viewed in FIG. 1, are illustrated as being interconnected while the ends at the left side of the Figure are connected at the terminals K1–K7 to individually grounded resistances R1–R7, the resistance values of which correspond as close as possible to the wave resistance of the respective associated control circuits formed thereby.

The terminals K1–K7 are also connected over a selector system A, for effecting selection of a particular control circuit and connection thereof to an impulse generator G having constant current characteristics. Such selector installations for the connection of unipolar or bipolar impulses are known, as are the corresponding impulse generators, in view of which it is believed unnecessary to present additional details with respect thereto. The transformer U and switch S is representative of similar connections with the other control lines and it shall be assumed that the closed switch S indicates that the control circuit L4 has been selected for connection with the impulse generator G. If a current impulse with amplitude I and a steep rise flank is supplied to the control circuit L4 the partial currents flow in return direction on the adjacent lines, namely a current *a*.1 in the two immediately adjacent lines, a current *b*.1 next two successive lines in outward direction, etc. In built-up state the partial currents depend only on the resistances of the control circuit and the secondary winding of the transformer U, and thus they are at least approximately equal to one another. It will also be kept in mind that memory systems, for example, matrix memories generally contain a considerably greater number of parallel control lines than that illustrated in the Figure.

On the other hand, at the beginning of the impulses, the current division takes place in relation to the partial wave resistances, dependent substantially on the conductor lengths or distances. The wave resistance with respect to the two nearest neighboring lines thus is the lowest and increases for the lines further away. Each of such wave lines is terminated with a resistance $R_{\perp}R/2$, but as the wave resistance of the waveline consisting of the control circuit involved in its two neighboring lines is only slightly larger than R a considerably faulty termination exists which results in the return current in the nearest lines exhibiting a strong overswing, which in turn is transferred to the read line and possibly may cause disturbances of the read signal.

According to a further improvement of the invention, the wave conduction characteristics of the control circuits parallel to one another can be further improved by disposing the lines in two or more groups which are separated from one another, instead of providing a common connection of all ends of the control circuits remote from the feed. Such grouping can be made, for example as illustrated in FIG. 2, in such a manner that a first group contains all lines with even numbers and a second group contains all lines with odd numbers. Another possibility, for example, resides in the consolidation of every fourth line, etc., as illustrated in FIG. 3. As a result of such types of connection of the control circuits, it is achieved that the lines adjacent the control line carry no current, or only negligibly small return currents. However, a higher wave resistance which is much closer to the resulting terminal resistance R+R/2 results for the immediately subsequent line of the same group of connections. Consequently, the overswing of the return currents and thereby the presence of interference impulses on the read circuit are correspondingly reduced and naturally also the danger of an undesirable influence of the memory cells associated with noncontrolled lines. As a different condition exists with respect to the outermost control circuits of a plurality of connected parallel control circuits, as compared with the remaining control circuits connected therewith resulting from the fact that no additional

connected lines exist adjacent such outermost circuits, it may be advantageous, depending on the type of group formation to provide a compensation therefor by the provision of a line at each side of such group which is terminated with a resistance having a value R, which line is included in the corresponding group but has no memory cells associated therewith, and could comprise one of the otherwise noncontrolled lines adjacent thereto.

What I claim is:

1. A memory system comprising a plurality of control lines, to individual lines of which impulses from a source of constant current may be selectively applied, with each line being provided with an inductive feed and having a termination at the feed end thereof at least corresponding approximately with its wave resistance, the other ends of the parallel control lines being interconnected, at least in groups, with return flow being effected over other of said lines of the group involved whereby such connecting points are not connected to a specific ground or other return line.

2. A memory system according to claim 1, wherein all control lines with even numbers are interconnected and all control lines with odd numbers are separate therefrom and interconnected.

3. A memory system according to claim 1, wherein every fourth line, i.e., the first, fifth, ninth, etc. are interconnected, and the second, sixth, 10th, etc. are interconnected, etc.

4. A memory system according to claim 1, wherein additional parallel lines are provided adjacent the outermost lines of the associated group, and connected therewith to compensate for the fact that such outermost lines are not sequentially disposed with respect to the other lines of such group.

5. A memory system according to claim 1 wherein parallel control lines comprise line and/or column lines of a memory matrix.

6. A memory system according to claim 5, wherein said memory elements comprise magnetic cores having an approximately rectangular hysteresis loop.

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