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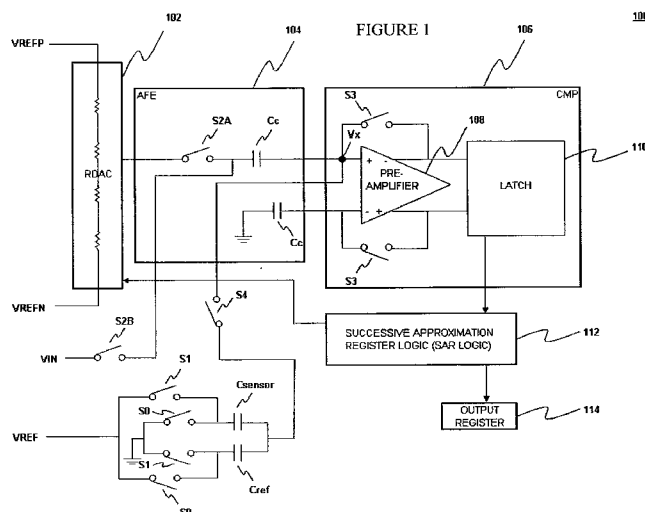
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(54) **Title:** DUAL- FUNCTION SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERTER (SA-ADC)



(57) **Abstract:** A dual-function analog to digital converter is disclosed comprising an analog front end (104), a functionality selection circuitry, a digital to analog converter (102), a comparator (106), a successive approximation register logic (112) and an output register (114). The analog front end (104) couples an input signal to the comparator (106) for either analog to digital conversion or capacitance to digital conversion. The functionality selection circuitry determines the input signal coupled to the comparator (106) as being either an output of the digital to analog converter (102) or an analog input capacitance signal. The digital to analog converter (102) generates a scaled reference voltage required by the comparator (106). The comparator (106) compares the input signal and the scaled reference voltage to generate a comparison result. The successive approximation register logic performs successive approximation based on the comparison result from the comparator (106) to generate either a scaled output required by the digital to analog converter (102) or a digital output proportional to the input signal stored in the output register (114).

DUAL-FUNCTION SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERTER (SA-ADC)

FIELD OF INVENTION

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The present invention relates to a successive approximation analog to digital converter (SA-ADC) that is capable of analog to digital conversion and capacitance to digital conversion, wherein this dual functionality is realized by using an improved analog front end (AFE) and a functionality selection circuitry.

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BACKGROUND ART

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Data acquisition has become a process that is applied in various technical aspects including medical, agricultural, transportation, electronic devices and many others. Data acquisition is a process of measuring physical conditions and converting these measured values into digital values that may be manipulated for the purpose of automatic / semi-automatic monitoring, control and etc. The main components of data acquisition include sensors, signal conditioning circuitry and analog to digital converters (ADC).

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Application Specific Integrated Circuits (ASIC) have been developed to provide customized IC's for the specific use of signal conditioning in combination with built-in ADCs. The signal conditioning circuitry includes multiple sensor readout/interface circuits for interfacing multiple sensors to convert sensor signals into electrical signals recognized by the ADC, more commonly analog signals. The ADCs then convert these analog signals from the sensor readout/interface circuits to corresponding digital values for further processing.

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As the number of required sensors increase, the need for multiple sensor readout/interface circuits also increases. However, multiple sensor readout/interface circuits contribute to higher power consumption within the ASIC, rendering a lower efficiency in the overall performance of data acquisition. Therefore, there is a need to integrate sensor readout/interface circuits into the existing analog to digital converters in a manner that is most efficient to reduce the power consumption of the ASIC.

SUMMARY OF INVENTION

The present invention provides a system and method for a dual function analog to digital converter, specifically, a dual function successive approximation analog to digital converter (SA-ADC). The present invention proposes to enhance power efficiency of signal conditioning Application Specific Integrated Circuits (ASIC) by eliminating capacitive sensor readout/interface circuits, wherein an improved analog front end (AFE) and a functionality selection circuitry is implemented on existing SA-ADC in order to realize dual functionality of the SA-ADC, which is analog to digital conversion and capacitance to digital conversion.

In one aspect of the present invention is a system and method for a dual function analog to digital converter comprising an analog front end, a functionality selection circuitry, a digital to analog converter, a comparator, a successive approximation register logic and an output register. The analog front end couples an input signal to the comparator for either analog to digital conversion or capacitance to digital conversion. The functionality selection circuitry determines the input signal coupled to the comparator as being either an output of the digital to analog converter or an analog input capacitance signal. The digital to analog converter generates a scaled reference voltage required by the comparator. The comparator compares the input signal and the scaled reference voltage to generate a comparison result. The successive approximation register logic performs successive approximation based on the comparison result from the comparator to generate either a scaled output required by the digital to analog converter or a digital output proportional to the input signal stored in the output register.

In a further aspect of the present invention the analog front end of the dual function analog to digital converter further comprises a first coupling capacitor, a second coupling capacitor and a sample and hold switch. A first terminal of the first coupling capacitor is coupled to the output of the digital to analog converter through the sample and hold switch. A second terminal of the first coupling capacitor is coupled to a first input of the comparator. The second coupling capacitor is coupled to a second input of the comparator. The input signal range of the analog front end during analog to digital conversion varies from the input signal range of the analog front end during capacitance to digital conversion. The functionality selection circuitry of the dual function analog to digital converter further comprises a first switch and a second switch. The first switch couples a first terminal of a first coupling capacitor of the analog front end to an analog input signal. The second switch couples the first input of the comparator to the analog input capacitance signal.

In one embodiment of the present invention, the dual function analog to digital converter performs analog to digital conversion wherein digital output proportional to an analog input signal is

generated and stored in the output register. During a sampling phase of analog to digital conversion, the sample and hold switch of the analog front end is turned OFF, the first switch of the functionality selection circuitry is turned ON while the second switch of the functionality selection circuitry is turned OFF and a pair of auto-zeroing switches within the comparator is
5 turned ON. During a bit cycling phase of analog to digital conversion, the sample and hold switch of the analog front end is turned ON, the first and second switch of the functionality selection circuitry is turned OFF and the pair of auto-zeroing switches within the comparator is turned OFF.

In another embodiment of the present invention, the dual function analog to digital converter
10 performs capacitance to digital conversion wherein digital output proportional to an analog input capacitance signal is generated and stored in the output register. During a pre-charge phase and a charge redistribution phase of capacitance to digital conversion, the sample and hold switch of the analog front end is turned ON and the first switch of the functionality selection circuitry is turned
15 OFF while the second switch of the functionality selection circuitry is turned ON. The pair of auto-zeroing switches within the comparator is turned ON during the pre-charge phase of capacitance to digital conversion and turned OFF during the charge redistribution phase of capacitance to digital conversion.

The present invention consists of features and a combination of parts hereinafter fully described
20 and illustrated in the accompanying drawings, it is being understood that various changes in the details may be made without departing from the scope of the invention or sacrificing any of the advantages of the present invention.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

To further clarify various aspects of some embodiments of the present invention, a more particular description of the invention will be rendered by references to specific embodiments thereof, which
5 are illustrated, in the appended drawings. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the accompanying drawings in which:

10 FIGURE 1 illustrates a block diagram of the dual function successive approximation analog to digital converter.

FIGURE 2A illustrates the dual function successive approximation analog to digital converter during a sampling phase of analog to digital conversion.

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FIGURE 2B illustrates the dual function successive approximation analog to digital converter during a bit cycling phase of analog to digital conversion.

FIGURE 3A illustrates the dual function successive approximation analog to digital converter
20 during a pre-charge phase of capacitance to digital conversion.

FIGURE 3B illustrates the dual function successive approximation analog to digital converter during a charge redistribution phase of capacitance to digital conversion.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention relates to a dual-function analog to digital converter that is capable of analog to digital conversion and capacitance to digital conversion. Hereinafter, this specification will describe the present invention according to the preferred embodiments of the present invention. However, it is to be understood that limiting the description to the preferred embodiments of the invention is merely to facilitate discussion of the present invention and it is envisioned that those skilled in the art may devise various modifications and equivalents without departing from the scope of the appended claims.

The present invention more particularly relates to a system and method for a dual function successive approximation analog to digital converter (SA-ADC) that enhances power efficiency of signal conditioning Application Specific Integrated Circuits (ASIC) by eliminating capacitive sensor readout/interface circuits. The term 'dual functionality' refers to the capability of a single SA-ADC performing the conventional analog to digital conversion as well as direct capacitance to digital conversion.

To realize this dual functionality, the present invention proposes an improved analog front end (AFE) and a functionality selection circuitry to be implemented on existing SA-ADCs, whilst retaining the conventional digital to analog converter (DAC), comparator, successive approximation register (SAR) logic and output register. The improved AFE and the functionality selection circuitry are implemented using passive components such as capacitors and analog switches. Therefore, there will not be any addition in power dissipation nor any contribution to the addition of noise. According to the embodiments of the present invention, the improved AFE and the functionality selection circuitry cater for the varied input signal range of the SA-ADC required for the dual functionality, which is the analog to digital conversion and capacitance to digital conversion.

The dual function SA-ADC according to the present invention is capable of digitizing conventional analog signals as well as digitizing a measured change in capacitance from a sensing capacitor. The output of the dual function SA-ADC is a digital output that is proportional to either an analog input signal or a change in an analog input capacitance signal. In both cases, the digital output will be free from errors caused by parasitic capacitance and analog switches charge injection through the implementation of a fully differential operation. Analog switches herein may be Metal-Oxide-Semiconductor (MOS) switches.

Reference is first being made to FIGURE 1. FIGURE 1 illustrates a block diagram of the dual function SA-ADC. The dual-function SA-ADC system (100) comprises an analog front end (104), a functionality selection circuitry, a digital to analog converter (102), a comparator (106), a successive approximation register logic (112) and an output register (114). An external capacitance that is to be measured by a capacitance sensor is modeled as a sense capacitor (C_{SENSOR}), a reference capacitor (C_{REF}) and a plurality of analog switches (S_0, S_1).

The AFE (104) couples an input signal to the comparator (106) for the SA-ADC to perform either of the dual functionality, which is the analog to digital conversion or capacitance to digital conversion. The functionality selection circuitry (or multiplexing circuitry) determines which input signal is to be coupled to the comparator (106), which is either an output of the digital to analog converter (102) or an analog input capacitance signal.

The DAC (102) generates a scaled reference voltage required by the comparator (106), while the comparator (106) compares the input signal and the scaled reference voltage to generate a comparison result. Finally, the SAR logic performs successive approximation based on the comparison result from the comparator (106) to generate either a scaled output required by the DAC (102) or a digital output proportional to the input signal stored in the output register (114).

The improved AFE (104) further comprises a first coupling capacitor (C_c), a second coupling capacitor (C_c) and a sample and hold switch (S_{2A}). A first terminal of the first coupling capacitor (C_c) is coupled to the output of the DAC (102) through the sample and hold switch (S_{2A}), while a second terminal of the first coupling capacitor (C_c) is coupled to a first input of the comparator (106). The second coupling capacitor (C_c) is coupled to a second input of the comparator (106).

To selection between the dual functionality of the SA-ADC is performed by the functionality selection circuitry. This circuitry further comprises a first switch (S_{2B}) and a second switch (S_4). These switches are programmably controlled by any form of control module or software programmed. These switches are configured according to a predefined switching sequence based on the desired functionality of the SA-ADC. The first switch (S_{2B}) couples the first terminal of a first coupling capacitor (C_c) of the AFE (104) to an analog input signal. The second switch (S_4) couples the first input of the comparator (106) to the analog input capacitance signal.

The DAC (102) of the dual function SA-ADC may be implemented as either a resistive digital to analog converter (RDAC) or capacitive digital to analog converter (CDAC). In the case of the later, the sample and hold block is incorporated within the CDAC instead of the AFE (104), as is

the case for the RDAC. The comparator (106) of the dual function SA-ADC further comprises a preamplifier (108), a latch (110) and a pair of auto-zeroing switches (S3).

Analog to digital conversion

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In one embodiment of the present invention, the dual function SA-ADC performs analog to digital conversion wherein a digital output proportional to an analog input signal is generated and stored in the output register (114). The analog to digital conversion mode comprises a sampling phase and a bit cycling phase. During the analog to digital conversion mode, the plurality of analog switches (S0, S1) that model the external capacitance that is to be measured are turned OFF. Switching sequence of the remaining analog switches provide the SA-ADC with a dynamic input signal range of

$$VREF' = VREFP - VREFN.$$

15 VREFP and VREFN are voltage references that may be supplied directly from a power supply, or an external voltage reference, or a digital logic output.

Reference is being made to FIGURE 2A. FIGURE 2A illustrates the dual function SA-ADC during the sampling phase of analog to digital conversion mode. During the sampling phase of the analog to digital conversion mode, the analog input signal is sampled onto the first coupling capacitor (C_c) and second coupling capacitor (C_c) of the AFE (104) and the preamplifier (108) of the comparator (106) is set to auto-zero. To enable sampling of the analog input signal, the sample and hold switch (S2A) of the AFE (104) is turned OFF and the first switch (S2B) of the functionality selection circuitry is turned ON. Simultaneously, the second switch (S4) of the functionality selection circuitry is turned OFF. To enable the preamplifier (108) auto-zero, the pair of auto-zeroing switches (S3) is turned ON.

Reference is being made to FIGURE 2B. FIGURE 2B illustrates the dual function SA-ADC during the bit cycling phase of analog to digital conversion mode. During the bit cycling phase of the analog to digital conversion mode, successive approximation of the sampled analog input signal is performed by the DAC (102) and the SAR logic (112) in order to generate the digital output proportional to the analog input signal that is later stored in the output register (114). To enable successive approximation of the sampled analog input signal, the sample and hold switch (S2A) of the AFE (104) is turned ON and the first and second switch (S2B, S4) of the functionality selection circuitry is turned OFF. The pair of auto-zeroing switches (S3) is turned OFF.

Capacitance to digital conversion

In another embodiment of the present invention, the dual function SA-ADC performs capacitance to digital conversion wherein digital output proportional to an analog input capacitance signal is generated and stored in the output register (114). The analog input capacitance signal is an external capacitance measured by the capacitance sensor. The capacitance to digital conversion mode comprises a pre-charge phase and a charge redistribution phase. During the capacitance to digital conversion mode, the sample and hold switch (S2A) of the AFE (104) and the second switch (S4) of the functionality selection circuitry are both turned ON while the first switch (S2B) of the functionality selection circuitry is turned OFF. Switching sequence of the remaining analog switches provide the SA-ADC with a dynamic input signal range of V_{REF} .

V_{REF} , the dynamic input signal range of the SA-ADC during the capacitance to digital conversion mode varies from V_{REF}' , the dynamic input signal range of the SA-ADC during the analog to digital conversion mode.

Reference is being made to FIGURE 3A. FIGURE 3A illustrates the dual function SA-ADC during the pre-charge phase of capacitance to digital conversion mode. During the pre-charge phase of the capacitance to digital conversion mode, V_X is set to 0, the sense capacitor (C_{SENSOR}) is not charged and the reference capacitor (C_{REF}) is charged to $V_{REF} - V_X$. To enable this, analog switch (S0) is turned ON while analog switch (S1) is turned OFF, and the pair of auto-zeroing switches (S3) is turned ON.

Reference is being made to FIGURE 3B. FIGURE 3B illustrates the dual function SA-ADC during the charge redistribution phase of capacitance to digital conversion mode. During the charge redistribution phase of capacitance to digital conversion mode, V_X changes as follows:

$$\frac{V_{REF} * (C_{REF} - C_{SENSOR})}{(C_{REF} + C_{SENSOR} + C_C)}$$

This corresponds to feeding the comparator (106) with an analog input signal of:

$$\frac{V_{REF} * (C_{REF} - C_{SENSOR})}{(C_{REF} + C_{SENSOR} + C_C)}$$

To enable this, analog switch (S0) is turned OFF while analog switch (S1) is turned ON, and the pair of auto-zeroing switches (S3) is turned OFF. This renders the DAC (102) having output of:

$$V_{DACOUT} = \frac{V_{REF} * (C_{REF} - C_{SENSOR})}{C_C}$$

Successive approximation of the analog input signal is performed by the DAC (102) and the SAR logic (112) in order to generate the digital output proportional to the analog input capacitance

signal, which is the change $[C_{REF} - C_{SENSOR}]$ in the external capacitance measured by the capacitance sensor, that is later stored in the output register (114).

VREF is a voltage reference that may be supplied directly from a power supply, or an external
5 voltage reference, or a digital logic output.

Successive approximation

10 In both the analog to digital conversion mode and capacitance to digital conversion mode, successive approximation begins with the SAR Logic (112) setting the MSB of the DAC (102) to 1 and the remaining bits are set to 0. This generates the scaled reference voltage of $\frac{1}{2}$ the full-scale range. The comparator (106) then determines if the scaled reference voltage provided by the DAC (102) is above or below the input signal to the comparator (106). If the scaled reference voltage is
15 above the input signal, the scaled reference voltage of $\frac{1}{4}$ the full-scale range is utilized for the successive comparison. This process continues until all the bits within the DAC (102) are tested and the nearest approximation (result) to the input signal is obtained. The result generated is stored in the output register (114).

CLAIMS

1. A dual-function analog to digital converter system (100) comprising:

an analog front end (104);
a functionality selection circuitry;
a digital to analog converter (102);
a comparator (106);
a successive approximation register logic (112); and
an output register (114);

wherein

the analog front end (104) couples an input signal to the comparator (106) for either analog to digital conversion or capacitance to digital conversion; the functionality selection circuitry determines the input signal coupled to the comparator (106) as being either an output of the digital to analog converter (102) or an analog input capacitance signal; the digital to analog converter (102) generates a scaled reference voltage required by the comparator (106); the comparator (106) compares the input signal and the scaled reference voltage to generate a comparison result; and the successive approximation register logic performs successive approximation based on the comparison result from the comparator (106) to generate either a scaled output required by the digital to analog converter (102) or a digital output proportional to the input signal stored in the output register (114).

2. A dual-function analog to digital converter (100) according to claim 1, wherein the analog front end (104) further comprises

a first coupling capacitor (C_c);
a second coupling capacitor (C_c); and
a sample and hold switch (S2A),

wherein

a first terminal of the first coupling capacitor (C_c) is coupled to the output of the digital to analog converter (102) through the sample and hold switch (S2A), the sample and hold switch (S2A) is turned OFF during a sampling phase of analog to digital conversion and turned ON during a bit cycling phase of analog to digital conversion and during a pre-charge

phase and a charge redistribution phase of capacitance to digital conversion;

a second terminal of the first coupling capacitor (C_c) is coupled to a first input of the comparator (106); and

5 the second coupling capacitor (C_c) is coupled to a second input of the comparator (106).

10 3. A dual-function analog to digital converter (100) according to claim 1, wherein the input signal range of the dual-function analog to digital converter (100) during analog to digital conversion varies from the input signal range of the dual-function analog to digital converter (100) during capacitance to digital conversion.

15 4. A dual-function analog to digital converter (100) according to claim 1, wherein the functionality selection circuitry further comprises
a first switch (S2B); and
a second switch (S4),
wherein

20 the first switch (S2B) couples a first terminal of a first coupling capacitor (C_c) of the analog front end (104) to an analog input signal, the first switch (S2B) is turned ON during a sampling phase of analog to digital conversion and turned OFF during a bit cycling phase of analog to digital conversion and during a pre-charge phase and a charge redistribution phase of capacitance to digital conversion; and
the second switch (S4) couples a first input of the comparator (106) to the
25 analog input capacitance signal, the second switch (S4) is turned ON during a pre-charge phase and a charge redistribution phase of capacitance to digital conversion and turned OFF during a sampling phase of and a bit cycling phase of analog to digital conversion.

30 5. A dual-function analog to digital converter (100) according to claim 1, wherein the digital to analog converter (102) comprises a resistive digital to analog converter or a capacitive digital to analog converter.

35 6. A dual-function analog to digital converter (100) according to claim 1, wherein the comparator (106) further comprises a preamplifier (108), a latch (110) and a pair of auto-zeroing switches (S3), wherein the pair of auto-zeroing switches (S3) is turned ON during a sampling phase of analog to digital conversion and a pre-charge phase of capacitance to

digital conversion and turned OFF during a bit cycling phase of analog to digital conversion and a charge redistribution phase of capacitance to digital conversion.

7. A method for dual-function analog to digital converter comprising the steps of:

5 coupling, by an analog front end (104), an input signal to a comparator (106) for either analog to digital conversion or capacitance to digital conversion; determining, by a functionality selection circuitry, the input signal coupled to the comparator (106) as being either an output of a digital to analog converter (102) or an analog input capacitance signal;
10 generating, by a digital to analog converter (102), a scaled reference voltage required by the comparator (106); comparing, by the comparator (106), the input signal and the scaled reference voltage to generate a comparison result; and performing, by a successive approximation register logic, successive
15 approximation based on the comparison result from the comparator (106) to generate either a scaled output required by the digital to analog converter (102) or a digital output proportional to the input signal stored in an output register (114).

8. A method for dual-function analog to digital converter according to claim 7, wherein the
20 method further comprises the steps of:

 coupling a first terminal of a first coupling capacitor (C_c) to the output of the digital to analog converter (102) through a sample and hold switch (S2A), the sample and hold switch (S2A) is turned OFF during a sampling phase of analog to digital conversion and turned ON during a bit cycling phase of analog to digital
25 conversion and during a pre-charge phase and a charge redistribution phase of capacitance to digital conversion; coupling a second terminal of the first coupling capacitor (C_c) to a first input of the comparator (106); and coupling a second coupling capacitor (C_c) to a second input of the comparator
30 (106).

9. A method for dual-function analog to digital converter according to claim 7, wherein the input signal range of the dual-function analog to digital converter (100) during analog to digital conversion varies from the input signal range of the dual-function analog to digital
35 converter (100) during capacitance to digital conversion.

10. A method for dual-function analog to digital converter according to claim 7, wherein the method further comprises the steps of:
- coupling, using a first switch (S2B), a first terminal of a first coupling capacitor (C_c) of the analog front end (104) to an analog input signal, the first switch (S2B) is turned ON during a sampling phase of analog to digital conversion and turned OFF during a bit cycling phase of analog to digital conversion and during a pre-charge phase and a charge redistribution phase of capacitance to digital conversion; and
- coupling, using a second switch (S4), a first input of the comparator (106) to the analog input capacitance signal, the second switch (S4) is turned ON during a pre-charge phase and a charge redistribution phase of capacitance to digital conversion and turned OFF during a sampling phase of and a bit cycling phase of analog to digital conversion.
11. A method for dual-function analog to digital converter according to claim 7, wherein the digital to analog converter (102) is comprises a resistive digital to analog converter or a capacitive digital to analog converter.
12. A method for dual-function analog to digital converter according to claim 7, wherein the comparator (106) further comprises a preamplifier (108), a latch (110) and a pair of auto-zeroing switches (S3), wherein the pair of auto-zeroing switches (S3) is turned ON during a sampling phase of analog to digital conversion and a pre-charge phase of capacitance to digital conversion and turned OFF during a bit cycling phase of analog to digital conversion and a charge redistribution phase of capacitance to digital conversion.

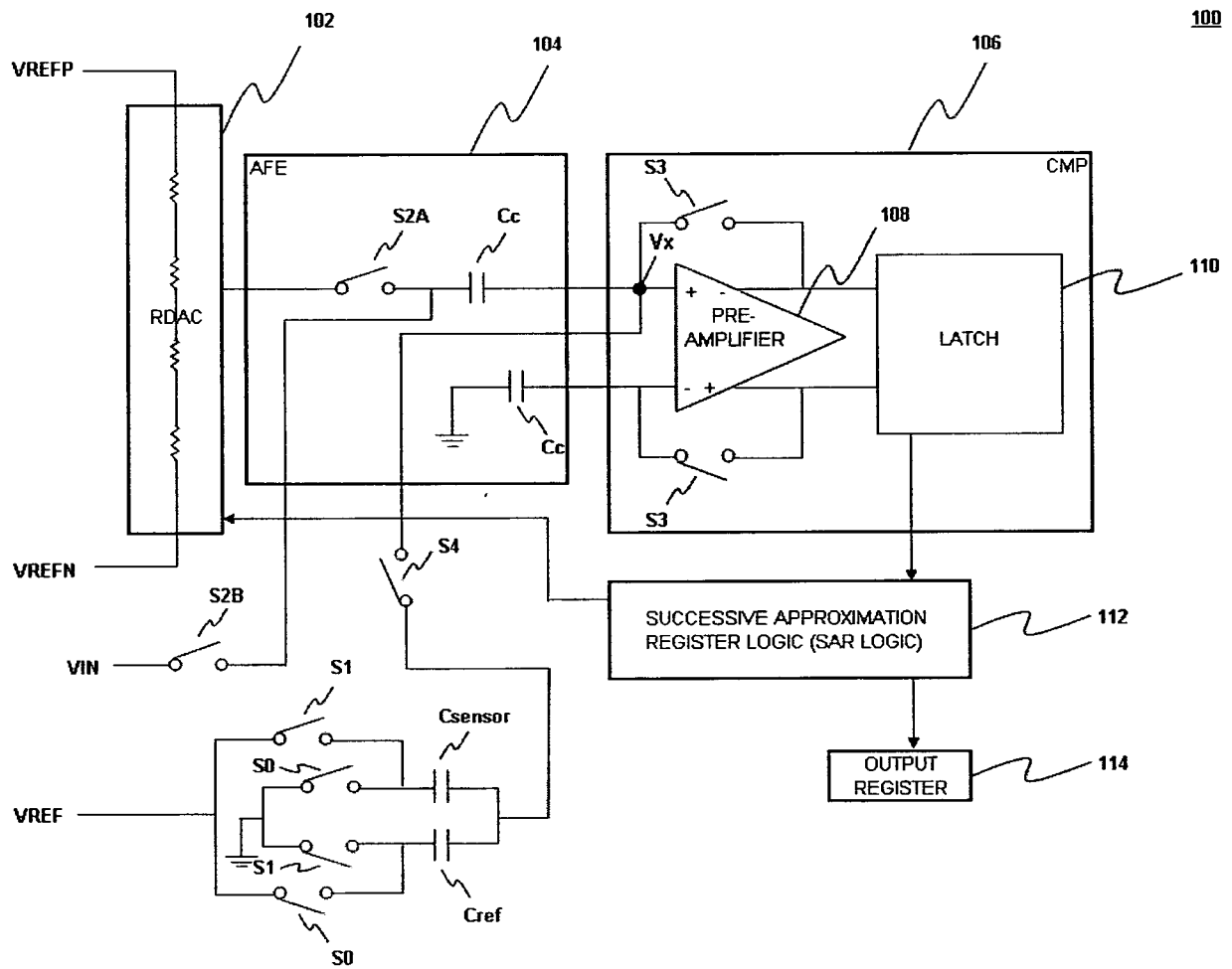


FIGURE 1

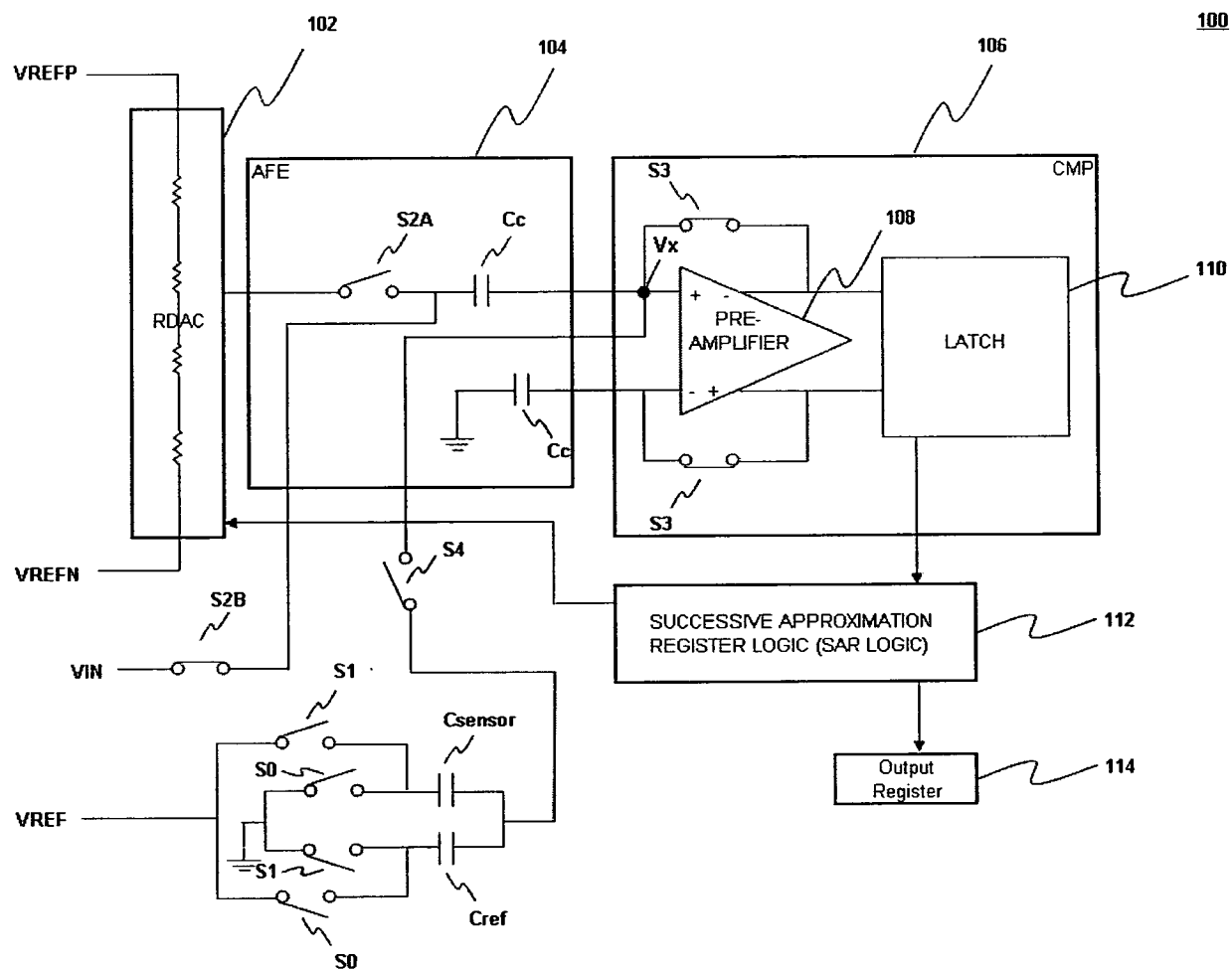


FIGURE 2A

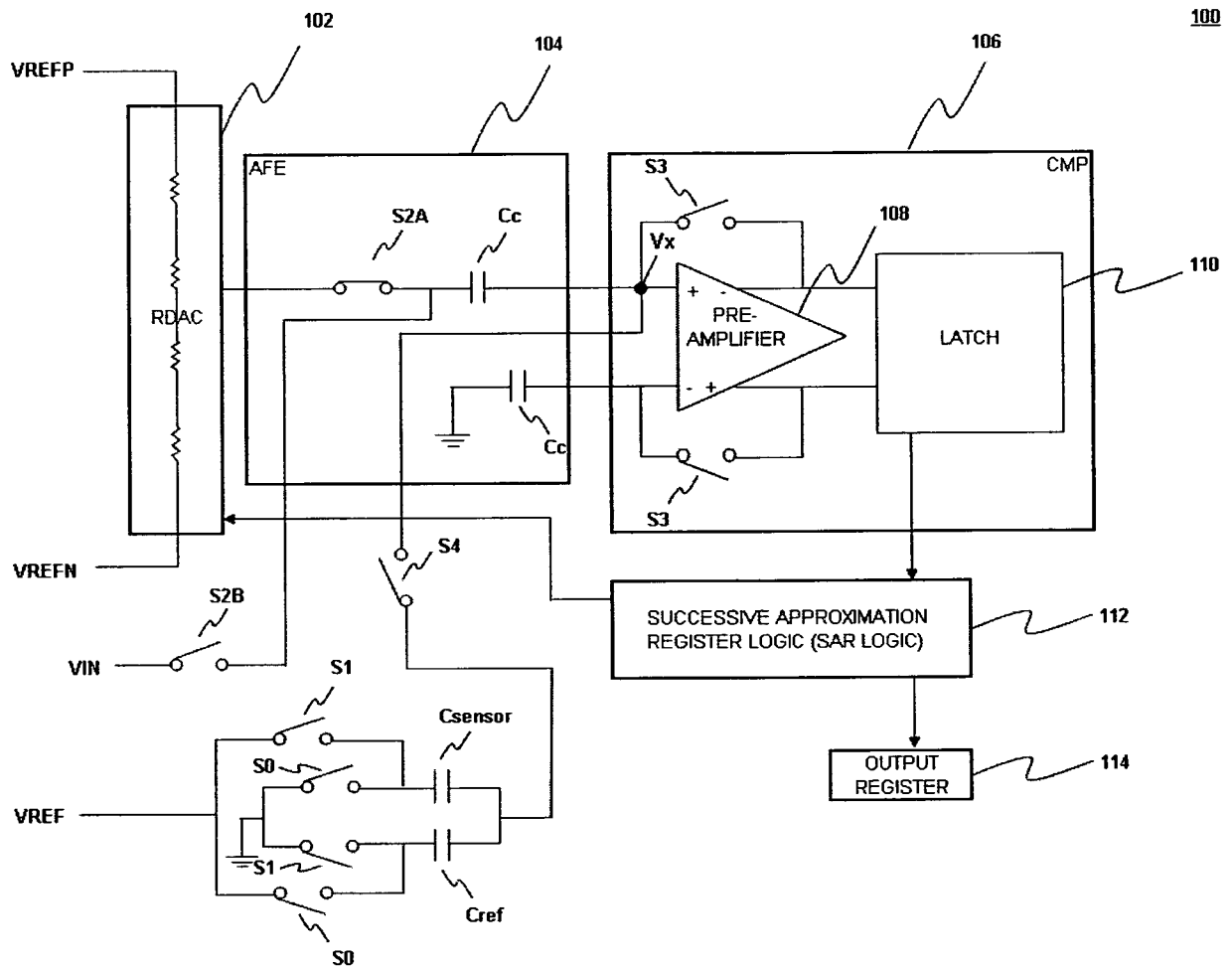


FIGURE 2B

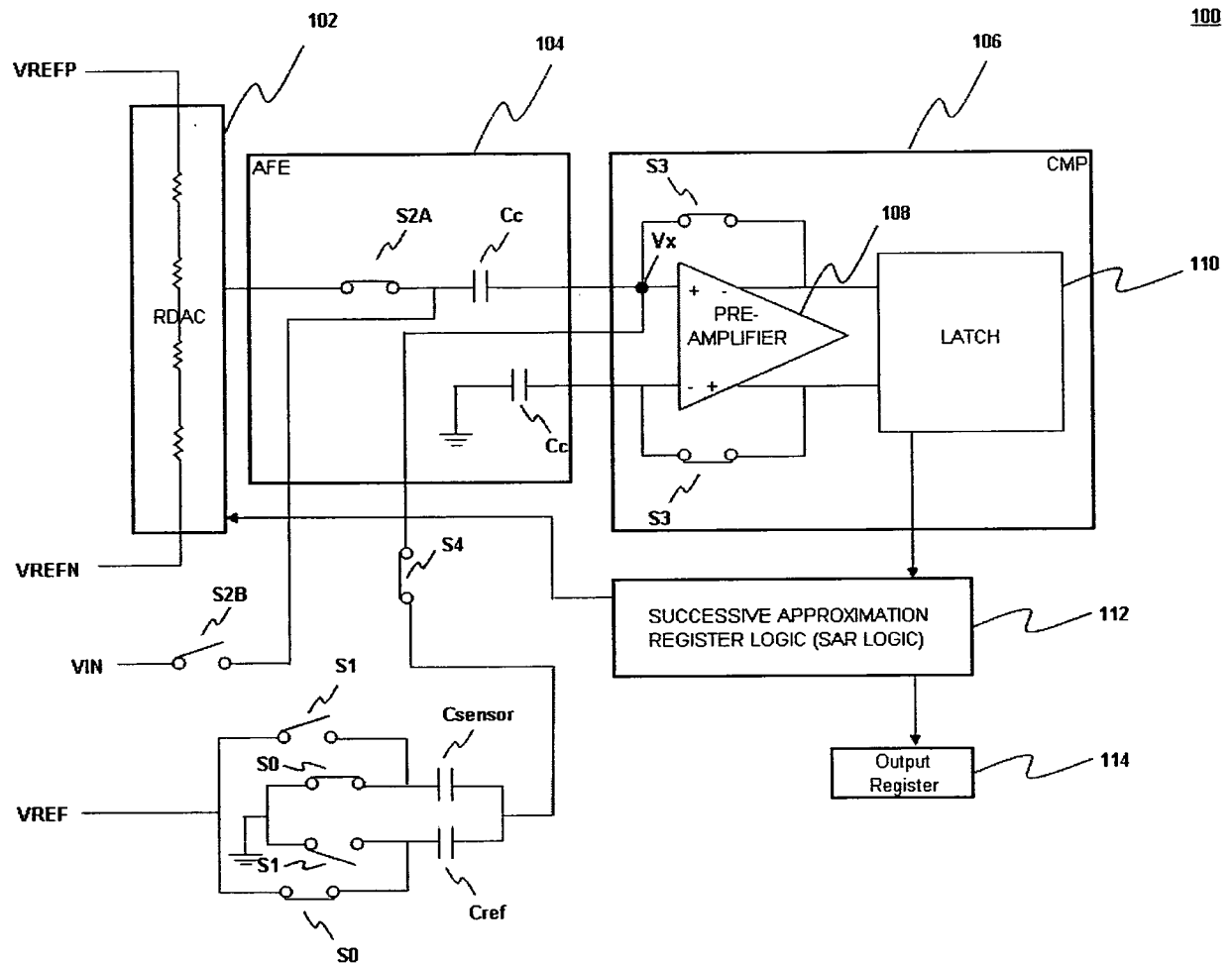


FIGURE 3A

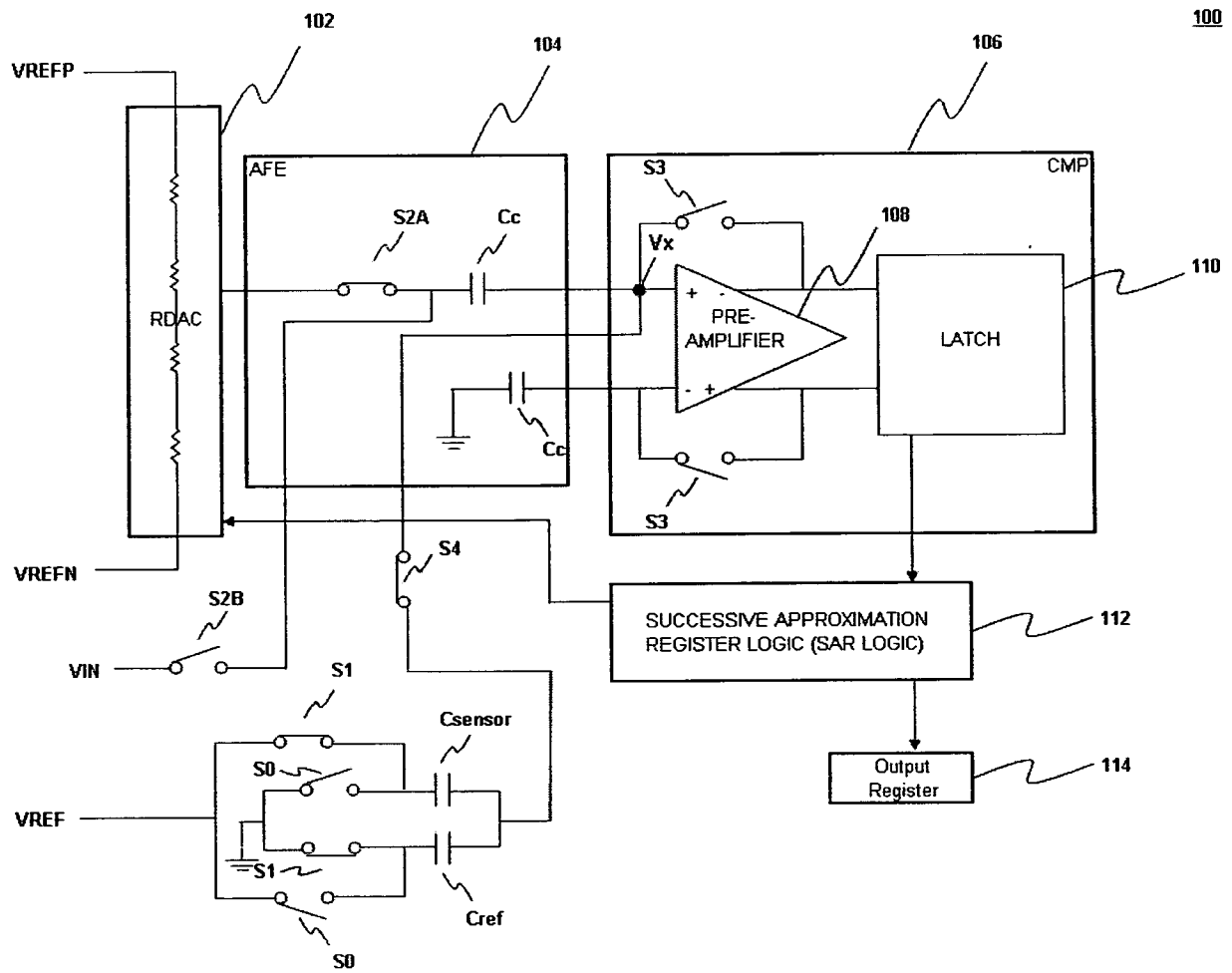


FIGURE 3B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/MY2011/000099

A. CLASSIFICATION OF SUBJECT MATTER												
Int. Cl.												
<i>H03M 1/12</i> (2006.01) <i>H03M 1/42</i> (2006.01)												
According to International Patent Classification (IPC) or to both national classification and IPC												
B. FIELDS SEARCHED												
Minimum documentation searched (classification system followed by classification symbols)												
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched												
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)												
DWPI & EPODOC - Keywords (DAC, ADC, register, comparator, SAR, capacitance) and like terms;												
C. DOCUMENTS CONSIDERED TO BE RELEVANT												
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.										
A	US 7782243 B1 (LU) 24 August 2010 Abstract											
A	US 2005/0146456 A1 (KONDO) 7 July 2005 Abstract, paragraphs [0012]-[0015]											
A	US 5488370 A (HARADA) 30 January 1996 Abstract											
A	US 4647903 A (RYU) 3 March 1987 Abstract, Fig 1											
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Date of the actual completion of the international search 11 August 2011		Date of mailing of the international search report 12.08.2011										
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/MY2011/000099

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member	
US	7782243	US	2010231429
US	2005146456	JP	2005295315
US	5488370	JP	7066728
US	4647903	JP	59161916
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.			
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