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(54) **Title**: POWER CONTROL BY PHASE CUTTING

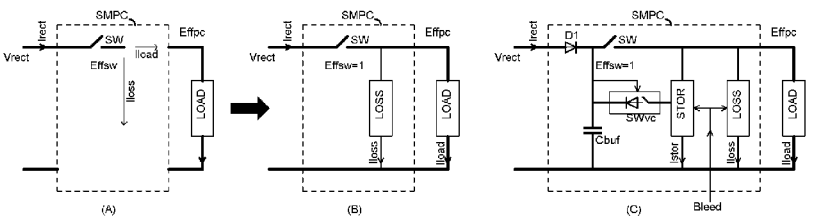


FIG. 5A

(57) **Abstract**: A power controlling apparatus for controlling electrical power delivered from a phase-cut AC power source to a load, said apparatus comprising: a rectifying means converting the AC power to DC power; a switched-mode power converter with the input coupled to the DC power and the output coupled to the load; and current controlling means to regulate the input current from the power source to the converter through control of the output and efficiency of the converter, wherein the efficiency of the converter is controlled through controlling the dissipative loss of at least one power switch of the converter; wherein the converter is controlled by a bleed controller comprising an analog-OR gate.

Power Control by Phase Cutting

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates generally to apparatus and methods for AC power control, and more particularly to AC power control by phase cutting.

Description of the Related Art

When electrical power, in terms of electrical voltage or current, is applied to a load, there are basically a number of issues critical for effective transfer of energy from the electrical power supply to the load.

First, the voltage or current level from the power supply should be appropriate for the load, as a load is usually designed to work properly only within a certain range of voltage or current level. For example, an incandescent lamp may work properly from a line voltage of a specified magnitude, say 230V or 110V, while an LED lamp requires a driving current of say 300 mA. Deviation from the specified range of voltage or current may give rise to compromised operation efficiency or even destructive damage to the power supply or the load.

Second, the load may have been specified to accept DC or AC power, at certain frequency, and with certain waveforms. For example, for the above quoted examples, the incandescent lamp may have been designed for 50/60 Hz sinusoidal voltage supplies, while the LED lamp may have been designed for DC current supplies. Deviation from such specifications may also give rise to compromised operation efficiency or even destructive damage to the power supply or the load.

Third, the power supply may need to be loaded properly in order to function normally as intended. An example is the TRIAC (TRIode for Alternating Current) dimmed power supply for electrical lighting, whereby there is a requirement for the TRIAC to be loaded sufficiently to maintain a load current of no less than a holding current threshold in order that the TRIAC remains conducting after being triggered by a pulse at the gate electrode. The minimum holding current is a

electrical characteristic of the particular TRIAC used.

Fourth, there is a need to control the load power by a command signal, either through a separate signal line, or through the power line itself. A TRIAC dimmer provides a good example of the latter, as both power and signal lines are combined together to a single line to the lighting device as the load. By suitable signal processing at the load side, the phase-cut waveform could actually be decoded for manipulation of the power delivered to the load in a desirable way more than just simple power level control. Obviously saving of signal lines implies economic benefits.

Over the decades large number of various electrical and electronic systems and methods are invented and designed to address the above issues. These include power transformers to raise or lower AC voltage levels, DC-to-DC converters or AC-to-DC converters to provide DC voltage supplies, and DC-to-AC or AC-to-AC converters to provide AC voltage supplies. All these have been deployed to address the above first and second issues.

As for the third and fourth issues, TRIAC dimmer is a good subject for study in view of the new technological challenges as this old technology is applied to modern electronic devices such as LED lights driven by the Switched-mode Power Supply SMPS, as will be explained below.

TRIAC dimmers are most popular among phase-cut power controllers, or simply called phase cutters, which control power by phase cutting, i.e. removing a portion of the sinusoidal waveform of the AC voltage, thus reducing the RMS (Root Mean Square) voltage, hence the power, delivered to the load. Phase cutting may actually be considered as a PWM (Pulse Width Modulation) technique applied specifically to AC power control and is normally required to be synchronized to the AC voltage supply frequency for proper operation.

Having been around for half a century, TRIAC dimmers have originally been designed for resistive loads, the incandescent lamps, and have been very popular for their simple circuitry and low cost. Further, by passing control signal and delivering power to the load through the same electrical path, TRIAC dimmers offer the easiest and cheapest way of installation in the two-wire mode, as illustrated in the circuit diagram of FIG. 1. Naturally, majority of existing residential wiring infrastructure has been installed accordingly for two-wire-mode. Basically the TRIAC dimmer consists of a CR (capacitor-resistor) timing circuit consisting of capacitor C1 and resistors R1+R2, and a power switching circuit consisting the diac D1 and TRIAC TR1. Note that when the TRIAC is

open circuit the load LOAD, resistive in the case of incandescent lamps, is in the critical path of the CR timing circuit. For this reason, there is the possibility that the load may affect the timing circuit and hence the performance of the TRIAC dimmer if the load does not provide sufficiently low impedance to the timing circuit.

Compared to incandescent lamps, modern devices as powered by switched-mode power converters present entirely different kinds of loads to the phase-cut power controllers. A typical example is LED light driven by a switching AC-to-DC converter, which presented a reactive and non-linear load to the phase-cut dimmer. This is a problem for the traditional dimmers as LED light, being promoted for high energy efficiency, might not be drawing sufficient current directly or through the power converter to hold the TRIAC dimmer on conduction when it should. Further, being reactive and non-linear, the electronic load may not provide a good circuit path for the timing circuit of the TRIAC dimmer to work properly in the two-wire connection mode, leading to erratic behaviour of the lamp such as flickering, flashing, pop-on, drop-out, etc. While three-wire connection mode offers a better solution than the two-wire mode in this regard, this is not feasible in many of the existing residential sites. How to design an LED driver that work properly with the two-wire dimming systems has therefore become of practical and commercial significance nowadays.

TRIAC dimmers are classified as “leading edge”, or “forward” phase-cut dimmers, in differentiation from “trailing edge”, or “backward” or “reverse” phase-cut dimmers. These two classes are named according to whether the cut portion is the leading or the trailing part of a single half-cycle of the AC voltage, as shown in FIG. 2 for example. From top to bottom, the first waveform is the line voltage before phase cutting, the second is being leading edge cut by around 90 degrees, while the bottom one is trailing edge cut by around 45 degrees.

Apart from the above two classes of phase-cut dimmers, there is yet another class which in each half-cycle cuts the AC power many times, or even at high frequencies. These dimmers are called sinewave dimmers which, due to the complexity in circuit structure and the high cost, are only deployed for high end applications in, for example, TV stations and theatres. These dimmers will however also be compatible to the power controllers disclosed by the present invention.

Phase cutting is indeed a simple and straight forward way for AC power control. However the “cutting” of phase gives rise to a phenomenon that may lead to problems in the design, namely the

very abrupt change of voltage and hence the similarly abrupt change of current that lead to undesirable EMI (Electromagnetic Interference). To address the problem, an LC filter consisting of inductor L1 and capacitor C2 is deployed as shown in FIG. 1 for EMI suppression.

For a TRIAC dimmer simple LC filter works well with resistive loads such as incandescent lamps. However it is a very different story if the dimmer is connected to an inductive or capacitive load, such as a SMPS (Switched-Mode Power Supply) driving a lighting device. From the output of a phase-cut power controller, the abrupt change of voltage, i.e. high dV/dt in symbolic form, impressed on a capacitive load can create very high current pulses, while abrupt change of current, or high dI/dt in symbolic form, impressed on an inductor can create very high voltage pulses. Such high levels of EMI if not suppressed could render the power controller and /or the load device inoperative or even destroyed.

For TRIAC dimmers, there is yet another issue for reactive loads. After each zero-crossing of the sinusoidal line voltage, the TRIAC is triggered ON at a phase angle determined by the CR timing circuit. Once triggered, the TRIAC continues to conduct until the current drops below the holding current threshold. For resistive loads, the current is normally maintained by design above the holding current until the sinusoidal voltage goes near to zero. The same process is repeated for each of the following half line cycles. By a reactive load however the load current, hence the TRIAC current, may go up and down abruptly, or rings, at the time when the TRIAC is turned from off to on. Once the current swings below the holding current threshold, even just momentarily, the TRIAC will be cut open immediately, causing flickering of the AC/DC converter-driven LED lights as the dimmer loads.

Not for the holding current alone, a minimum loading current is required generally for powering the phase-cut power controller in two-wire mode, by either leading or trailing edge triggering. Therefore for a light load, a resistive dummy load may need to be connected in parallel to draw sufficient amount of current for proper operation of the phase-cut power controller, as shown in FIG. 3A.

Therefore the dummy load has three functions: helping to provide the necessary holding/loading current for the phase cutter during the conduction time, helping to provide a electrical path for proper operation of the CR timing circuit during the non-conduction time, and helping to provide sufficient power for proper operation of the phase cutter in the two-wire mode.

Note that the dummy load may be drawing current from the phase cutter, either directly from the output of the cutter, or through the filter & damper, or through the rectifier, as shown in FIG. 3A. Neglecting the usually small current bypassed by the Filter and Damper Unit, the total current through the Phase Cutter, identified by Ipcut in the block diagram, is equal to sum of Ismpc, the input current to the Switched-mode Power Converter, and Idummy, the current drawn by the Dummy Load. Note also that in general the positions of the rectifier and the filter & damper in cascade might be interchanged as far as dummy load is concerned. As an example, patent US6452343 is an early patent that deploys dummy load/bleeder for the TRIAC dimmers.

However it is obvious that by such arrangement, energy is dissipated on the dummy load or bleeder wastefully. Attempts have therefore been made to reduce the power wastage by controlling the current through the dummy load as and only when required, dynamically or adaptively. Many different circuit schemes have been devised to control the dummy load or bleed current, by monitoring the dimmer voltage output, or the dimmer current output, or the timing of dimmer switching.

The block diagram of FIG. 3B is to illustrate a phase-cut power controlling system with a variable dummy load. As shown, the Dummy Load is controlled by a Dummy Load Controller DLC to draw current from the rectifier output. Irect, representative of the dimmer output current, is detected and compared to a predetermined current reference represented by Iref by a comparator of finite gain (not shown) inside the Dummy Load Controller DLC. Iref can be a constant or a time-varying voltage, representing say a current value no less than the holding current threshold of the phase cutter (such as TRIAC). Any shortfall of the dimmer current represented by Irect from that represented by Iref is amplified by the comparator which will drive the Dummy Load to draw more current from the rectifier output, in parallel with the switch-mode power converter, so as to maintain the current from the phase cutter no less than the predetermined value represented by Iref. At the moments the switch-mode power converter is drawing more current, the Dummy Load will be drawing less, hence less power is wasted.

Note that unlike the case of fixed dummy load, current is to be drawn from the rectifier output but not the rectifier input for the convenience of control in unipolar mode. Likewise, the voltage and current sensing points are also at post-rectification points for the same reason. Shown in FIG.3B there are other alternative sensing points as represented by dotted lines, for such as dimmer output voltage, switched-mode power converter voltage or current, as are deployed by various control

schemes of the prior arts exemplified by the following patents.

In patents US6870327, US8169154, US8264165 and US8716957 the dimmer voltage output is continuously monitored, and dummy load is switched on for a short period of time when the dimmer switch is turned on, counteracting any undershoot of the ringing dimmer current that might turn off the dimmer TRIAC as a consequence of dimmer switching.

In patent US8664885 the dimmer output voltage is also continuously monitored, the dummy load/bleeder current is allowed to flow only when the dimmer voltage output is below a preset voltage level, on the assumption that the dimmer TRIAC will lose hold only when the line input voltage, hence the dimmer voltage output, is below the set voltage level. On the other hand, for US7132802, when the dimmer voltage output is close to zero, a bleeder is turned on across the dimmer output to facilitate the proper operation of the dimmer timer.

In patents US7656103, US8283875, US8441210, US8575901, US8610375 and US8704462 the dimmer output current is continuously monitored, and compared to a voltage reference representative of the holding current threshold of the dimmer TRIAC. Only when the dimmer output current falls short of the threshold, the dummy load or bleeder current is turned on and controlled to make up for the shortfall. Alternatively, the current through or voltage across the (LED) load is monitored for the control of the bleeder current, as in the patents US8581498 and US8766560.

In the search for even better solutions, it has been proposed to deliberately increase the output of the switched-mode power converter, so that the converter is drawing more current from the phase cutter as if it is taking an additional role as a dummy load or bleeder. The benefit achieved is that no extra components for the dummy load or bleeder are required, thus avoiding the associated penalties in cost and efficiency. This seems to have been attempted in patent US8610375, by which the duty ratio of the power converter switch is increased when the TRIAC current is detected to be lower than the holding current threshold. However it is not articulated as how the operation of the converter would be jeopardized as the converter is forcefully driven for higher input current by the raised duty ratio but without addressing the effects on the output level of the converter, i.e. the accompanying effect of increased power delivered to the load, and if and how energy efficiency is compromised.

It is therefore highly desirable as an objective by the present invention to develop a method to load or bleed the phase-cut power controller effectively without the need for any separate dummy

load or bleeder, and at the same time there should absolutely be no side-effect on the power output to the load.

There is also a need to control the power to the load smoothly, as in the case for controlling the luminous output from an LED lamp by a dimmer. It is a general experience of what are available in the market nowadays, that the traditional incandescent lamps outperform the LED lamps readily in terms of smoothness in dimming control. It is of great interest to the market to have the LED lamps performing as good as the incandescent lamps in this regard.

FIG. 4A to 4C shows the operation principle of various schemes of phase-cut power control in the prior art, for loads powered by switched-mode power converters, just like the case for many LED lights nowadays.

Quoting LED light as a typical example of load under phase-cut power control, there are two different approaches in the prior art to power the load through a switched-mode power converter. The first approach is for the switched-mode power converter to generate a current of the magnitude proportional to that (such as the RMS or the average or other measures) of the phase-cut voltage. By altering the magnitude of the phase-cut voltage output, the current through the LED light is altered in proportion, and the light output thereby is controlled accordingly.

In FIG. 4A, the rectifier output voltage represented by Vrect is detected and transformed to a DC signal Vrectdc by the DC Sig Gen module such that Vrectdc is a DC voltage representative the magnitude of Vrect, either in RMS or average or any other measures. Vrectdc can also be made representative of the duty cycle (percentage uncut portion) of Vrect. Vrectdc is presented as an instantaneous reference to the positive input of the comparator Comp of finite gain, as Ispcref. Output current from the Switched-mode Power Converter to the Load is detected as and represented by Ispc. Ispc is compared to Ispcref to generate an error signal Ispcerr which is a feedback signal to drive the switched-mode power converter in a direction so as to reduce this error signal. Consequently the load current is driven to follow the magnitude of voltage output from the phase cutter.

The second approach is for the switched-mode power converter to generate a constant current (or less desirable, voltage) which is delivered to the LED light in chopped mode at a duty cycle proportional to the magnitude (such as the RMS or the average) of the phase-cut voltage. For the

chopping frequency it would be just convenient to use the 100/120 Hz signal available from the rectified line voltage. Further the control circuit can be much simplified if duty cycle of the output voltage of the phase-cut dimmer can be accepted as representative of the desired magnitude of power to the LED light.

FIG. 4B is a block diagram showing how this approach works. The voltage output from the rectifier represented by Vrect is detected and compared to a low voltage reference represented by Vrectlow by the comparator Comp, the output of which is a square wave Vchop. Vchop is of high voltage level when Vrect is higher than Vrectlow, and Vchop is of low voltage level when Vrect is lower than Vrectlow, meaning that the duty cycle of Vchop is essentially following that of the voltage output from the phase cutter. Consequently the output from the power switched-mode power converter, either current or voltage, is chopped and delivered to the load in accordance with the phase-cut power controller.

At a line frequency of 50/60 Hz, while it is not a problem for incandescent lights, the LED lights may flicker at 100/120 Hz to a level discernible to human eyes. This is due to the fact that, compared to an incandescent light, an LED responds to the pulsating driving current with a much lower electro-optical response time.

Therefore unless the response time of the LED light is sufficiently slowed down by phosphorescence built into the LED device, a higher chopping frequency such as 800 Hz, as recommended by some studies, would be desirable to get rid of the flicker problem. FIG. 4C is a circuit illustrating how this is accomplished. As shown, the rectifier output voltage Vrect is detected and transformed to a DC signal Vrectdc by the DC Sig Gen module such that Vrectdc is representative the magnitude of Vrect, either in RMS or average or any other measures. Vrectdc can also be made representative of the duty cycle of Vrect. Vrectdc drives the pulse width modulation controller PWM Sig Gen which generates a chopping signal Vchop of a frequency 800 Hz or higher, with a duty cycle proportional to Vrectdc. Consequently the output from the power switched-mode power converter and delivered to the load, either current or voltage, is chopped in accordance with the phase-cut power controller at a frequency high enough to remove the flicker effect.

Apart from flickering, there is yet another aspect of the light dimmers in the present market that often fails to meet the expectation of the users, namely to dim the light smoothly to a low or even zero level, and suitably compensated for dilation of the pupils of the viewers as light level is lowered.

For this purpose, a more sophisticated control scheme is required to achieve the above desirable dimming characteristics.

It is therefore desirable also as an objective of the present invention to design a method of control for improved dimming characteristics through phase cutting.

In general for application to DC operated devices, large capacitors are normally indispensable for energy storage in the conversion process from AC to DC. This is even more so for conversion from phase-cut power supplies, when the duty cycle of the supplied voltage can be very small. Large capacitors are needed to store up electrical charge to maintain a continuous power supply for the normal operation of the control circuits. This necessitates the deployment of electrolytic capacitors which unfortunately do not have good reliability and long life as compared to other electronic components such as LEDs and semiconductor ICs. As such, it is also desirable as an objective of the present invention to design a dimmable switched-mode power converter without the need for large capacitors. Without the large capacitors, a byproduct benefit is that large inrush current due to the presence of large capacitors is much reduced, so is the need for input current dampers. A further benefit is that, without the large capacitors, the input line current tends to follow more closely with the input line voltage, meaning that high power factor is preserved.

Please note that throughout the description above and in the following, the TRIAC dimmer is frequently quoted as an example of a typical phase-cut power controller, because it sets a good example for which all the innovations of the present invention apply. Likewise, LED light with switched-mode power converter is frequently quoted as an example of a typical reactive load to the phase-cut power controller. It should therefore be understood that despite of limited examples the description of the present invention and the corresponding claims apply where appropriate to any phase-cut power controllers and to any sorts of loads.

SUMMARY OF THE INVENTION

Accordingly, the objectives of the present invention are to develop a power controlling apparatus and method with the following features:

a) The amount of holding/loading current as required by the phase cutter be met with by the

switching converter without any extra dummy load/bleeder.

b) Smooth dimmer characteristic for lighting loads down to zero, without flickering.

c) Need of electrolytic capacitors reduced.

d) Need of input damping device reduced.

e) High power efficiency and high power factor achieved.

To meet the minimum bleeding/loading current requirements of the phase-cut power controller, the TRIAC dimmer in particular, it is recognized that an independent dummy load/bleeder is not desirable from either cost reduction or energy efficiency point of view. It is proposed that the role of dummy load/bleeder be instead taken up by the switched-mode power converter and the load. Guided by the teaching of the present invention, the current through the phase cutting power controller (or simply, phase cutter) is continuously monitored to see if the requirement of the minimum bleeding/loading current is met. If it falls short, the converter is driven harder (say through increasing duty cycle of PWM) to increase the input current to the converter, hence the bleeding/loading current of the phase cutter, until the requirement is met. Meanwhile, the power delivered to the load is monitored and controlled continuously to a specified power level by driving the converter in the same way as that demanded for the minimum bleeding/loading current. It is fine if the minimum bleeding/loading requirement is met while the specified power of the load is reached. However if the minimum bleeding/loading requirement is not met while the specified power of the load is already reached, driving the converter harder will force a higher power into the load than what is specified by design of the load. To solve this dilemma, the converter is driven harder to increase the bleeding/loading current to meet the requirement of the phase cutter, but at the same time the power delivered to the load will need to be stopped from increasing. There is no way out but to dissipate the extra power somewhere, or to store it up as static energy such as electric charge in the capacitors or electric current in the inductors. It is just fortunate to have the essential elements in a typical switched-mode power converter for this purpose: its switching element(s) can be made to dissipate the extra power, and the inductive elements, capacitor(s) and inductor(s), to store up the energy as delivered by the extra power incurred to meet the loading current requirement of the phase cutter.

As for the way power is controlled by the phase cutter, it is recognized that sometimes it might be necessary to deploy a more sophisticated control scheme for the desired function. A typical example is the control of light by phase-cut dimmer. It is well known that perceived light is affected by iris dilation, a natural reflexive action for adaptation. Therefore low light levels do not appear to

human eyes as low as measured by the lighting power. For most light dimmers now in the market, the range of dimming control range is too narrow that light level goes down too quickly as dimmer is turned down towards the low end and light level remains high to dilated pupils at the low end of the dimmer control. To improve, a "square law" function is proposed to be built into one of the embodiments of the present invention so that power delivered to the load is roughly proportional to the square of the average of the output voltage of the phase cutter.

Further to eliminate the need of large capacitors, an energy feedback scheme is developed to bootstrap up the input voltage to the switch-mode power converter so that converter output power is maintained throughout the valleys of the line voltage without the use of large capacitors for charge storage. Small capacitors in the order of a fraction of microfarads are still needed though for the purpose of EMI filtering.

Additional applications and advantages of the invention will become apparent from the following description and the accompanying drawings. It is understood that changes in the specific structure shown and described may be made without departing from the scope and spirit of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

With the foregoing in view, as other advantages as will become apparent to those skilled in the art to which this invention relates as this patent specification proceeds, the invention is herein described by reference to the accompanying drawings forming a part hereof, which includes descriptions of some typical preferred embodiments of the principles of the present invention, in which:

FIG. 1 is a schematic diagram of a TRIAC Dimmer as a typical phase cutter.

FIG. 2 is a timing diagram showing the leading and trailing edge dimming waveforms.

FIG. 3A is a block diagram of a phase-cut power controlling system with a fixed dummy load.

FIG. 3B is a block diagram of a phase-cut power controlling system with a variable dummy load.

FIG. 4A is a block diagram of a phase-cut power controlling system with output current control.

FIG. 4B is a block diagram of a phase-cut power controlling system with output chopping at

100/120 Hz.

FIG. 4C is a block diagram of a phase-cut power controlling system with output chopping at 800 Hz.

FIG. 5A is a block diagram showing the relationship between the phase cutter current and the power conversion efficiency of the switch-mode power converter.

FIG. 5B is a block diagram of a dimming system with output chopping at 100 Hz as an embodiment of the present invention

FIG. 6 is a circuit diagram of analog-OR as an embodiment of the present invention

FIG. 7A is a schematic diagram showing how efficiency of the switched-mode power converter is reduced by weakening the drive signal to the MOSFET as the power switch

FIG. 7B is a schematic diagram showing how the efficiency of the switched-mode power converter is reduced by negative feedback from the source electrode of the MOSFET as the power switch

FIG. 7C is a schematic diagram showing how efficiency of the switched-mode power converter is reduced by loading the drain electrode of the MOSFET as the power switch.

FIG. 7D is a schematic diagram showing how efficiency of the switched-mode power converter is reduced by negative feedback from the collect electrode of the transistor as the power switch.

FIG. 7E is a schematic diagram showing how input current to the switched-mode power converter is increased by transformer coupled regenerative snubbing

FIG. 7F is a schematic diagram showing how input current to the switched-mode power converter is increased by capacitor coupled regenerative snubbing.

FIG. 8 is a block diagram showing the operation flow for system in FIG. 5

FIG. 9 is a block diagram showing the dimming system with output chopping at 800 Hz as an embodiment of the present invention.

FIG. 10A is a schematic diagram of a Wide-input-range Efficiency-controlled Switched-mode Power Converter, with regenerative snubbing as an embodiment of the present invention

FIG. 10B is a schematic diagram of a Wide-input-range Efficiency-controlled Switched-mode Power Converter, with regenerative snubbing as an embodiment of the present invention

FIG. 11A is a timing diagram showing the input and output waveforms of the Wide-input-range Efficiency-controlled Switched-mode Power Converter

FIG. 11B is the timing diagram of FIG 11A with time scale expanded to show the details of the charging current pulses for regenerative energy transfer.

FIG. 12 is a block diagram showing a dimming system by current (/voltage/power) control as an embodiment of the present invention

FIG. 13 is a block diagram showing a dimming system with square law characteristic as an embodiment of the present invention.

FIG. 14 is a graph showing the LED dimming curves as achieved by an embodiment of the present invention

DETAILED DESCRIPTION OF THE INVENTION

The invention will now be described more specifically with reference to the figures. It is to be noted that the following descriptions of preferred embodiments of this invention are prepared herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the exact forms disclosed, since the teaching of power control by phase cutting according to the present invention may be advantageously used and modified for various applications.

FIG. 5A is a block diagram illustrating how the phase cutter current is related to the power conversion efficiency of the switch-mode power converter, essential for explanation of the principles of the present invention. Shown by circuit (A) is a Switched-mode Power Converter SMPC connected to the rectifier output at voltage Vrect and drawing current Irect from the rectifier and hence the phase cutter (both not shown). The Switched-mode Power Converter SMPC is represented symbolically by a switch SW, with the output delivering a load current Iload to the load LOAD. Assuming that the power efficiency of the converter is Effpc, the power delivered to the LOAD is Vrect x Irect x Effpc. The input current to the converter, i.e. Irect, may be imagined to be composed of two within the converter: Iload which flows to the load LOAD, and Iloss which is the current contributing to all the dissipation (loss) by the switches and all other components of the converter. Assuming further that all the dissipation is on a fictitious load LOSS, then we can redraw an equivalent circuit (B), with Effsw, the efficiency of the switch SW, equal to one, i.e. the switch SW is lossless. Irect = Iload + Iloss, with magnitude of currents and impedances transformed to the input equivalent of the power converter, for ease of analysis.

Equating the input and output power of the converter,

Vrect x Irect = Vrect x Iloss + Vrect x Iload, then,

Effpc x Vrect x Irect = Vrect x Iload

(1-Effpc) x Vrect x Irect = Vrect x Iloss

Therefore Iload = Effpc x Irect

Now if we demand that the dimmer current Irect be always greater than the threshold (such as the holding current threshold of a TRIAC) Ihold, i.e. Irect = Iload + Iloss > Ihold, hence

Iload / Effpc > Ihold

In other words, while maintaining a constant power and hence a constant loading current Iload, we could control the efficiency of the power converter to enable a sufficiently large current flow through the phase cutter for normal operation of the latter.

If however deliberately lowering the efficiency of a power converter is not acceptable, there is one possible way out by channeling part of the current Iloss to an energy storage when increased phase cutter current Irect is demanded, and the stored energy be consumed (by the load) later when reduced phase cutter current is demanded. Such idea is illustrated by Circuit (C) of FIG. 5A, where STOR is the storage element which may be implemented by capacitor or inductors, or even storage batteries. Under the control of the signal Bleed, power switches (not shown)may also be deployed inside the storage element STOR to process the form of the energy (such as raising the voltage) or to control the flow of energy in appropriate direction and at appropriate time. Shown in Circuit (C) as an example, energy may be passed to a buffer capacitor Cbuf when Vrect falls below a predetermined value, through a voltage-controlled unipolar power switch SWvc. Consequently the power converter is partially powered by energy stored in Cbuf during the "valley" period of Vrect, and in particular when bleeding is not required, leading to a smoother converter output. Further details will be discussed in association with FIG. 10A and FIG. 10B.

For illustration of the overall control and maintenance of the phase cutter loading current, a phase-cut power control system with output chopping as an embodiment of the present invention is shown by the block diagram of FIG. 5B. Bleeding current is actively controlled to satisfy the requirement of the phase cutter for the loading current, the holding current of a TRIAC dimmer as a typical example. Dimming control is through 100/120 Hz chopping as explained with respect to FIG. 4B. Compared to FIG. 4B, a Bleed Controller is introduced to control the input current to the switch-mode power converter in meeting simultaneously the minimum current requirement of the phase cutter and the power requirement of the load. Derived from the phase-cut signal by comparing signal Vrect with a predetermined Vrectlow by comparator Comp2, the chopping signal Vchop is applied to the Output Chopper switch, or directly to the Switched-mode Power Converter as indicated by dotted line, as the way shown in FIG. 4B. A capacitor Cf is connected at the input of the power converter for filtering high frequency leakage from the converter, but NOT for filtering the

low frequency ripples from the rectifier. The voltage waveform from the rectifier output should not be distorted by the presence of the capacitor Cf in view of the need of generating the chopper signal Vchop therefrom.

Current output from the rectifier is detected as signal Irect. Irect is representative of the phase-cut current as the preceding filter & damper and rectifier modules should not by design change the current to any significant extent except the very high frequency components which are of no interest as far as bleeding current is concerned. Irect and the point of measurement as shown are chosen as a matter of design convenience. Any other circuit points that would yield the measure of the phase cutter current may be deployed instead for the purpose. Suitably scaled down (not shown), Irect is coupled to a comparator Comp1 of finite gain and compared to a predetermined reference voltage represented by Irectref. This reference voltage can be a constant or a time-varying voltage, and can be chosen to be representative of the minimum bleeding/loading current required for normal operation of the phase cutter, the threshold holding current in case of a TRIAC dimmer for example. The output of the comparator Comp1 is Irecterr, an error signal indicative how far Irect falls short of Irectref. Through an analog-OR gate, the error signal is coupled to the Switch Control Pulse Gen module which generates switching control pulses to drive the Switched-mode Power Converter. By the design, the switch control pulses may have a duty cycle proportional to the error signal Irecterr, such that an increase in the error signal raises the duty cycle of the switch control pulses to the power converter, and thus increasing both the input and output current of the converter.

At the same time, the output from the power converter, indicated by Uspc, is detected. Uspc is representative of any one of the output current, voltage or power. Uspc may also be taken after the Ouput Chopper switch as indicated by the dotted line, filtered before coupled to a comparator Comp3 of finite gain. At comparator Comp3, Uspc is compared to Uspcref, a predetermined reference signal representative the required output current, voltage or power. The result of comparison, Uspcerr, is an error signal indicative as how far the converter output Uspc departs from the reference Uspcref, i.e. how much the converter output falls short of the desired output level. Symmetrical to Irecterr, and through the analog-OR gate, the error signal is also coupled to the Switch Control Pulse Gen module which generates switching control pulses to drive the Switched-mode Power Converter. In other words, there are two error signals presented to the analog-OR gate to control the Switch Control Pulse Gen module. By the operation nature of analog-OR gate, any one of the two inputs with a higher positive signal level dominates the output of the analog-OR gate.

By the prior art, a two-input analog-OR gate can be implemented simply by two diodes with the two cathodes of the diodes connected together as the output of the gate, or by one diode and one resistor with the cathode of the diode connected to the resistor as the output. However analog-OR gates so formed have non-linearity error due to the non-linear characteristic of the diodes. For improvement, a new circuit topology of analog-OR gate is developed as shown in FIG. 6 as an embodiment of the present invention. The design offers the benefit of zero non-linearity error, and each of the inputs can be independently scaled by proper selection of the resistor values. As shown in FIG. 6, the voltage gain for signal Irecterr is equal to (R1+R2)/R2, while voltage gain for signal Uspcerr is (R3+R4)/R4. Further by symmetry of the circuit, it can be expanded to any number of inputs.

With the two error signals presented to the inputs of the analog-OR gate, and assuming equal amplification for the two signals by the gate, there are two scenarios to consider:

Scenario one: Uspcerr is larger than Irecterr, meaning that the demand on the power converter for converter output power is stronger than the demand for the minimum bleeding/loading current. Uspcerr will dominate the analog-OR gate, resulting that the target converter output power to the load being reached at an input current exceeding the minimum bleeding/loading current requirement of the phase cutter. This is an acceptable result any way.

Scenario two: Irecterr is larger than Uspcerr, meaning that the demand on the power converter for the minimum bleeding/loading current is larger than the demand for higher converter output power to the load. Irecterr will dominate the analog-OR gate, resulting that the minimum bleeding/loading current requirement of the phase cutter being met but with the load over-driven because the converter is over-driven only to meet the minimum current requirement. This is an unacceptable situation.

To solve the dilemma, error signal Uspcerr is inverted and coupled to the converter as a signal Bleed. Signal Bleed is a command for the converter to bleed more, i.e. to raise the converter input current but WITHOUT increasing the power output to the load. There is no way out but to dissipate the extra current somewhere, or to store it up as static energy such as electric charge in the capacitors or electric current in the inductors. It is just fortunate to have in a switched-mode power converter the right components for the purpose: the switching elements to dissipate the extra current, and the reactive elements, capacitors and inductors, to store up the energy.

Referring to FIG. 7A which is a schematic diagram displaying part of a Switched-mode Power Converter, with at least one power switching element, preferably the main switching element. Transistor Q1 is such a switching element. To reduce the efficiency of the converter, signal Bleed is applied to the base of transistor Q2 via resistor R3, turning on Q2. This effectively grounds the common node of resistor R2 and capacitor C1, thus lowering the driving to Q1. Consequently the switch Q1 is not completely turned on and off, causing higher volt-drop across the source-drain electrodes of transistor Q1, and longer switching times, resulting in an increased switching loss as heat, right on Q1.

Similarly schematic diagrams of part of Switched-mode Power Converters are displayed in FIG. 7B to 7D, showing how efficiency of the Switched-mode Power Converter is reduced in different ways. As shown in FIG. 7B, efficiency of the Switched-mode Power Converter is reduced by negative feedback from the source electrode of the MOSFET Q1 as the main switch, rendering Q1 more dissipative in switching; in FIG. 7C the efficiency of the Switched-mode Power Converter is reduced by loading the drain electrode of the MOSFET Q1 with a capacitor C1 thus increasing the dissipation on Q1; and in FIG. 7D the efficiency of the Switched-mode Power Converter is reduced by negative feedback from the collect electrode of the bipolar transistor Q1, again rendering Q1 more dissipative.

Instead of dissipating power in the main switch, the energy transferred from the power source associated with the extra bleeding/loading current can also be stored up as static energy through regenerative snubbing. As shown in FIG. 7E, Q1 is the main switch switching the power transformer T1. Inductor L3 is coupled to the transformer T1. When signal Bleed goes high, transistor Q2 is turned on by negative current from comparator IC1, completing the path of L3 and diode D1 for induced current on L3 to flow to the capacitor Cstor . Thus, the input current to the Switched-mode Power Converter is increased by transformer coupled regenerative snubbing. The stored energy in Cstor might be consumed at a later time say when supply from the line is at a low level.

Similarly FIG. 7F shows how input current to the Switched-mode Power Converter is increased by capacitor-coupled regenerative snubbing. Energy is coupled from the drain electrode of the MOSFET Q1 as the main switch.

For a better understanding of the overall operation of the phase-cut power control system shown in FIG. 5B, an operation flow chart is provided in FIG. 8. Starting from the state that the phase-cut AC voltage is filtered, damped and rectified, it is queried as whether the rectifier output current, i.e. the phase cutter current, represented by Irect is higher than the reference current represented by Irectref or not. If no, duty cycle of the switch control signal is increased to drive the output Uspc of the switched-mode power converter up. If yes, it is queried if the converter output Uspc has reached the target value Uspcref. If no, duty cycle of the switch control signal is increased to drive the output Uspc of the switched-mode power converter up. If yes, efficiency of the switched-mode power converter is driven down (by signal Bleed). An equilibrium state is reached when both the converter output Uspc and the phase cutter current Irect have attained the target values at a certain efficiency of the switched-mode power converter.

In parallel to the above flow, the DC power supply for house-keeping, DCS, is powered up, followed by the power up of the Switched-mode Power Converter. Chopping signal Vchop is generated from the phase-cut voltage, and power output from the converter is chopped and delivered to the load.

To reduce the possible flicker effect for LED lights, it is well known that a higher chopping frequency is desirable. FIG. 9 is a block diagram showing the dimming system with output chopping at 800 Hz or higher as an embodiment of the present invention. The chopping operation is similar to what has been described with regard to FIG. 4C. Basically the chopper signal Vchop is generated from a DC signal Vrectdc proportional to the magnitude of the voltage output of the rectifier, represented by Vrect.

Referring to FIG. 9, a Wide-input-range Efficiency-controlled Switched-mode Power Converter abbreviated WESPCO is introduced. In essence, this is a wide-input-range converter developed to cater for the low level input voltage which is often the case in large phase-cut (high dimming) situations. This is also developed with an intention to eliminate the need of large capacitors. An energy feedback scheme is deployed to bootstrap up the input voltage to the switch-mode power converter so that converter output power is maintained throughout the valleys of the line voltage without the use of large capacitors for charge storage. Small capacitors in the order of a fraction of microfarads are still needed though for the purpose of EMI filtering.

FIG. 10A is a schematic diagram of part of a Wide-input-range Efficiency-controlled

Switched-mode Power Converter, for illustration of the key portion of the circuit in connection with both regenerative and dissipative snubbing, but omitting the voltage level translation part for clarity. As shown, by the signal Bleed the transistor Q4 is turned on via U2, so that high voltage pulses at the drain electrode of the main switch MOSFET Q1 is coupled continuously by capacitor C1 to the diode pump formed by rectifying diodes D1 and D2, with charge stored up in capacitor C2. Switch formed by MOSFET Q2 is normally open until switched on by the comparator U1. Vrectf, which is at the output of the filter & damper module which is now positioned after the rectifier module, is coupled to the negative input of the comparator U1 and compared to a predetermined voltage Vrectmin. Vrectmin is chosen to be the minimum voltage to be maintained as Vrectf. Whenever Vrectf falls below Vrectmin, U1 output goes up and turns on Q2, allowing the charge on C2 to be discharged through the diode D4 to the storage capacitor Cstor. As Cstor is charged up, Vrectf goes up and Q2 is switched off as soon as Vrectf is higher than Vrectmin. Charging of Cstor by C2 is stopped and Vrectf goes down as Cstor discharges through the primary coil L1 of transformer T1. The cycle repeats as an oscillation until the line voltage is up and Vrectf rises to a level higher than Vrectmin. Consequently Vrectf is maintained always at a level no lower than the predetermined value of Vrectmin. Note that Vb at the non-inverting input of U2 determines the action level of signal Bleed on regenerative snubbing, while the resistors R1 and R2 determines that on dissipative snubbing on the MOSFET switch Q1. Therefore by adjusting Vb, R1 and R2 the relative priority of regenerative and dissipative actions on MOSFET Q1 can be altered by design.

Similarly, FIG. 10B is a schematic diagram of a Wide-input-range Efficiency-controlled Switched-mode Power Converter, with regenerative energy transferred to the power input by magnetic coupling as an embodiment of the present invention. As shown, inductor L3 is magnetically coupled to the high frequency switching transformer T1 by the action of signal Bleed. C2 is charged up by L3 through diode D2. The operation then follows the same as that described for FIG. 10A.

FIG. 11A is a timing diagram showing the input and output waveforms of the Wide-input-range Efficiency-controlled Switched-mode Power Converter as an embodiment of the present invention. The waveform is generated from a circuit operated according to FIG. 10B with only small capacitors. From top to bottom, the first waveform is the rectified line voltage without filtering, the second is the switched charge current from capacitor C2 to capacitor Cstor. The third one is the voltage Vrectf at the input of the power converter. Note that a minimum voltage of around 100 V is maintained. The bottom waveform is the output voltage of the converter at around 31 V for a load current of around 300 mA.

FIG. 11B is the timing diagram of FIG. 11A with time scale expanded at around 30 ms to show clearly the charging current pulses for regenerative energy transfer.

FIG. 12 is a block diagram showing a dimming system by current (/voltage/power) control as an embodiment of the present invention. Deploying Wide-input-range Efficiency-controlled Switched-mode Power Converter WESPCO and without the chopping approach, a clean DC/AC can be generated for the load. Apart from the Bleed Controller, the operation of circuit is similar to what has been described in FIG. 4A. In general, the output of the converter can be controlled in terms of voltage, current or power by sensing the output Uspc in the respective parameters.

FIG. 13 is a block diagram showing a dimming system with square law characteristic as an embodiment of the present invention. As shown the rectifier output voltage Vrectf, filtered and damped, is detected and transformed to a DC signal Vrectdc by the DC Sig Gen module such that Vrectdc is representative the magnitude of Vrect, either in RMS or average or any other measures. Vrectdc can also be made representative of the duty cycle of Vrect. Vrectdc is presented as an instantaneous reference to the positive input of the comparator Comp3 of finite gain, as Ispcref. Signal Uspcerr, output of Comp3, is responsible for controlling the output of the Wide-input-range Efficiency-controlled Switched-mode Power Converter WESPCO via the analog-OR gate and the Switch Control Pulse Gen module. Signal Uspcerr is also inverted to become signal Bleed for ensuring that the converter output is still in control despite of a conflicting need to satisfy the bleeding/loading requirement of the phase-cut power controller.

Vrectdc is also presented to the Chopper Controller module for generating a chopper signal Vchop to chop the output of the converter WESPCO at a duty cycle in proportion to the magnitude of the phase-cut voltage.

Should the signal Vrectdc be made proportional to the average of the voltage Vrect as output from the phase-cut power controller, it has been proven that

$$Vrectdc = K1*(1-\cos(Alpha))/2$$

where K1 is a scaling factor proportional to the peak value of the sinusoidal input line voltage before phase cutting.

Alpha is the angle of conduction of the phase cutter.

Then the duty cycle will be, according to the design of FIG. 13
DutyC=K2*Vrectdc =K1*K2* (1-cos(Alpha))/2

Further if Uspc is detected as the average power output from the converter WESPCO, then power from the converter is:
Pspc=K3*Vrectdc

Therefore power deliver to the load is

Pload=Pspc*DutyC=K3*Vrectdc*K2*Vrectdc=K2*K3*Vrectdc^2
In other words, power delivered to the load is proportional to the square of the average voltage from the phase-cut power controller.
In terms of the angle of conduction Alpha:

Pload =K2*K3[K1*(1-cos(Alpha))/2]^2
=K1^2*K2*K3*[(1-cos(Alpha))/2]^2
=K*[(1-cos(Alpha))/2]^2 where K= K1^2*K2*K3*

Plotting normalized Vrectdc and Pload gives the illustrative graph in FIG. 14 as the LED light output under two different ways of driving the lights, i.e. curve “a” being proportional to the average of the phased cut voltage, and curve “b” being proportional to the square of the average of the phased cut voltage.

It is well known that perceived light is affected by iris dilation, a natural reflexive action for adaptation. Therefore low light levels do not appear to human eyes as low as measured by the lighting power. Consequently, as light is dimmed down, curve “b” provides a wider and smoother feeling of control than curve “a” over the same lighting range. For higher lighting range, curve “b” is still superior in providing a more “natural” curve than “a” which is more flattened at the top, closer to a “dead” zone meaning that less light level change is felt as the dimmer is turned towards the brightest extreme.

Circuit arrangement as described provides flexibilities for further adjustments of the “dimming’

characteristics of the phase-cut power controllers as needed by the application. For example, should the signal Uspc be made representative of the average output voltage or current of the converter WESPCO, while Vrectdc be made the average of the phase cutter output voltage, the power delivered to the load will be proportional to the third power of the average of the phase-cut output voltage. Further variations dimming characteristics are possible through arrangements of special signal processing of the phase-cut output voltage for the control of the power controller.

Although the invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the invention as described. That is, the discussion included in this application is intended to serve as a basic description. It should be understood that the specific discussion may not explicitly describe all embodiments possible; many alternatives are implicit. It also may not fully explain the generic nature of the invention and may not explicitly show how each feature or element can actually be representative of a broader function or of a great variety of alternative or equivalent elements. Again, these are implicitly included in this disclosure. Where the invention is described in device-oriented terminology, each element of the device implicitly performs a function. Neither the description nor the terminology is intended to limit the scope of the invention.

Claims

What is claimed is:

1. A power controlling apparatus for controlling electrical power delivered from a phase-cut AC power source to a load, said apparatus comprising:
   A rectifying means converting the AC power to DC power;
   A switched-mode power converter with the input coupled to the DC power and the output coupled to the load; and current controlling means to regulate the input current from the power source to the converter through control of the output and efficiency of the converter.
2. The apparatus according to Claim 1, wherein the current controlling means comprises a first sensing means to determine the current from the power source, a second sensing means to determine the output magnitude of the converter; a pulse signal generator controlled by an analog-OR gate of output signals of the two sensing means; wherein the generated pulse signal is coupled to the converter to control the output magnitude of the converter while the inverted signal of the output of the second sensing means is coupled to the converter to control the efficiency of the converter.
3. The apparatus according to Claim 2, wherein the analog-OR gate is comprising two diodes with cathodes connected together as the output, and each of the anodes connected respectively to the output of an operational amplifier, wherein the non-inverting inputs of the operational amplifier are serving as the inputs to the analog-OR gate while each of the inverting inputs of the operational amplifiers is receiving scaled negative feedback from the gate output.
4. The apparatus according to Claim 2, wherein the efficiency of the converter is controlled through controlling the dissipative loss of at least one power switch of the converter.
5. The apparatus according to Claim 2, wherein the input current to the converter is controlled by means of regenerative snubbing of at least one power switch of the converter.
6. The apparatus according to Claim 5, wherein energy is stored up from regenerative snubbing for consumption when bleeding is not required.
7. The apparatus according to Claim 6, wherein the energy is stored in a capacitor, an inductor, a rechargeable battery, or a combination of different energy storage devices.
8. The apparatus according to Claim 6, wherein the stored energy is transferred to the input of

the power converter when the input voltage of the converter is below a predetermined level.

9. The apparatus according to Claim 6, wherein the converter is a wide input range converter.
10. The apparatus according to Claim 9, wherein the output magnitude of the converter is controlled according to the magnitude of the phase cutter output voltage, and power delivered to the load being chopped at a duty cycle according also to the magnitude of the phase cutter output voltage.
11. The apparatus according to Claim 10, wherein the chopping frequency is 800 Hz or above for lighting loads.
12. A method for controlling electrical power delivered from a phase-cut AC power source to a load, said method comprising:

    Converting the AC power to DC power by a rectifier means;

    Coupling the DC power to the input of a switched-mode power converter; coupling the load to the output of the converter; and regulating the input current from the power source to the converter by a current controlling means through the control of the output and efficiency of the converter.
13. The method according to Claim 12, wherein the current controlling means comprises a first sensing means to determine the current from the power source, a second sensing means to determine the output magnitude of the converter; a pulse signal generator controlled by an analog-OR function of the output signals of the two sensing means; wherein the generated pulse signal is coupled to the converter to control the output magnitude of the converter while the inverted output of the second sensing means is coupled to the converter to control the efficiency of the converter.
14. The method according to Claim 13, wherein the analog-OR gate function is implemented by two diodes with cathodes connected together as the output, and each of the anodes connected respectively to the output of an operational amplifier, wherein the non-inverting inputs of the operational amplifier are serving as the inputs to the analog-OR gate while each of the inverting inputs of the operational amplifiers is receiving scaled negative feedback from the gate output.
15. The method according to Claim 13, wherein the efficiency of the converter is controlled through controlling the dissipative loss of at least one power switch of the converter.
16. The method according to Claim 13, wherein the input current to the converter is controlled by means of regenerative snubbing of at least one power switch of the converter.
17. The method according to Claim 16, wherein energy is stored up from regenerative snubbing for consumption when bleeding is not required.

18. The method according to Claim 17, wherein the energy is stored in a capacitor, an inductor, a rechargeable battery, or a combination of different energy storage devices.
19. The method according to Claim 17, wherein the stored energy is transferred to the input of the power converter when the input voltage of the converter is below a predetermined level.
20. The method according to Claim 17, wherein the converter is a wide input range converter.
21. The method according to Claim 20, wherein the output magnitude of the converter is controlled according to the magnitude of the phase cutter output voltage, and power delivered to the load being chopped at a duty cycle according also to the magnitude of the phase cutter output voltage.
22. The method according to Claim 21, wherein the chopping frequency is 800 Hz or above for lighting loads.

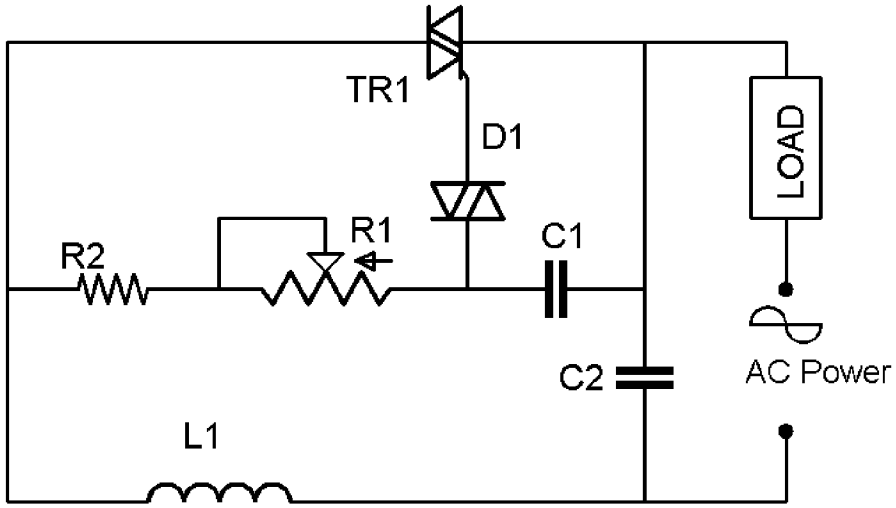


FIG. 1 (Prior Art)

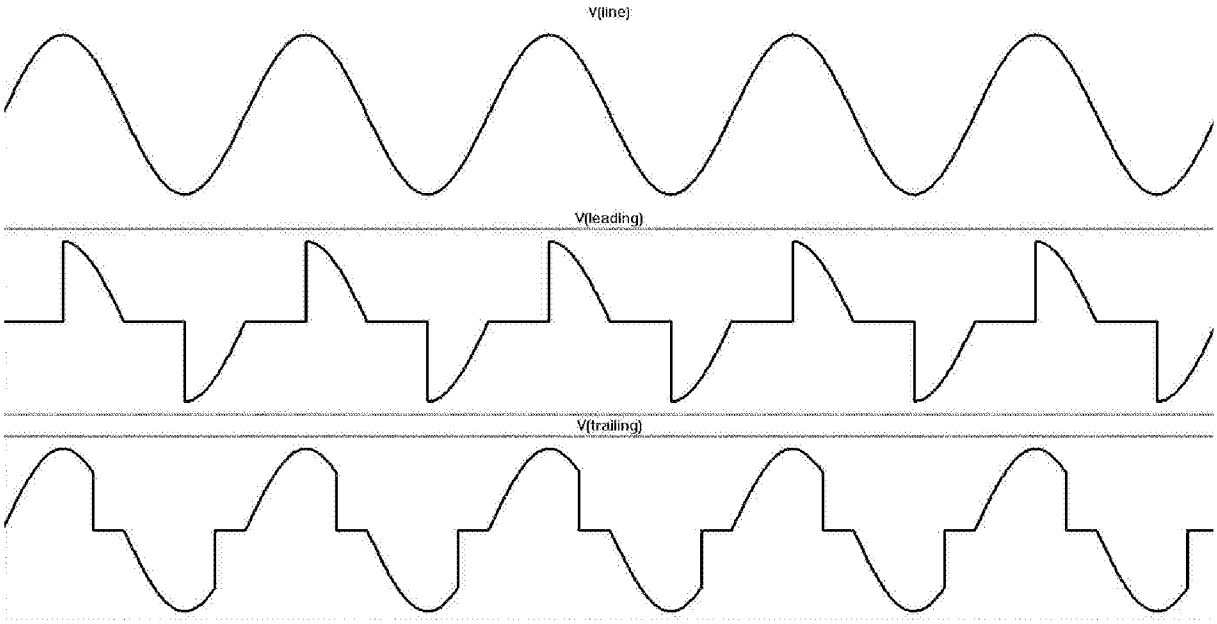


FIG. 2 (Prior Art)

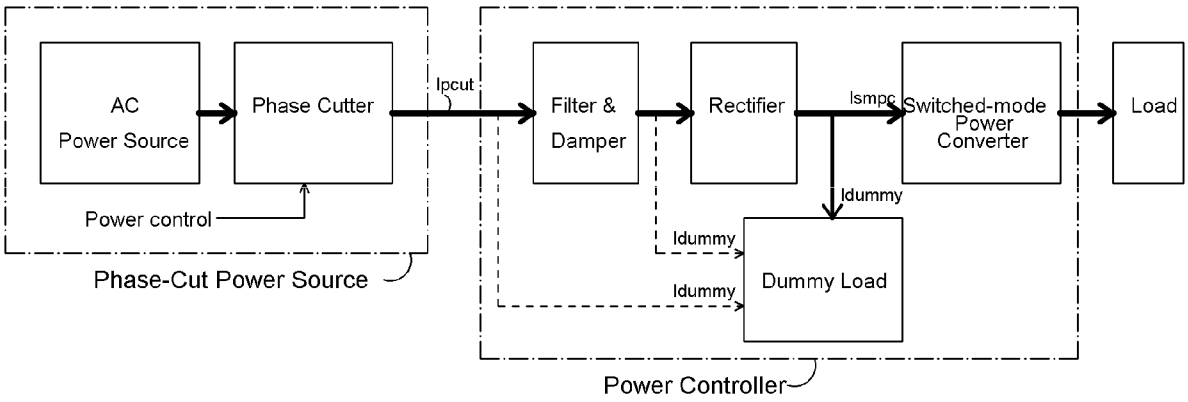


FIG. 3A (Prior Art)

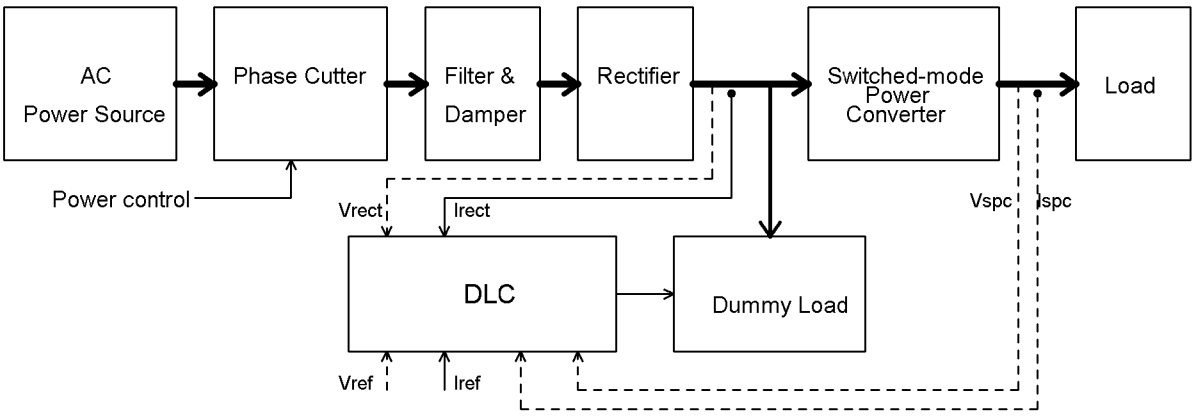


FIG. 3B (Prior Art)

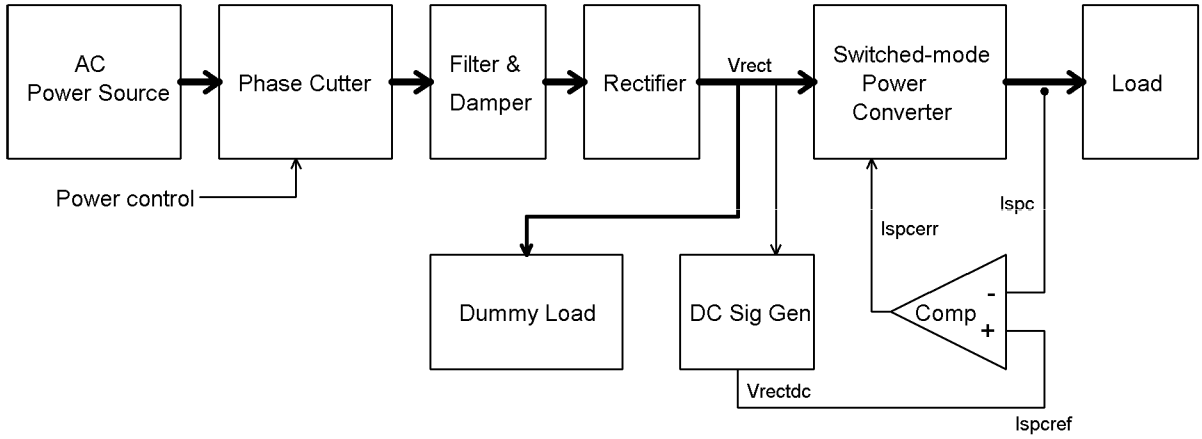


FIG. 4A (Prior Art)

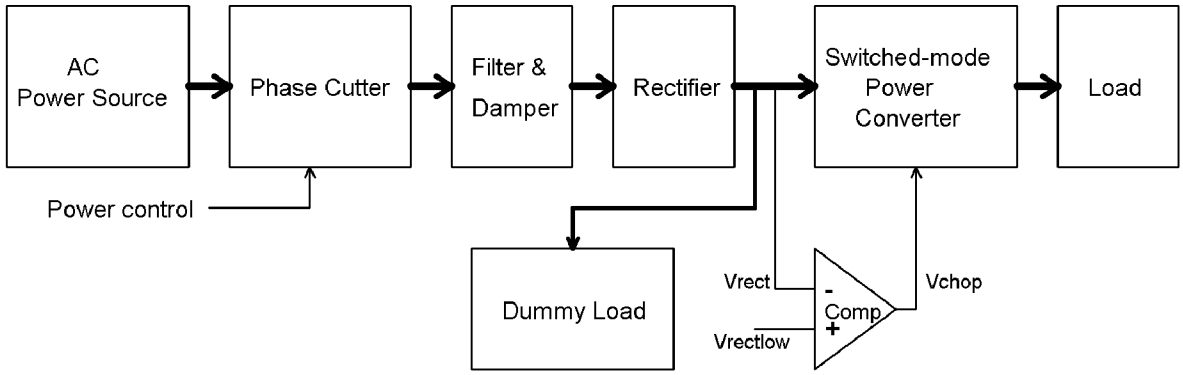


FIG. 4B (Prior Art)

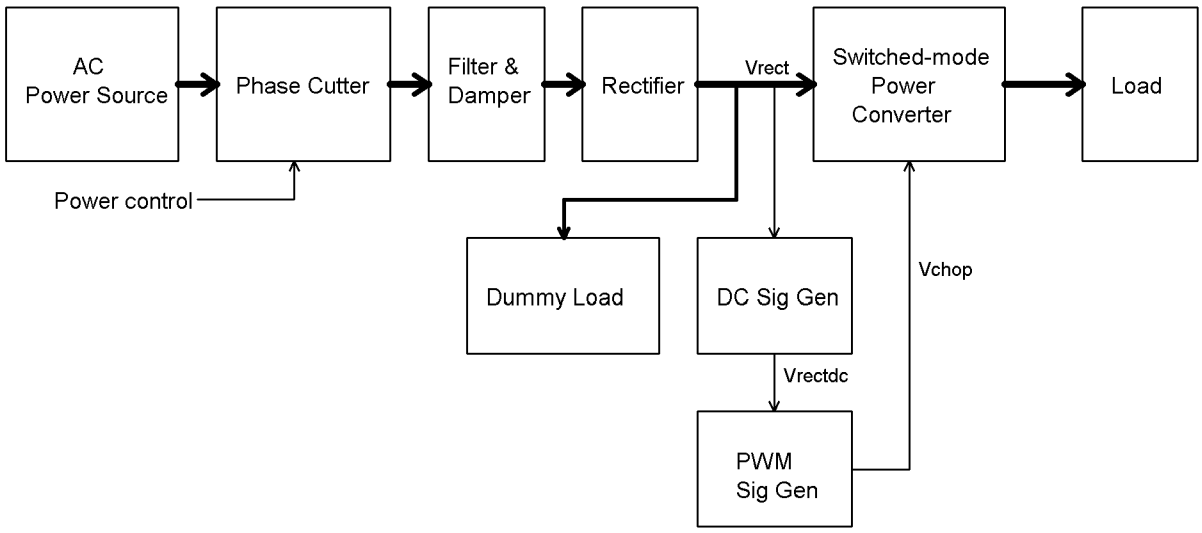


FIG. 4C (Prior Art)

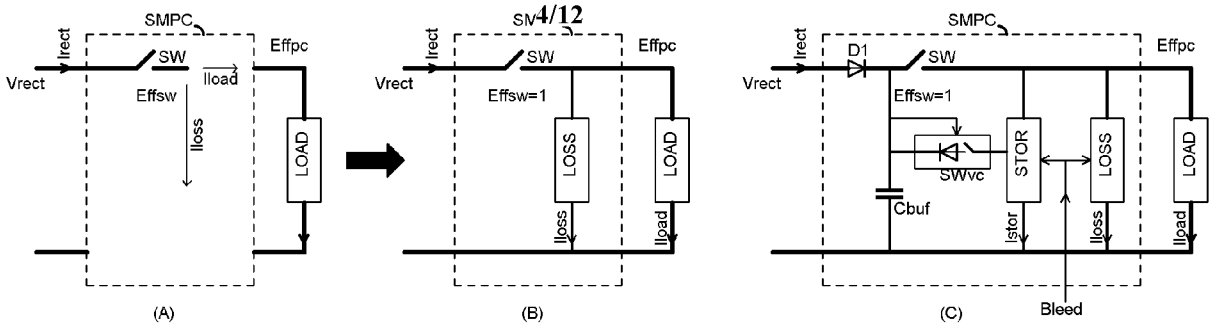


FIG. 5A

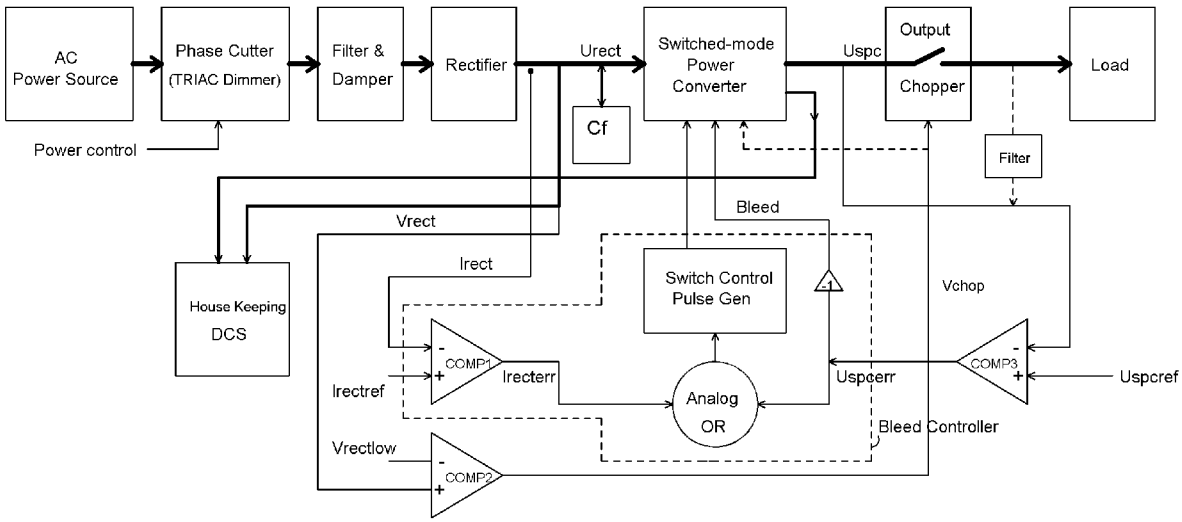


FIG. 5B

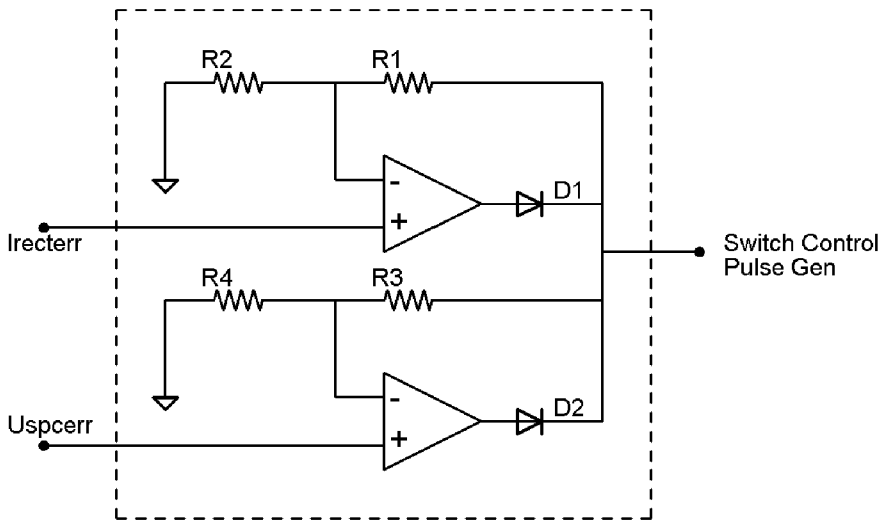


FIG. 6

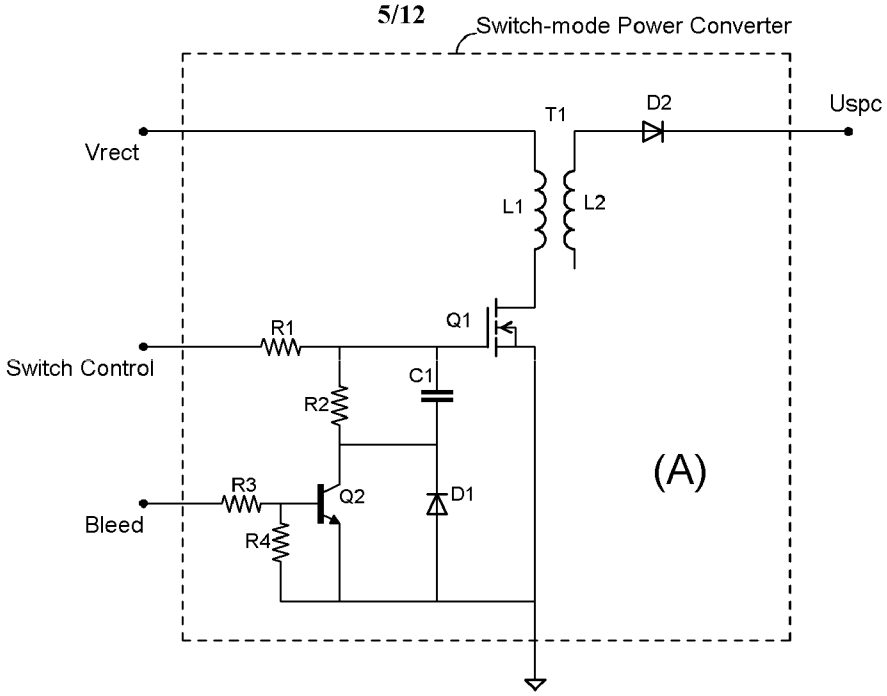

Switch-mode Power Converter
Vrect
T1
D2
Uspc
L1
L2
Q1
R1
Switch Control
C1
R2
R3
Q2
D1
Bleed
R4
(A)

FIG. 7A

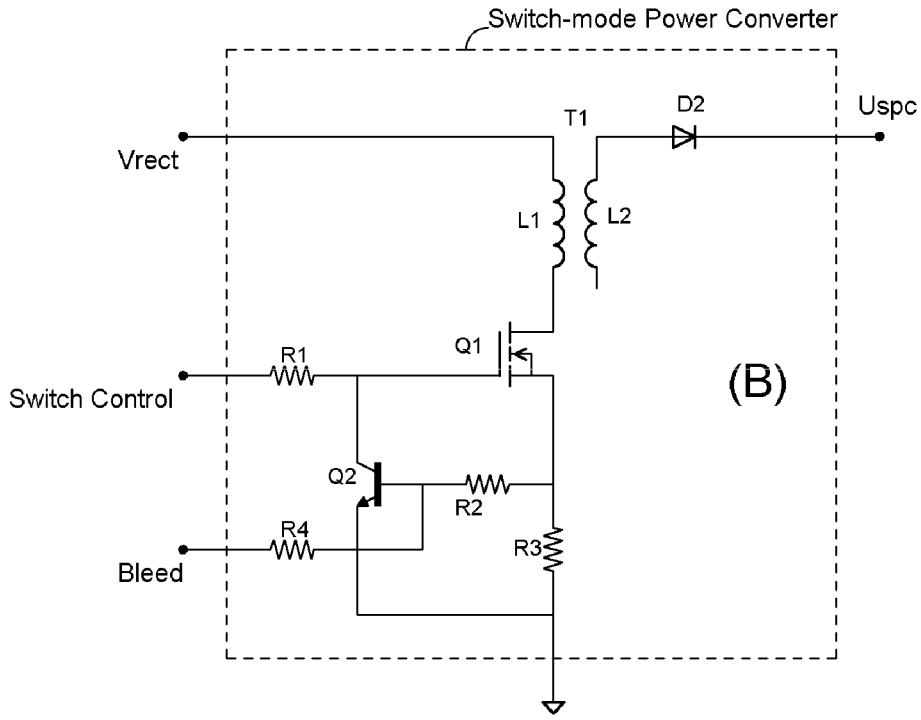

Switch-mode Power Converter
Vrect
T1
D2
Uspc
L1
L2
Q1
R1
Switch Control
(B)
Q2
R2
R4
R3
Bleed

FIG. 7B

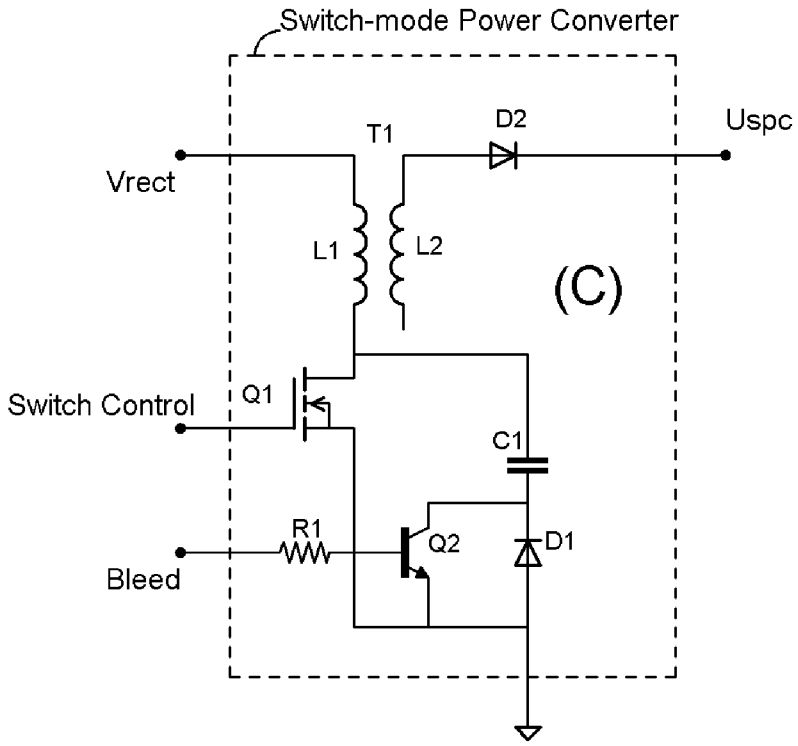

Switch-mode Power Converter
T1
D2
Uspc
Vrect
L1
L2
(C)
Switch Control
Q1
C1
R1
Q2
D1
Bleed

FIG. 7C

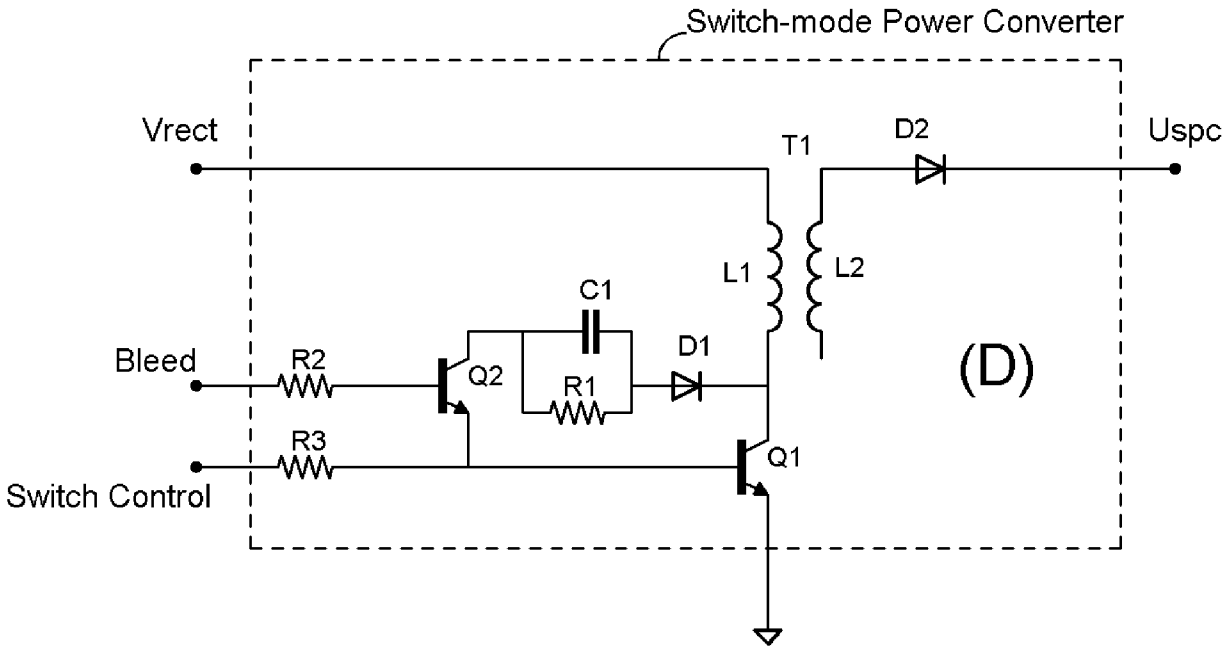

Switch-mode Power Converter
Vrect
T1
D2
Uspc
L1
L2
C1
Bleed
R2
Q2
D1
R1
(D)
R3
Q1
Switch Control

FIG. 7D

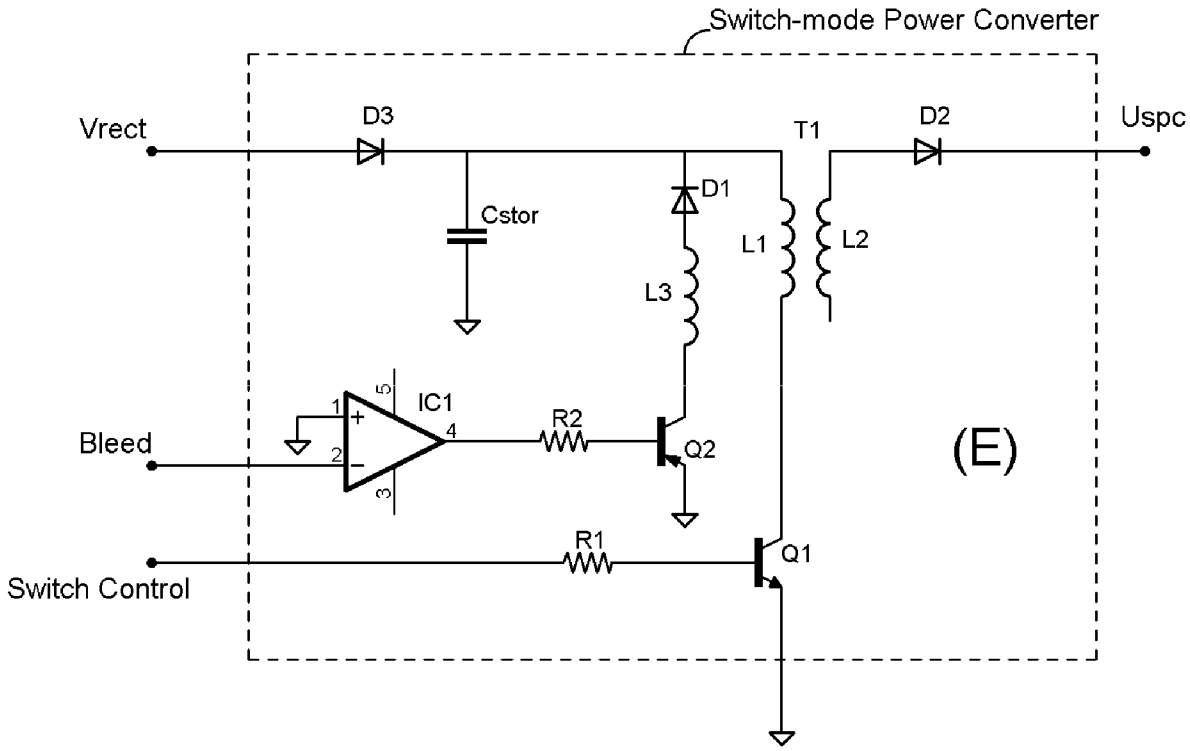

Switch-mode Power Converter
Vrect
D3
T1
D2
Uspc
D1
Cstor
L1
L2
L3
IC1
R2
Bleed
Q2
(E)
R1
Q1
Switch Control

FIG. 7E

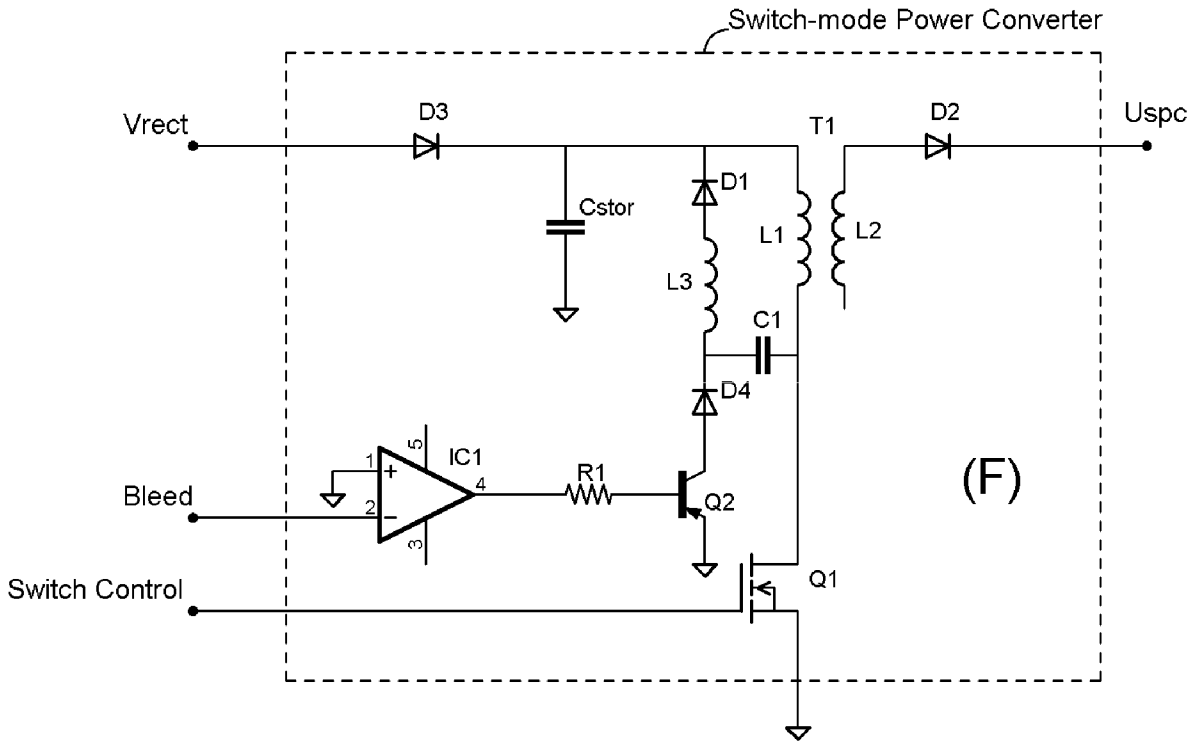

Switch-mode Power Converter
Vrect
D3
T1
D2
Uspc
D1
Cstor
L1
L2
L3
C1
D4
IC1
R1
Bleed
Q2
(F)
Q1
Switch Control

FIG. 7F

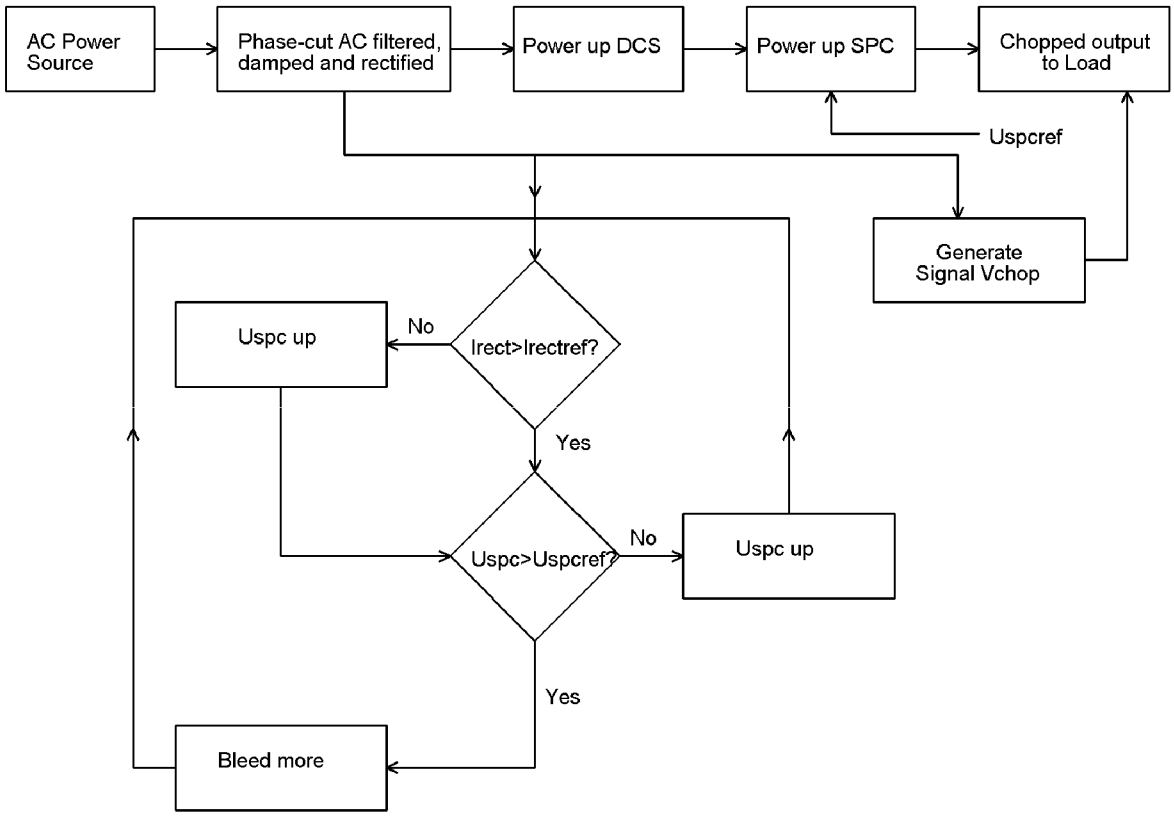

AC Power Source
Phase-cut AC filtered, damped and rectified
Power up DCS
Power up SPC
Chopped output to Load
Uspcref
Generate Signal Vchop
Uspc up
No
Irect>Irectref?
Yes
Uspc>Uspcref?
No
Uspc up
Yes
Bleed more

FIG. 8

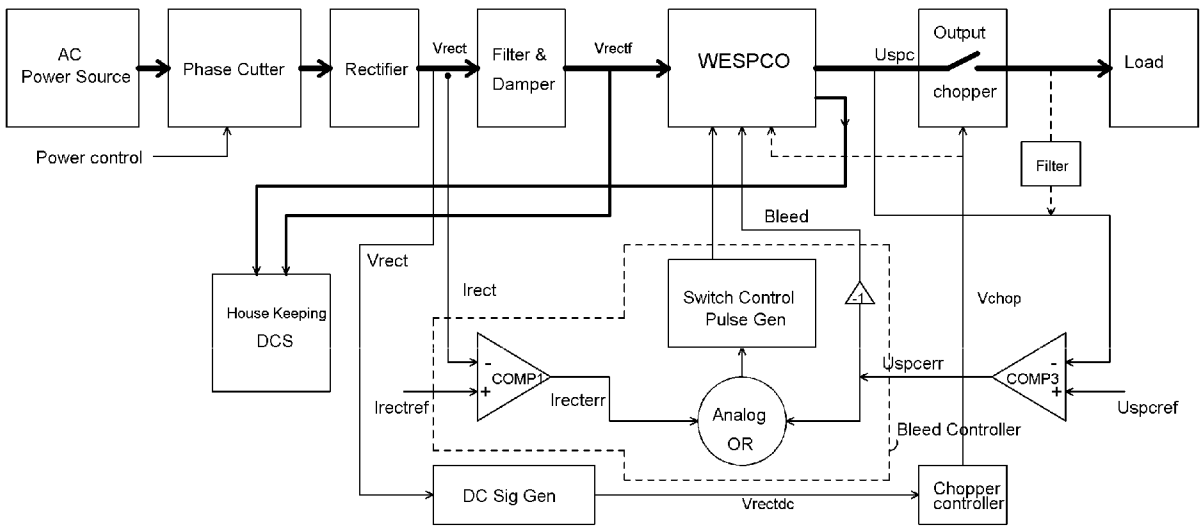

AC Power Source
Phase Cutter
Rectifier
Vrect
Filter & Damper
Vrectf
WESPCO
Uspc
Output chopper
Load
Power control
Filter
Bleed
Vrect
Irect
House Keeping DCS
Switch Control Pulse Gen
-1
Vchop
COMP1
Irectref
Irecterr
Analog OR
Uspcerr
COMP3
Uspcref
Bleed Controller
DC Sig Gen
Vrectdc
Chopper controller

FIG. 9

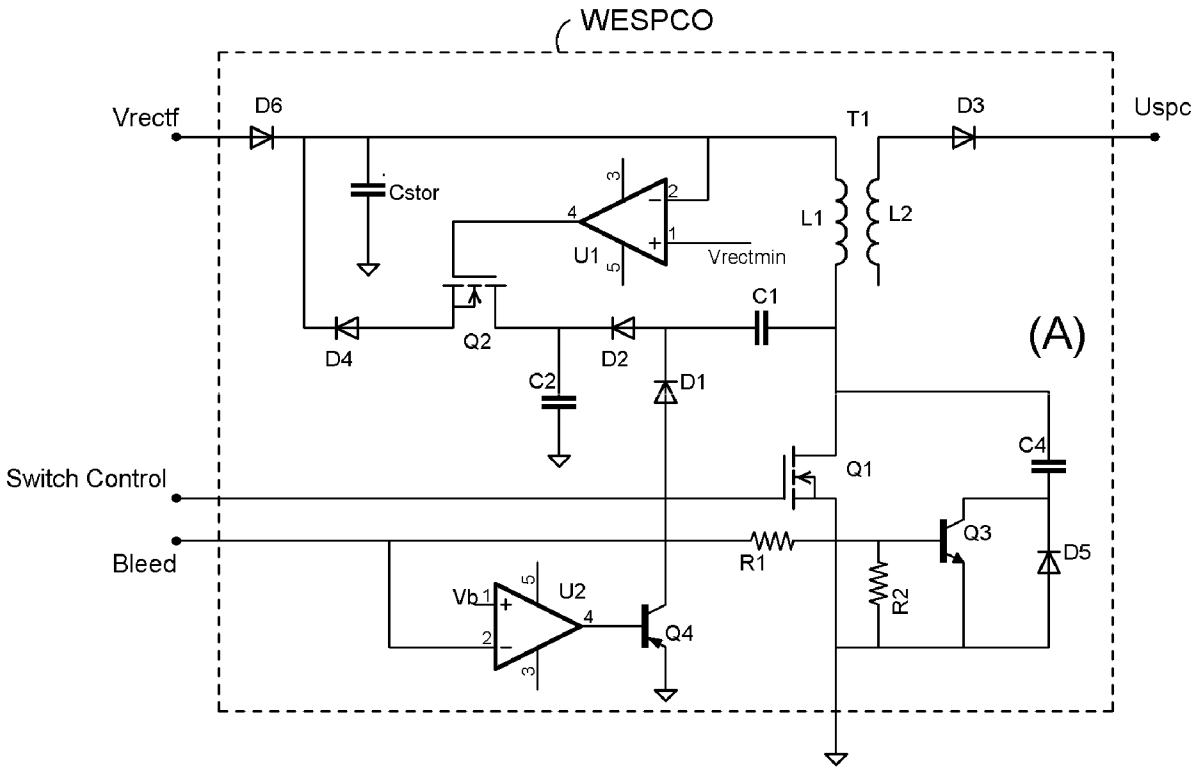


FIG. 10A

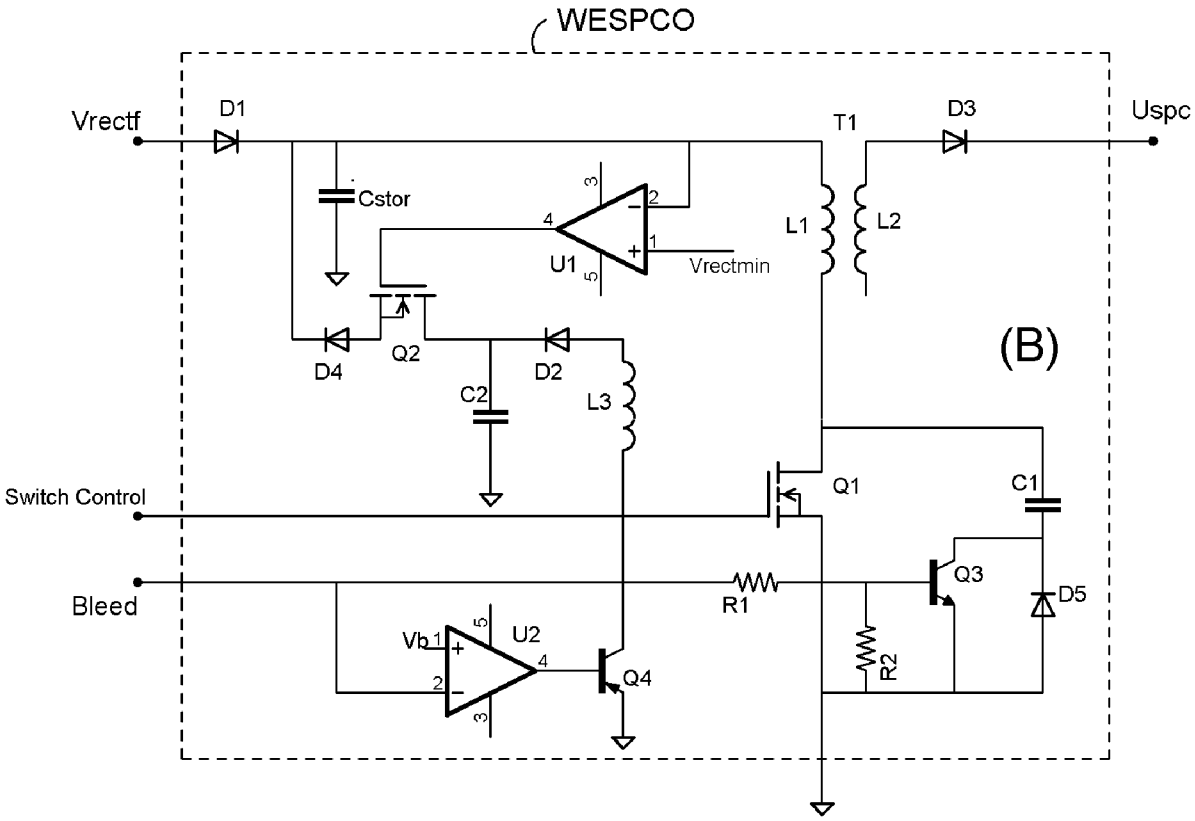


FIG. 10B

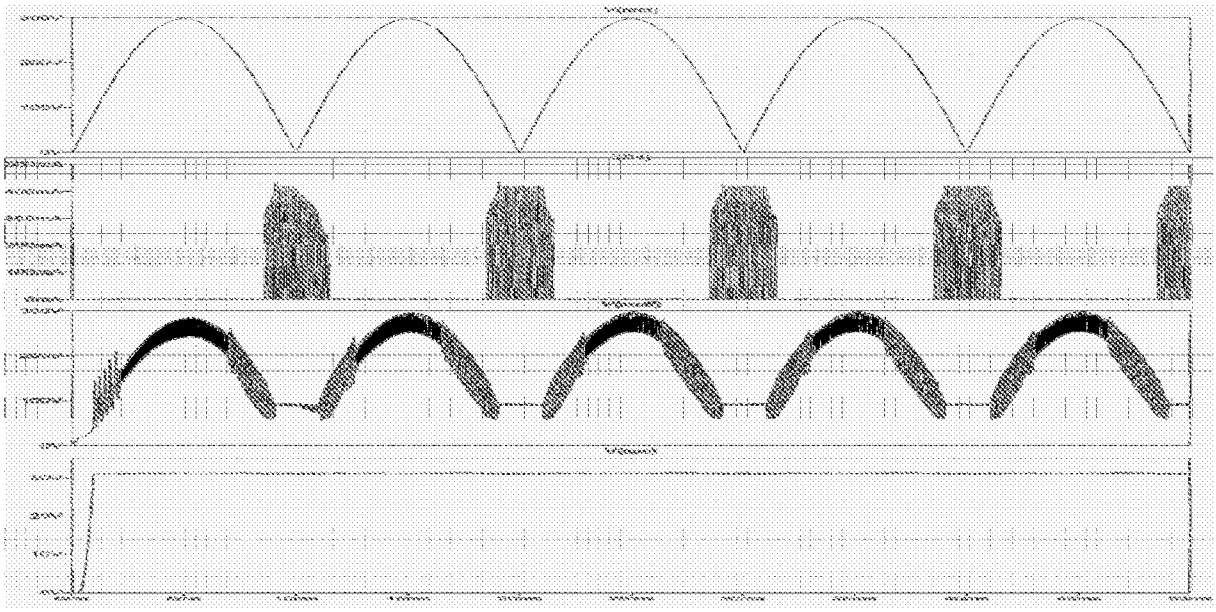


FIG. 11A

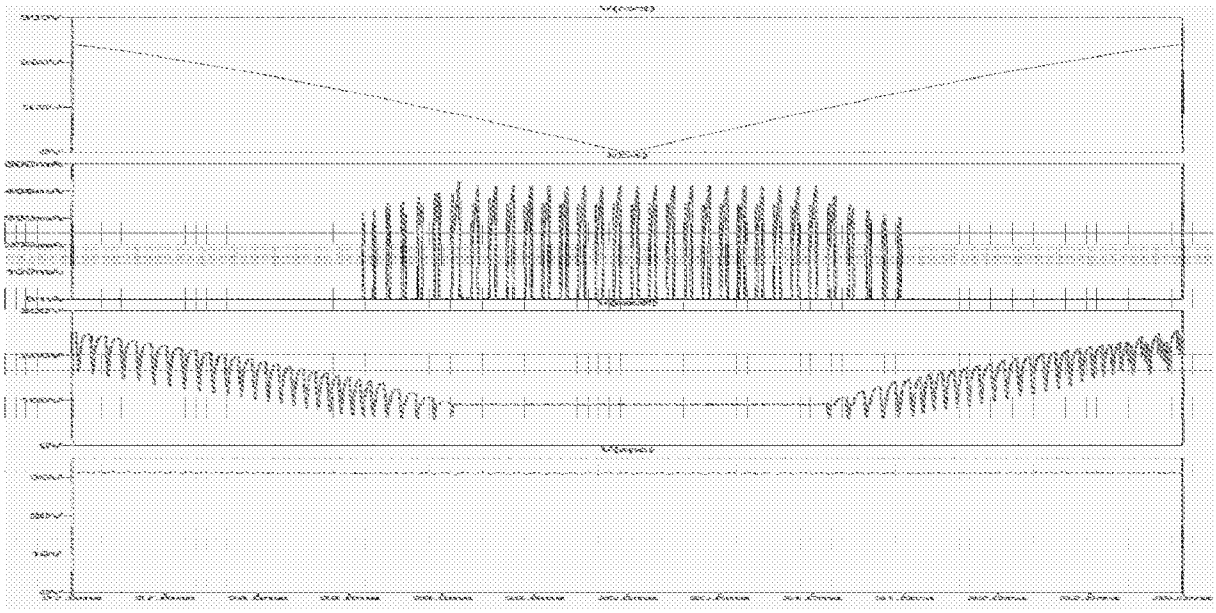


FIG. 11B

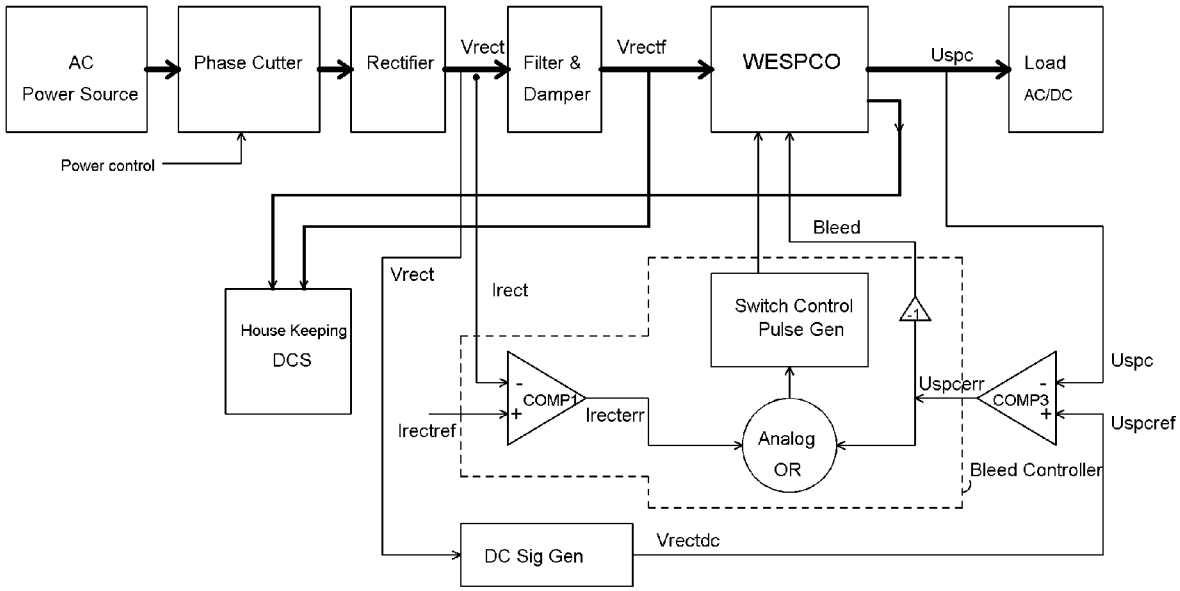

AC
Power Source
Phase Cutter
Rectifier
Vrect
Filter &
Damper
Vrectf
WESPCO
Uspc
Load
AC/DC
Power control
Bleed
Vrect
Irect
House Keeping
DCS
Switch Control
Pulse Gen
-1
Uspc
Uspcerr
COMP3
COMP1
Irectref
Irecterr
Analog
OR
Uspcref
Bleed Controller
DC Sig Gen
Vrectdc

FIG. 12

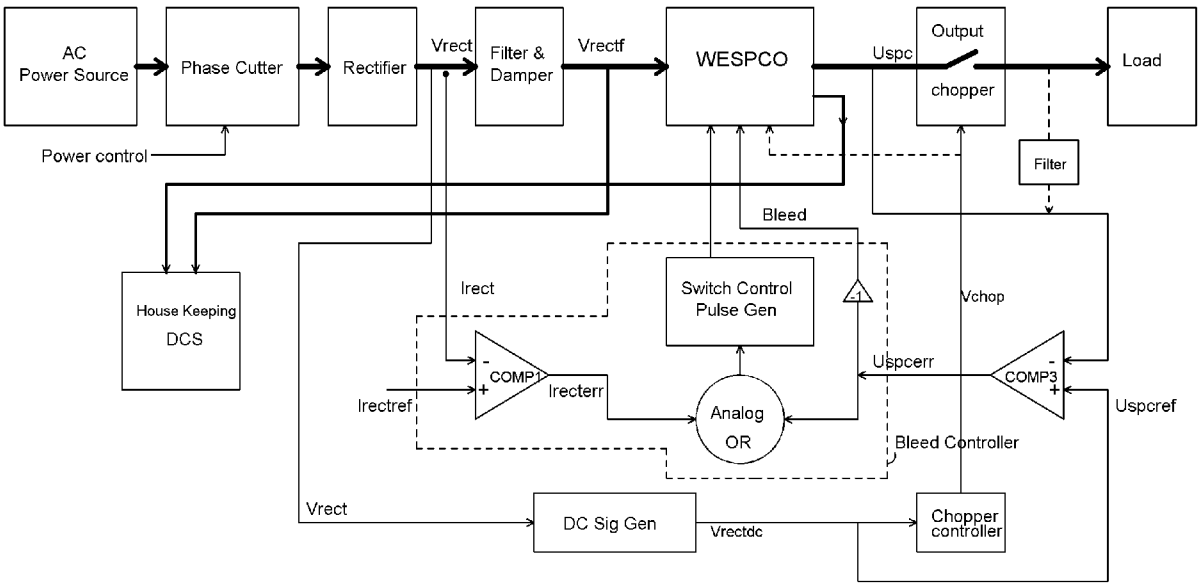

AC
Power Source
Phase Cutter
Rectifier
Vrect
Filter &
Damper
Vrectf
WESPCO
Uspc
Output
chopper
Load
Power control
Filter
Bleed
House Keeping
DCS
Irect
Switch Control
Pulse Gen
-1
Vchop
Uspcerr
COMP3
COMP1
Irectref
Irecterr
Analog
OR
Uspcref
Bleed Controller
Vrect
DC Sig Gen
Vrectdc
Chopper
controller

FIG. 13

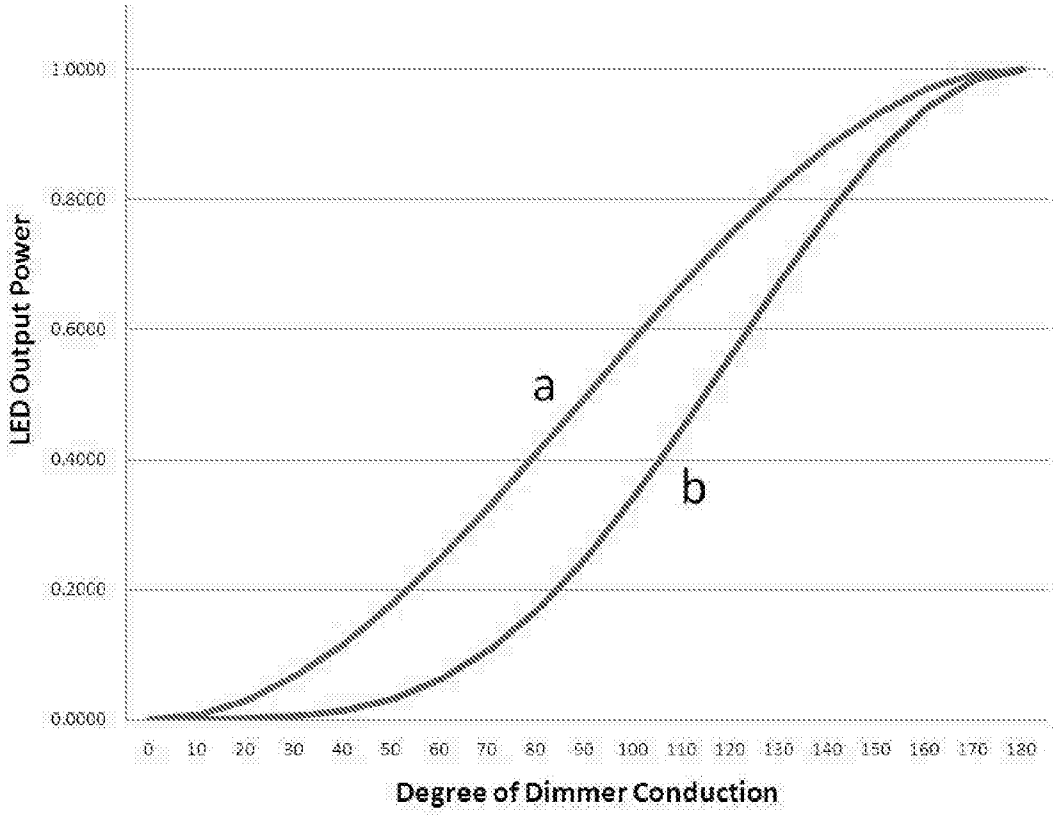

LED Output Power
1.0000
0.8000
0.6000
0.4000
0.2000
0.0000
a
b
0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180
Degree of Dimmer Conduction

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2015/050357

A. CLASSIFICATION OF SUBJECT MATTER

H05B 37/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05B; H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CNPAT,WPI,EPODOC, triac, thyristor, dimmer, LED, light, emitting, diode, efficien+, phase, cut+, switch+, mode, gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2012016197 A1 (CIRRUS LOGIC, INC.) 02 February 2012 (2012-02-02) description, paragraphs [0015]-[0032], and figures 1-6B	1,12
A	WO 2013027121 A1 (MARVELL WORLD TRADE, LTD. ET AL.) 28 February 2013 (2013-02-28) the whole document	1-22
A	WO 2013032592 A1 (OSRAM SYLVANIA INC. ET AL.) 07 March 2013 (2013-03-07) the whole document	1-22
A	CN 202488799 U (OSRAM GMBH) 10 October 2012 (2012-10-10) the whole document	1-22
A	US 2013234613 A1 (MCCUNE, JR., EARL W.) 12 September 2013 (2013-09-12) the whole document	1-22

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 May 2015	**27 May 2015**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	**SHI,Wenqing**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)010-62413411**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IB2015/050357

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		CN 103748753 A	23 April 2014
		US 2013044524 A1	21 February 2013
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		CN 103931273 A	16 July 2014
		EP 2752087 A1	09 July 2014
		US 2014159608 A1	12 June 2014
CN 202488799 U	10 October 2012	None	
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IB2015/050357

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
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		US 2014239833 A1	28 August 2014