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Electronic timepiece

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H3T
Selected US
specifications from
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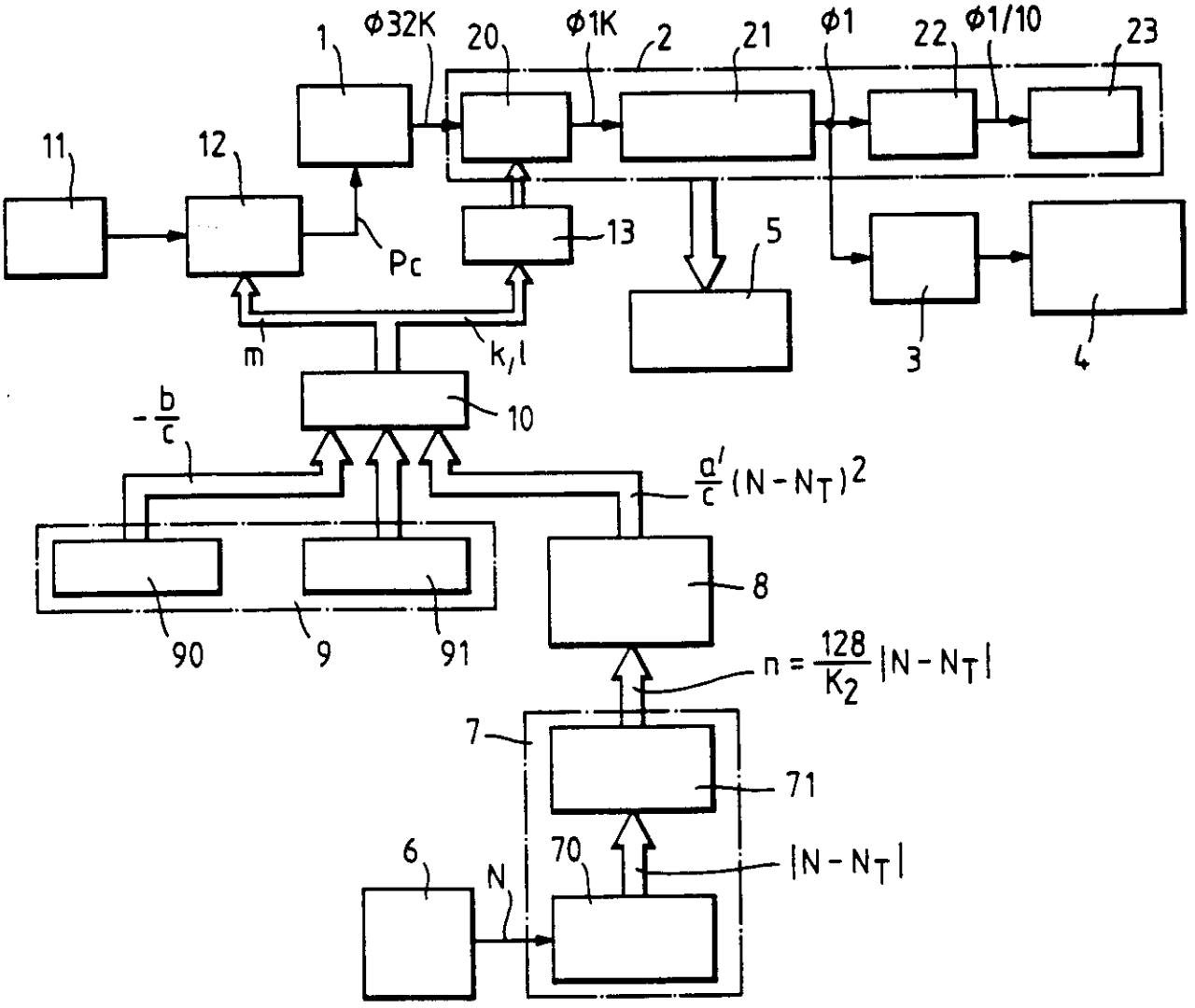
H03L

Fig.1.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Φ32K
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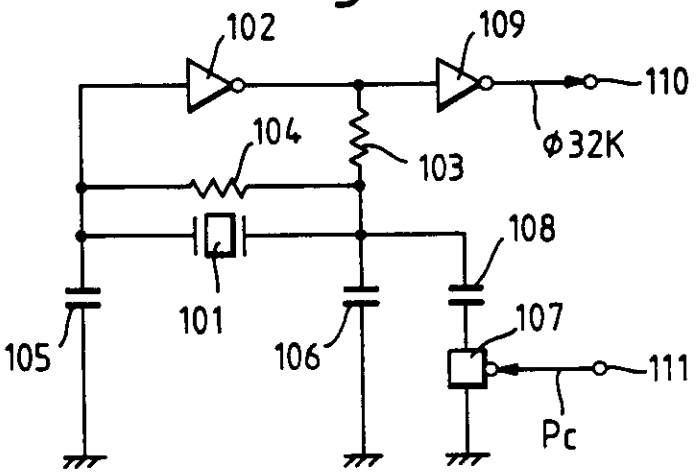
Φ1K
2
21
Φ1
22
Φ1/10
23
11
12
13
5
Pc
m
k, l
3
4
10
$-\frac{b}{c}$
$\frac{a'}{c}(N-N_T)^2$
8
90
9
91
$n=\frac{128}{K_2}|N-N_T|$
7
71
6
N
70
$|N-N_T|$

Fig.6.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Φ32K
104
103
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106
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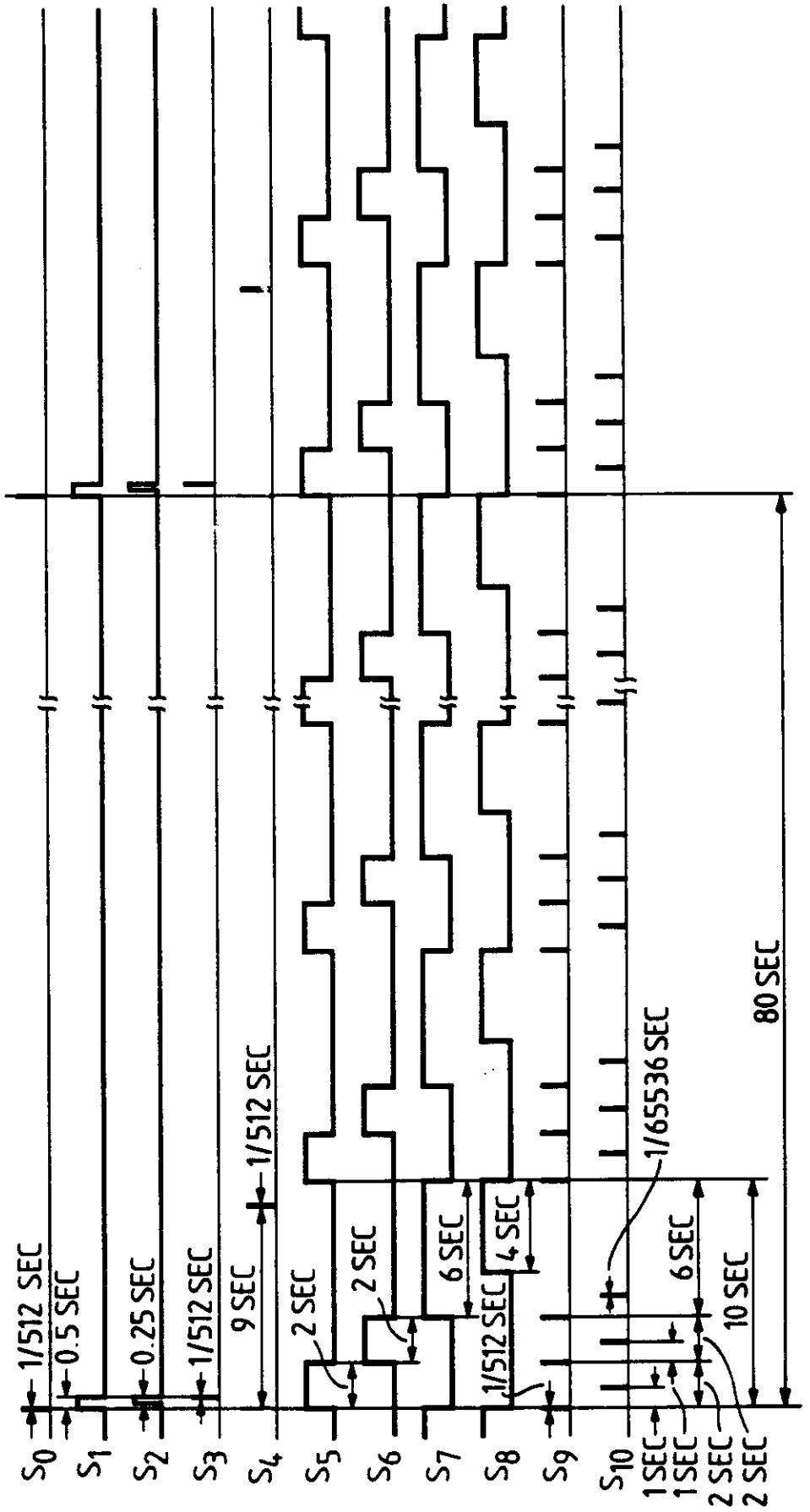
111
Pc

Fig.2.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6 SEC
10 SEC
80 SEC
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S4
S5
S6
S7
S8
S9
S10
1SEC
1SEC
2 SEC
2 SEC

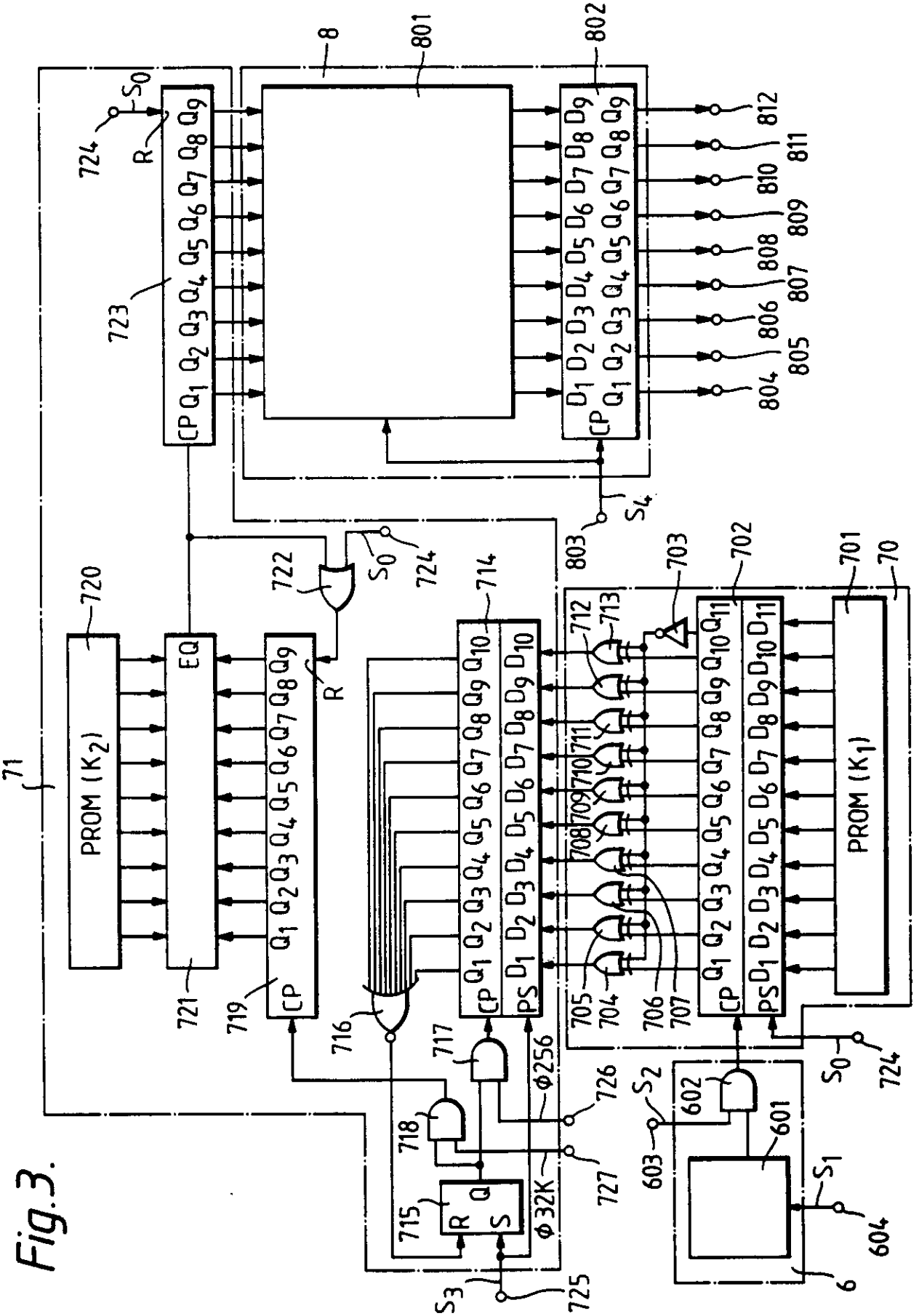

8
801
802
724
S_0
R
723
CP Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9
804 805 806 807 808 809 810 811 812
803
S_4
722
714
712
713
703
702
701
70
71
720
PROM (K_2)
EQ
721
719
716
717
718
715
S
Q
ϕ256
ϕ32K
726
727
725
S_3
705 704 706 707 708 709 710 711
PS
PROM (K_1)
S_2
602
601
603
604
S_1
6

Fig.3.

Fig.4.

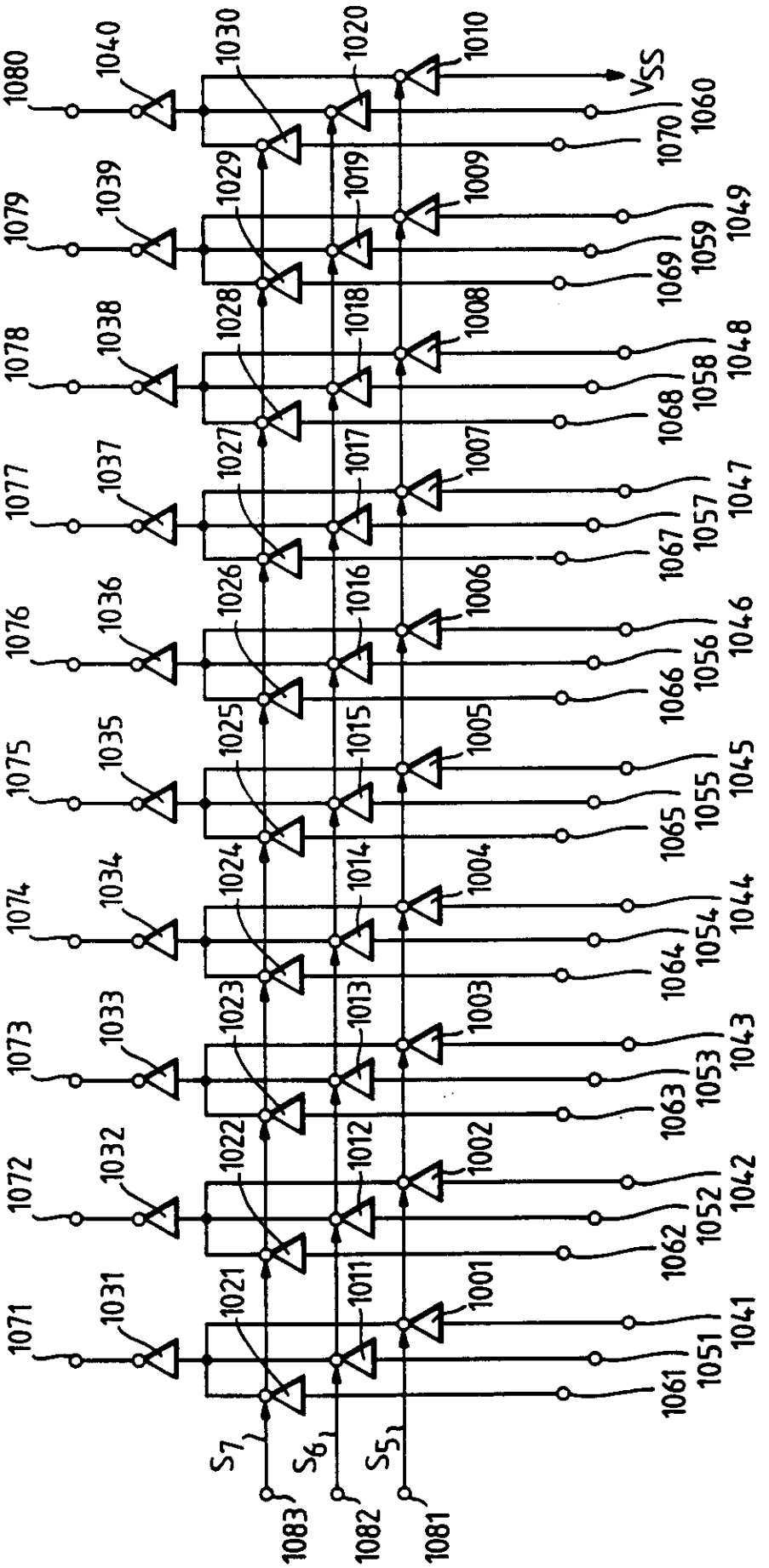
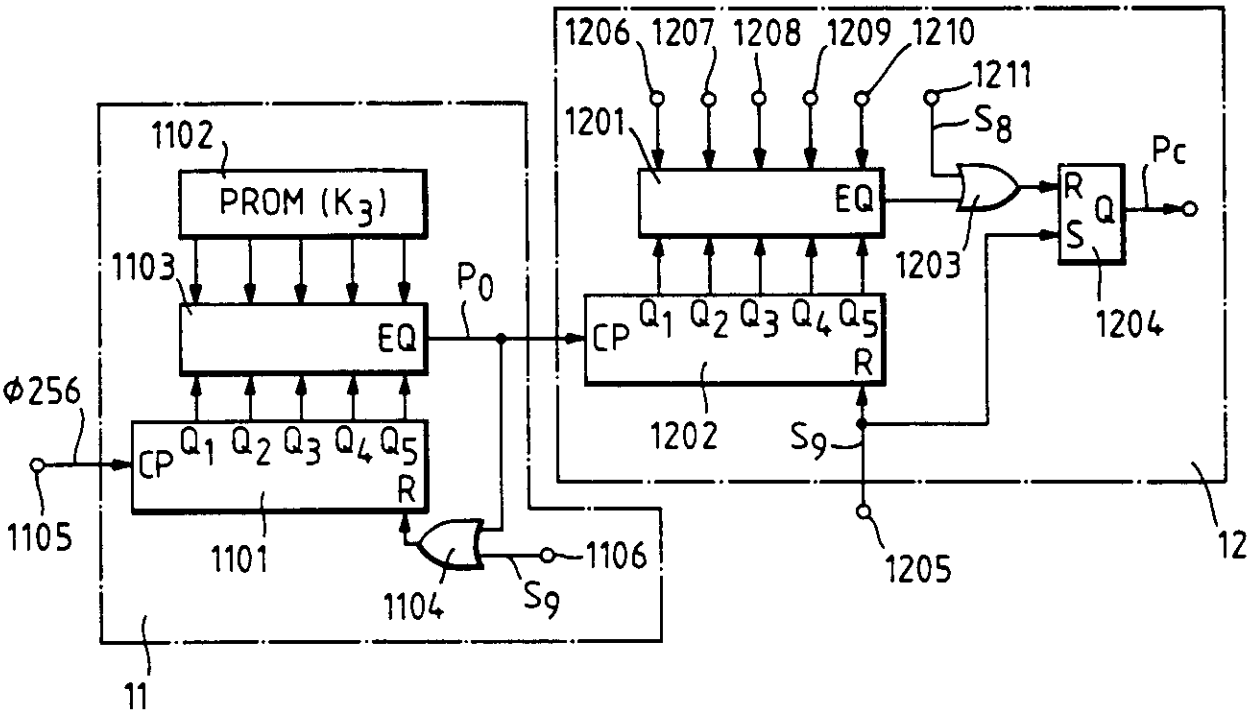


Fig.5.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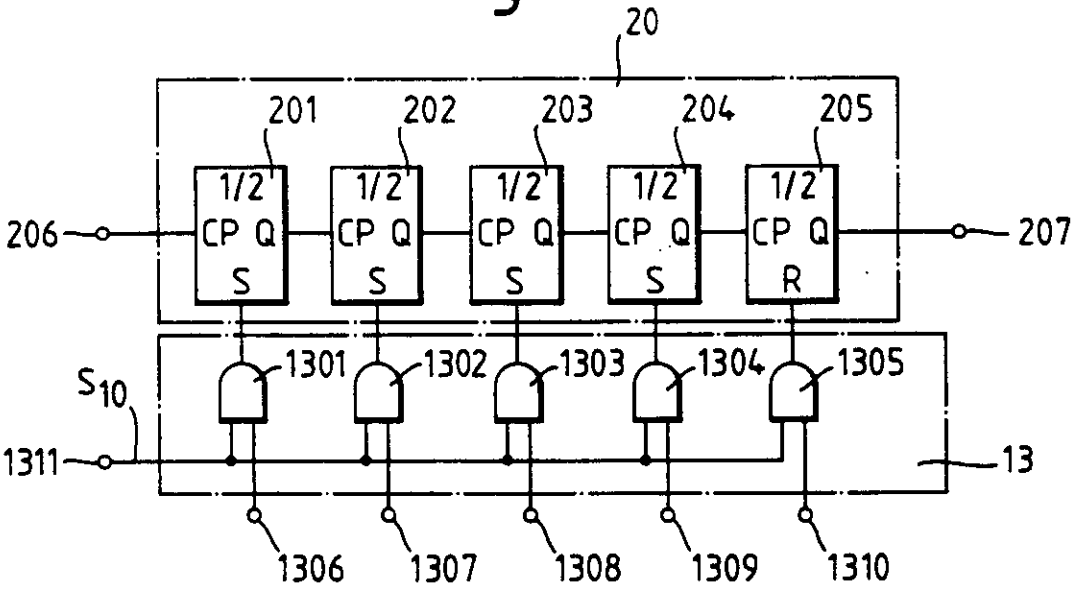
PROM (K_3)
1103
EQ
P_0
ϕ256
CP Q_1 Q_2 Q_3 Q_4 Q_5
R
1105
1101
1104
S_9
1106
11
1206 1207 1208 1209 1210
1211
1201
S_8
EQ
Pc
R Q
S
1203
1204
CP Q_1 Q_2 Q_3 Q_4 Q_5
R
1202
S_9
1205
12

Fig.7.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201 202 203 204 205
1/2
CP Q
S
R
206
207
1301 1302 1303 1304 1305
S_{10}
1311
13
1306 1307 1308 1309 1310

ELECTRONIC TIMEPIECE

This invention relates to electronic timepieces.

Electronic timepieces with a temperature compensation facility are suggested in U.S. Patent Specification No. 3719838 and published Japanese Patent Application Nos. 56-19482 and 58-223778.

U.S. Patent Specification No. 3719838 provides a method wherein data for compensating temperature characteristics of a quartz crystal oscillator corresponding to a given temperature are directly written in to a programmable ROM. Published Japanese Patent Application No. 56-19482 discloses a method wherein temperature compensation data previously written in to a mask ROM whose address is designated by the output conditions of a divider circuit is read out when the number of output pulses of a temperature sensing oscillator circuit reaches a number determined by a dividing ratio setting means.

Further, published Japanese Patent Application No. 58-223778 provides a temperature compensating circuit which adjusts an output of an A/D converter circuit for producing the temperature value, and suggests a method wherein temperature compensating data previously written into a mask ROM is read out by the output of the temperature compensating circuit.

The above have the following disadvantages. With the method disclosed in U.S. Patent Specification No. 3719838 it is possible directly to write temperature compensating data which corresponds to the given temperature into the programmable ROM. Thus, even

though the secondary temperature coefficient and the peak temperature of the quartz crystal oscillator circuit may vary, it is possible to adjust them to the given temperature of each timepiece. It is, therefore, an ideal temperature compensating method. However, the size of a non-volatile memory circuit such as an MNOS transistor memory circuit or FAMOS transistor memory circuit is three to four times the size of a MOS transistor memory circuit such as a mask ROM. Therefore, in the case of an electronic timepiece whose annual rate is 5 seconds and whose memory capacity of the ROM is required in K-bit units, the size of an IC chip becomes extremely large so that it cannot be used in a wristwatch where space is limited.

In the method according to published Japanese Patent Application Nos. 56-19482 and 58-223778, there is no problem regarding the size of memory chips since mask ROMs are used. However, both methods provide means for adjusting an offset amount of the given temperature, but do not provide means for adjusting the rate of change of temperature (i.e. inclination). Thus, it is possible to adjust variation in the peak temperature of a quartz crystal oscillator circuit, but not possible to adjust the variation in the secondary temperature coefficient, so that the more the coefficient departs from the peak temperature, the more the rate of adjustment fails to agree. Therefore, in order to obtain a high degree of accuracy, e.g. an annual rate of 5 seconds, a special quartz crystal vibrator with a particularly advantageous secondary temperature coefficient is required and this results in a high manufacturing cost.

The present invention seeks to provide an electronic timepiece with a temperature compensation facility wherein, no matter how varied the secondary temperature coefficient and peak temperature of the quartz crystal oscillator circuit, they can be adjusted respectively to the rate temperature characteristic of each electronic timepiece, without using a PROM which requires a large-sized IC chip. Further, the present invention seeks to provide time rate adjusting means of high resolution to achieve an electronic timepiece of high precision with an annual rate of a few seconds.

According to the present invention there is provided an electronic timepiece comprising: a temperature signal generating means for producing a temperature signal representative of temperature; temperature signal converting means comprising an offset adjusting means for adjusting an offset amount of said temperature signal and including a PROM for storing the offset amount and an inclination adjustment means for adjusting inclination of said temperature signal and including a PROM for storing the adjusted inclination; a mask ROM for producing rate compensation data corresponding to a temperature converted value produced by said temperature signal converting means; and rate compensating means for compensating a rate of the electronic timepiece in accordance with the rate compensation data.

The electronic timepiece may include a peak rate compensating means for passing preset data relating to the peak temperature rate of the electronic timepiece to the rate compensating means.

The electronic timepiece may include a minimum compensation determining circuit for determining minimum compensation data of

the rate of the electronic timepiece. Preferably the electronic timepiece includes a time dividing circuit for receiving the minimum compensation data for controlling the frequency of the output signal of an oscillator circuit.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of an embodiment of an electronic timepiece according to the present invention;

Figure 2 is a timing chart of output signals of a control signal generating circuit of the electronic timepiece of Figure 1;

Figure 3 is a circuit diagram of a temperature generating circuit, a temperature converting circuit and a temperature characteristic compensation data generating circuit of the electronic timepiece of Figure 1;

Figure 4 is a circuit diagram of a data selecting circuit of the electronic timepiece of Figure 1;

Figure 5 is a circuit diagram of a minimum compensation determining circuit and a time dividing circuit of the electronic timepiece of Figure 1;

Figure 6 is a circuit diagram of a quartz crystal oscillator circuit of the electronic timepiece of Figure 1; and

Figure 7 is a circuit diagram of a logic tuning circuit and a 1/32 divider circuit of the electronic timepiece of Figure 1.

Figure 1 is a block diagram of an embodiment of an electronic timepiece according to the present invention. A quartz crystal oscillator circuit 1 has a secondary temperature characteristic. A divider circuit 2 comprises a 1/32 divider circuit 20 which divides a signal ϕ32K of 32768Hz from the oscillator circuit 1 into a signal

ϕ1K of 1024Hz, a 1/1024 divider circuit 21 which divides the signal ϕ1K into a signal ϕ1 of 1Hz, a 1/10 divider circuit 22 which divides the signal ϕ1 into a signal ϕ1/10 of 1/10Hz and a 1/8 divider circuit 23 which divides the signal ϕ1/10 into a signal ϕ1/80 of 1/80Hz. A driving circuit 3 shapes the alternating signal ϕ1 for driving a stepping motor included in a display mechanism 4. The display mechanism 4 includes a stepper motor, a gear train, a seconds hand, a minutes hand and an hours hand. A control signal generating circuit 5 combines signals of various frequencies shaped by the divider circuit 2 and produces control signal S_0 to S_{10} illustrated by the timing chart of Figure 2. A temperature generating circuit 6 detects the temperature of the electronic timepiece and delivers a plurality of pulses as temperature data N. A temperature converting circuit 7 comprises an offset adjusting circuit 70 for converting the pulses of temperature data N delivered from the temperature generating circuit 6 to the form of $|N - N_T|$ and an inclination adjusting circuit 71 for multiplying $|N - N_T|$ by $128/K_2$ as will be explained in greater detail hereafter. A temperature characteristic compensation data generating circuit 8 outputs 9 bits of temperature characteristic compensating data, $Dn=\left(\frac{a_0}{c}.n^2\right)$ which corresponds to a temperature converting value $n = \left(\frac{128}{K_2}.|N-N_T|\right)$ outputted from the temperature converting circuit 7. A peak rate compensating memory circuit 9 memorizes 10 bits of compensating data $\left[-\frac{b}{c}\right]$ for setting a rate of b sec/day (in equation (1)) at the peak temperature to zero. The peak rate compensating memory circuit 9 comprising a factory compensating memory circuit 90 which can be preset in

the factory where the electronic timepiece is manufactured and an after-sales service compensating memory circuit 91 which can be adjusted during after-sales service. A data selecting circuit 10 selects data designated by a control signal from among the temperature characteristic compensating data, peak rate compensating data from the factory compensating memory circuit 90 and peak rate compensating data from the after-sales service compensating memory circuit 91. A minimum compensation determining circuit 11 determines a minimum compensation c sec/day. A time dividing circuit 12 forms a time dividing signal Pc for compensating the oscillation frequency of the quartz crystal oscillator circuit 1 by using the lower 5 bits of 10 bit data delivered from the data selecting circuit 10. A logic tuning circuit 13 adjusts the rate by advancing or retarding the 1/32 divider circuit 20 as determined by the upper 5 bits of data delivered from the data selecting circuit 10.

Moreover, the factory compensating memory circuit 90 is adjusted using a PROM and the after-sales service compensating memory circuit 91 is adjusted by cutting a wiring pattern of a circuit block.

When the quartz crystal oscillator circuit 1 is not compensated, the rate y with respect to temperature is given by:

$$y = -a \cdot (\theta - \theta_T)^2 + b \ (\text{sec/day}) \qquad (1)$$

wherein a is the secondary temperature coefficient and θ_T is the peak temperature and b is the rate of the peak temperature.

The number of pulses of temperature data N delivered from the temperature generating circuit 6 approximates with respect to

temperature to:

$$N = A\theta + B \qquad (2)$$

wherein A is a constant representing inclination and B is a constant representing the temperature value at $0^{\circ}C$.

From equation (2) the following equation is derived:

$$\theta = \frac{N - B}{A} \qquad (2)'$$

Further, assuming that temperature data N at the peak temperature θ_T is N_T, the following equation is obtained:

$$\theta_T = \frac{N_T - B}{A} \qquad (2)''$$

Substituting equations (2)' and (2)'' into equation (1), it is found that when the quartz crystal oscillator circuit 1 is not compensated, the rate y approximates with respect to the temperature data N according to the following equation:

$$y = -a' \cdot (N - N_T)^2 + b \quad (\text{sec/day}) \qquad (3)$$

wherein a' is a/A^2.

It is found from equation (3) that in order to obtain a flat temperature characteristic of the quartz crystal oscillator circuit 1, the value of the temperature data N obtained by the temperature generating cirucit 6 should be compensated by $\left(a' \cdot (N - N_T)^2\right)$ sec/day in the direction of advance. Therefore, in order to compensate $\left(a' \cdot (N - N_T)^2\right)$ sec/day by means of the minimum compensation c sec/day, the number of steps Y is obtained by the following equation:

$$Y = \left(\frac{a'}{c} \cdot (N - N_T)^2\right) \qquad (4)$$

wherein $(\ )$ indicates an integral number.

On receipt of the temperature converting value n, the temperature

compensating data generating circuit 8 outputs the temperature characteristic compensating data Dn represented by the following equation:

$$Dn = \left(\frac{a'_0}{c}.n^2\right) \qquad (5).$$

In order to generate the temperature characteristic compensating data Dn equivalent to the number of steps Y to be compensated through the temperature characteristic compensating data generating circuit 8, the temperature converting value n given by the following equation is produced by the temperature converting circuit 7:

$$n = \left(\sqrt{\frac{a'}{a'_0}}.|N - N_T|\right) \qquad (6).$$

Herein, since a' is a/A^2, the value of a is in the range between 0.0025 and 0.0035 and the value of A is in the range between 10 and 20. Thus, it follows that the value of a' is in the range between $0.0025/20^2$ and $0.0035/10^2$. When the maximum value $0.0035/10^2$ is a'_0, the value of $\sqrt{\frac{a'}{a'_0}}$ in equation (6) is in the range between 0.4226 and 1. It is difficult to arrange a circuit configuration whereby a value of 0.4226 to 1 is multiplied by $|N - N_T|$. Thus, the value is multiplied by $\sqrt{\frac{a'}{a'_0}} = \frac{128}{K_2}$, so that K_2 is in the range between 128 and 303 (rounded up or down to the nearest whole number in the conventional manner as appropriate). Obtaining the temperature data N from the temperature generating circuit 6, the temperature converting circuit 7 performs operation of $n = \left(\frac{128}{K_2}|N - N_T|\right)$ and delivers the result to the temperature characteristic compensating data generating circuit 8 when the temperature data N is obtained from the temperature generating circuit 6. Thereby, the temperature

characteristic compensating data Dn equivalent to the number of steps Y to be compensated, which is obtained from equation (4), is outputted from the temperature characteristic compensation data generating circuit 8.

Reference is now made to Figure 3, where an example of the circuit arrangement and circuit connection of each of the temperature generating circuit 6, the temperature converting circuit 7 and the temperature characteristic compensation data generating circuit 8 are shown.

The temperature generating circuit 6 comprises a temperature sensing oscillator circuit 601 and an AND gate 602. The temperature sensing oscillator circuit 601 operates only when the control signal S_1 inputted to a terminal 604 is "H" level, and the oscillation frequency f approximates with respect to temperature in accordance with the following equation:

$$f = A'\theta + B' \qquad (7),$$

where A' and B' are constants. The gate 602 passes an output pulse of the temperature sensing oscillator circuit 601 only when the control signal S_2 inputted to a terminal 603 is "H" level. The number of pulses passed through the AND gate 602 is given by equation (2) above and represents the temperature data. In view of the variation of A' in equation (7), the width of the control signal S_2 is set so that the value of A in equation (2) is greater than 10. In this embodiment, the value of A' is greater than 40, so that the width of the control signal S_2 is 0.25 sec.

An offset adjusting circuit 70, which is included in the temperature converting circuit 7, comprises a PROM 701 for memorizing an 11-bit offset adjusting value K_1, a presettable up-counter 702, an inverter 703 and exclusive OR gates (hereinafter referred to as EX-OR gates) 704 to 713. The value of the offset adjusting value $K_1 = [2^{10} - N_T]$ is written into the PROM 701 and this value is inputted to the presettable up-counter 702 at the moment when the control signal S_0 applied to a terminal 724 becomes "H" level. The presettable up-counter 702 counts the pulses passed by the AND gate 602 after the value of $[2^{10} - N_T]$ is preset. Thus, the value represented by output terminals Q_1 to Q_{11} of the presettable up-counter 702 after the count of pulses of the temperature data N becomes $[2^{10} - N_T + N]$. The value of 10-bit data represented by outputs of the EX-OR gates 704 to 713 is the inverted value of the outputs at terminals Q_1 to Q_{10} when an output at the terminal Q_{11} of the presettable up-counter 702 is "L" level. While, when the output of the terminal Q_{11} is "H" level, the value of 10-bit data becomes the value represented by the outputs at the terminals Q_1 to Q_{10}. Therefore, the value represented by the outputs of the EX-OR gates 704 to 713 becomes $[|2^{10} - N_T + N - 2^{10}|] = [|N - N_T|]$.

An inclination adjusting circuit 71, which is included in the temperature converting circuit 7, comprises a presettable down-counter 714, a R-S flip-flop circuit 715 wherein a set signal is preferred, a NOR gate 716, AND gates 717,718, an up-counter 719, a PROM 720 for memorizing 9-bit inclination adjusting value K_2, a coincidence detector circuit 721, an OR gate 722 and an up-counter 723.

Counters 719,723 are reset to zero by the control signal S_0 fed to a terminal 724.

The value [$|N - N_T|$] represented by the outputs of the EX-OR gates 704 to 713 is inputted to the presettable down-counter 714 at the moment when the control signal S_3 inputted to a terminal 725 becomes "H" level. An output of the R-S flip-flop 715 is "H" level from the moment when the control signal S_3 becomes "H" level until the signal ϕ256 applied to a terminal 726 is inputted by [$|N - N_T|$] pulses through the AND gate 717 to a CP terminal of the presettable down-counter 714 and the outputs at terminal Q_1 to Q_9 thereof becomes "L" level and the output of the NOR gate 716 becomes "H" level. During this period the AND gate 718 passes the signal ϕ32K applied to a terminal 727. Therefore, the number of pulses passing through the AND gate 718 is $\frac{32768}{256}$ times the number of pulses passing through the AND gate 717, namely [128 x $|N - N_T|$] pulses.

Being reset by the control signal S_0, the counter 719 starts counting the pulses which pass through the AND gate 718. When the count coincides with the inclination adjusting value K_2 written into the PROM 721, an output EQ of the coincidence detector circuit 721 is "H" level and the counter 719 is again reset, thereby the number of times the output EQ of coincidence detector circuit 721 is "H" level is $\left(\frac{128}{K_2}.|N - N_T|\right)$. Therefore, the temperature converting value n represented by the outputs at terminals Q_1 to Q_9 of the counter 723 is also $\left(\frac{128}{K_2}.|N - N_T|\right)$.

The temperature characteristic compensation data generating circuit 8 comprises a latch circuit 802 and a mask ROM 801 constructed in 9-bit x 300 words which is addressed by outputs at the terminals Q_1 to Q_9 of the counter 723. The temperature characteristic compensation data Dn represented by the above equation (5) is written into address n of the mask ROM 801 and the data is outputted when the control signal S_4 inputted to a terminal 803 is "H" level. The latch circuit 802 holds the temperature characteristic compensation data Dn of the mask ROM 801 for 80 seconds until the following data is outputted.

It will be seen from the following equation that the temperature characteristic compensation data Dn outputted from the temperature characteristic compensation data generating circuit 8 is equal to the number of compensating steps Y represented by equation (4).

$$
\begin{aligned}
Dn &= \frac{a'_0}{c} \cdot n^2 \\
&= \frac{a'_0}{c} \cdot \left(\frac{128}{K_2} \cdot |N - N_T|\right)^2 \\
&= \frac{a'_0}{c} \cdot \left(\sqrt{\frac{a'}{a'_0}} \cdot |N - N_T|\right)^2 \\
&= \frac{a'_0}{c} \cdot \frac{a'}{a'_0} \cdot (N - N_T)^2 \\
&= \frac{a'}{c} \cdot (N - N_T)^2
\end{aligned}
$$

In this embodiment of an electronic timepiece according to the present invention, rate compensation is performed with a period of 10 seconds and compensation of temperature characteristic, peak rate for a factory and peak rate for after-sales service are respectively performed independently at different timing. Compensation

is performed by logic tuning to an accuracy of $\frac{1}{32768} \times \frac{86400}{10} = 0.2637$ sec/day and is further performed by ON and OFF action of a switch 107 (Figure 6) of the quartz crystal oscillator circuit 1 to an accuracy of about $\frac{0.2637}{32} = 0.0082$ sec/day.

Figure 4 is a circuit diagram of the data selecting circuit 10. 9-bit temperature characteristic compensating data outputted from terminals 804 to 812 in Figure 3 is inputted to terminals 1041 to 1049. The factory compensating memory circuit 90 is a 10-bit peak rate compensation memory circuit whose outputs are inputted to terminals 1051 to 1060. Further, the after-sales service memory circuit 91 is a 10-bit peak rate compensation memory circuit whose outputs are inputted to terminal 1061 to 1070. Clocked inverters 1001 to 1010 are held ON for a period of 2 seconds when the control signal S_5, which is inputted to a terminal 1081 is "H" level, and deliver the temperature characteristic compensation data via inverters 1031 to 1040 to terminals 1071 to 1080. Clocked inverters 1011 to 1021 are held ON for a period of 2 seconds when the control signal S_6, which is inputted to a terminal 1082, is "H" level, and deliver the peak rate compensating data for a factory via the inverters 1031 to 1040 to the terminals 1071 to 1080. Further, clocked inverters 1021 to 1030 are held ON in a remaining period of 6 seconds when the control signal S_7, which is inputted to a terminal 1083, is "H" level, and deliver the peak rate compensating data for after-sales service via the inverters 1031 to 1040 to the terminals 1071 to 1080.

Figure 5 illustrates the minimum compensation determining circuit 11 in greater detail. The minimum compensation determining circuit 11 comprises an up-counter 1101, a PROM 1102 for memorizing a 5-bit minimum compensation determining value K_3, a coincidence detector circuit 1103, and an OR gate 1104. When the counter 1101 counts the signal $\phi 256$ inputted to a terminal 1105 K_3 times, an output signal P_o at a terminal EQ of the coincidence detector circuit 1103 becomes "H" and the up-counter 1101 is reset. Thus, after the control signal S_9 inputted to a terminal 1106 becomes "H" level and the up-counter 1101 is once reset, one period of the signal P_0 at the output terminal EQ of the coincidence detector circuit 1103 is thus $\frac{K_3}{256}$ seconds.

The time dividing circuit 12 as shown in Figure 5 comprises a coincidence detector circuit 1201, an up-counter 1202, an OR gate 1203 and a R-S flip-flop circuit 1204 in which a reset signal is preferred. Terminals 1206 to 1210 are connected to receive the lower 5-bit data from the terminals 1071 to 1075 (Figure 4) of the 10-bit data selected by the data selecting circuit 10. On the assumption that the value represented by the lower 5-bit data is m, when the up-counter 1202 counts the signal P_0 by m pulses after being reset by the control signal S_9 inputted to a terminal 1205, the output at terminal EQ of the coincidence detector circuit 1201 becomes "H" level. The time dividing signal Pc is set by the control signal S_9 inputted to the terminal 1205. The time dividing signal Pc is reset when the output at the terminal EQ

of the coincidence detector 1201 becomes "H" level or the control signal S_8 inputted to a terminal 1211 becomes "H" level. Therefore, the time when the time dividing signal Pc becomes "H" level is $\frac{K_3}{256}$.m sec. Here, it is assumed that the temperature characteristic compensation data represented by the terminals 1206 to 1210 is m_1, peak rate compensating data for a factory is m_2 and peak rate compensating data for after-sales service is m_3, m_1 is indicated in the first 2 seconds of the compensating period of 10 seconds, m_2 is indicated in the next 2 seconds and then m_3 is indicated for the remaining 6 seconds. Since during the last 4 seconds of the remaining 6 seconds, the time dividing signal Pc becomes "L" level by the control signal S_8, the time when the time dividing signal Pc becomes "H" level is $\frac{K_3(m_1+m_2+m_3)}{256}$sec and the time when the time dividing signal Pc becomes "L" level is $\left\{10 - \frac{K_3(m_1+m_2+m_3)}{256}\right\}$sec. The quartz crystal oscillator circuit 1 oscillates at the rate of $(y + \Delta y)$ sec/day when the signal Pc is "H" level, and oscillates at the rate of y sec/day when Pc is "L" level. Therefore, the rate compensated by the time dividing signal Pc is given by the following equation:

$$\frac{(y+\Delta y)\times\frac{K_3(m_1+m_2+m_3)}{256} + y \times \left\{10 - \frac{K_3(m_1+m_2+m_3)}{256}\right\}}{10} - y$$
$$= \frac{K_3(m_1+m_2+m_3)}{2560}.\Delta y \text{ sec/day} \qquad (8)$$

From equation (8) minimum compensation c is given by:

$$C = \frac{K_3}{2560}.\Delta y \text{ sec/day} \qquad (9)$$

In this embodiment the minimum compensation c is 0.2637/32 sec/day.

Thus it is preferable that the value K_3 obtained by the following equation is written into the PROM 1102:

$$K_3 = \left\{ \frac{0.00824 \times 2560}{\Delta y} \right\} \qquad (10)$$

Figure 6 is a circuit diagram of the quartz crystal oscillator circuit 1. The quartz crystal oscillator circuit 1 comprises a tuning fork type crystal vibrator 101 cut at an angle of $+5^{\circ}$ with respect to the X axis, an oscillation inverter 102, a ballast resistor 103, a negative feedback resistor 104, gate capacitors 105,106, an inverter for waveform shaping 109, the switch 107 already referred to and a switch 108 which is capable of being switched by the switch 107. Two different frequencies of the signal ϕ32K at a terminal 110 depend upon the ON and OFF states of the switch 107. When the time dividing signal Pc fed to a terminal 111 is "L" level, the oscillator oscillates with a smaller rate y sec/day. While, when the signal Pc is "H" level, oscillation is performed at a greater rate (y + Δy) sec/day. The capacitance of the switching capacitor 108 is determined in such a manner that the value of Δy is necessarily larger than 0.2637X10/2 = 1.3185 sec/day since compensation is performed for 2 seconds out of 10 seconds.

Figure 7 is a circuit diagram of the 1/32 divider circuit 20 and the logic tuning circuit 13. The logic tuning circuit 13 comprises AND gates 1301 to 1305. The 1/32 divider circuit comprises an input terminal 206, 1/2 divider circuits 201 to 204 with set terminals S, a 1/2 divider circuit 205 with a reset terminal R and an output terminal 207. At the moment when the control signal

S_{10} inputted to a terminal 1311 becomes "H" level, the 1/32 divider circuit 20 is set to the state of advance or delay determined by input data of terminals 1306 to 1310 of the logic tuning circuit 13. Upper 5-bit data among the output data of the data selecting circuit 10 is inputted to the terminals 1306 to 1310. Compensation according to the data is performed once per 10 seconds. Therefore, on the assumption that the temperature characteristic compensating data applied to the terminals 1306 to 1309 is k_1, peak rate compensating data for factory applied to the terminal 1306 to 1309 is k_2, peak rate compensating data for after-sales service applied to the terminals 1306 to 1309 is k_3, peak rate compensating data for factory applied to the terminal 1310 is ℓ_2 and peak rate compensating data for after-sales service applied to the terminal 1310 is ℓ_3, compensation due to logic tuning is given by the following equation:

$$0.2637 \times \left\{(k_1+k_2+k_3)-32 \times (\ell_2+\ell_3)\right\} \text{ (sec/day)} \qquad (11)$$

From equations (8) to (11) compensation of the rate is given by the following equation:

$$\frac{0.2637}{32} \times \left\{(m_1+m_2+m_3) + 32 \times (k_1+k_2+k_3) - 1024 \times (\ell_2+\ell_3)\right\} \text{ (sec/day)} \qquad (12)$$

In order to obtain the value of a', N_T and b in the equation (3) which are necessary for adjusting temperature characteristic and the peak rate, rates y_1, y_2, y_3 corresponding to three known temperatures $\theta_1, \theta_2, \theta_3$, and the number of pulses N_1, N_2, N_3 of the temperature data respectively at these temperatures are measured and

the following simultaneous equations are solved:

$$y_1 = -a'.(N_1 - N_T)^2 + b$$
$$y_2 = -a'.(N_2 - N_T)^2 + b$$
$$y_3 = -a'.(N_3 - N_T) + b \qquad (13)$$

In this calculation the data at temperature θ is not required, thus it is not necessary to know the exact temperature and also to adjust exact temperature environment. Further, since the difference in the rate Δy required for adjusting the minimum compensation is almost equal in all ranges of temperature, measurement at temperature of above θ_1,θ_2, and θ_3 can be performed. Based on the values of a', N_T, b and Δy which are obtained in the above manner, the folowing calculation can be performed:

$$K_1 = \left(2^{10} - N_T\right), \quad K_2 = \left(128 \times \sqrt{\frac{a'_0}{a'}}\right),$$
$$K_3 = \left(\frac{0.00824 \times 2560}{\Delta y}\right), \quad K_4 = \left(-\frac{b}{c}\right).$$

The values obtained are respectively written into the PROM 701, the PROM 720, the PROM 1102 and the factory compensating memory circuit 90, thereby adjustment of temperature characteristic, minimum compensation and peak rate adjustment can be effected. This measurement and adjustment are performed electronically and can be automated so that cost for adjustment is small.

As noted above, in the electronic timepiece with temperature compensation facility, based upon the fact that the rate y is represented by equation (3) with respect to the value of temperature data N, $N' = |N - N_T|$ is obtained by the offset adjusting circuit 70 and the temperature converting value $n = \left(\frac{128}{K_2}.N'\right)$ is obtained by the inclination adjusting circuit 71. Therefore, the value of

the temperature characteristic compensating data $Dn = \left\{\frac{a'_0}{c}.n^2\right\}$ which is written into address n of the mask ROM 801 becomes equal to the number of compensation steps Y given by the equation (4), and thereby a flat temperature characteristic is realised.

Further, the minimum compensation determining circuit 11 sets the minimum compensation c sec/day to the value of $1/2^5$ of 0.2637 sec/day being the minimum compensation by logic tuning, namely, it is set to 0.00824 sec/day. Thus, the peak rate is sufficiently compensated to the accuracy required for the desired annual rate. Furthermore, the amplitude of the temperature characteristic after compensation is far smaller than that by only logic tuning. Moreover, in accordance with this embodiment, when peak rate adjustment is necessary because of aging or failure by cutting the pattern of after-sales service memory circuit 91, adjustment is precisely and quickly done in the same manner as logic tuning even in a general watchmaker's premises.

It will be appreciated that whilst compensation by each set of data is independently performed at different timing it is also possible to employ a method where the data is added by use of an adding circuit.

In the electronic timepiece according to the present invention and described above with a temperature compensation facility, variation in the offset amount of the temperature values and in peak temperature of quartz crystal vibrators can be adjusted by an offset adjusting circuit, and the variations in the inclination of temperature value and in the secondary temperature coefficients

of the quartz crystal vibrators can be adjusted by an inclination adjusting circuit. Therefore, this invention enables a mask ROM of large integration to produce temperature characteristic compensating data suitable for the characteristics of the rate and temperature of each timepiece, without using a special quartz crystal vibrator with specific peak temperature and secondary coefficient characteristics. As a result, low-priced and small-sized timepieces of high precision are realised.

Further, as noted above, the electronic timepiece may be of high precision by providing a first compensation circuit which controls the oscillator circuit by the lower M-bit data and compensates the rate adjustment and a second compensation circuit which controls the divider circuit with the remaining upper bits of data, the rate compensation data and then compensates the rate. In addition, there is provided means wherein the minimum compensation of the first compensation circuit is set to $\frac{1}{2^M}$ of the minimum compensation of the second compensation circuit. Therefore, when the value of the rate compensation data represented as D-bit data is d, the value represented by the lower M-bit of the D-bit data is m, the value represented by the remaining K-bit is k and the minimum compensation of the second compensation circuit is g sec/day, the compensation is represented by $(\frac{g}{2^M}.m+g.k) = \frac{g}{2^M}.(m+2^M k) = \frac{g}{2^M}.d$ sec/day, so that digital tuning having a resolution of $\frac{g}{2^M}$ sec/day and adjusting width of $(\frac{g}{2^M}.2^D) = (g.2^K)$ sec/day is achieved.

As shown in the above embodiments, in the case when the first

and second compensation circuits are controlled by 5-bit data and the minimum compensation width of the second compensation circuit is 0.2637 sec/day, a digital tuning method having a resolution of $\frac{0.2637}{2^5}$ = 0.00824 sec/day equivalent to a trimmer capacitor and large adjusting width of $0.2637 \times 2^5 = 8.4384$ sec/day is realised.

Therefore, the electronic timepiece according to the present invention and described above achieves rate adjustment to a high degree of accuracy, precisely and quickly. Further, since the trimmer capacity is not used, there is no change of the rate due to failure or humidity change and a small-sized timepiece is also realised.

Attention is drawn to British Patent Application No. 8710556 (Serial No 2190218) in which protection is sought for matter described in this specification.

CLAIMS

1. An electronic timepiece comprising: a temperature signal generating means for producing a temperature signal representative of temperature; temperature signal converting means comprising an offset adjusting means for adjusting an offset amount of said temperature signal and including a PROM for storing the offset amount and an inclination adjustment means for adjusting inclination of said temperature signal and including a PROM for storing the adjusted inclination; a mask ROM for producing rate compensation data corresponding to a temperature converted value produced by said temperature signal converting means; and rate compensating means for compensating a rate of the electronic timepiece in accordance with the rate compensation data.

2. An electronic timepiece as claimed in claim 1 including a peak rate compensating means for passing preset data relating to the peak temperature rate of the electronic timepiece to the rate compensating means.

3. An electronic timepiece as claimed in claim 1 or 2 including a minimum compensation determining circuit for determining minimum compensation data of the rate of the electronic timepiece.

4. An electronic timepiece as claimed in claim 3 including a time dividing circuit for receiving the minimum compensation data for controlling the frequency of the output signal of an oscillator circuit.

5. An electronic timepiece as claimed in claim 1 and substantially as herein described with reference to and as shown in the accompanying drawings.

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