United States Patent

[11] 3,582,689

[72] Inventors **Kenneth C. Smith**
Weston, Ontario;
Adel S. Sedra, Toronto, Ontario, both of, Canada

[21] Appl. No. **769,798**
[22] Filed **Oct. 23, 1968**
[45] Patented **June 1, 1971**

[73] Assignee **Canadian Patents and Development Limited**
Ottawa, Ontario, Canada

[54] CURRENT CONVEYOR WITH VIRTUAL INPUT REFERENCE POTENTIAL

2 Claims, 7 Drawing Figs.

[52] **U.S. Cl.** **307/297,** 307/200, 325/381, 330/24
[51] **Int. Cl.** **H03k 1/12,** H03f 3/04
[50] **Field of Search** ..... 307/203, 207, 270, 200, 297, 313; 330/16, 17, 19, 20, 24, 25, 38 M; 325/381; 321/1—4

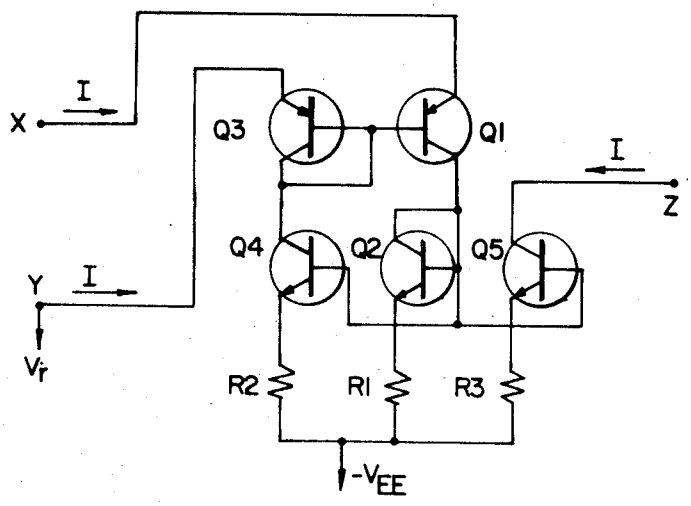
[56] **References Cited**

UNITED STATES PATENTS

3,320,551	5/1967	Miller	307/237X
3,392,344	7/1968	Meacham	330/24

Primary Examiner—Stanley D. Miller, Jr.
Attorney—James R. Hughes

ABSTRACT: A basic circuit comprising a first transistor having an input terminal for introduction of a current, an output connected to a diode-connected second transistor, and a control electrode connected to the control electrode of a diode-connected third transistor whose output is adapted for connection to a reference potential source and whose input is connected to the output of a fourth transistor, with the control electrodes of the second and fourth transistors interconnected and the output of the second and the input of the fourth transistors connected via equal resistors to a power supply source such that the current flowing in the first and second transistors is equally reproduced in the third and fourth transistors and a fifth transistor connected to extract a current equal to or related to these currents and to feed it to an output terminal.



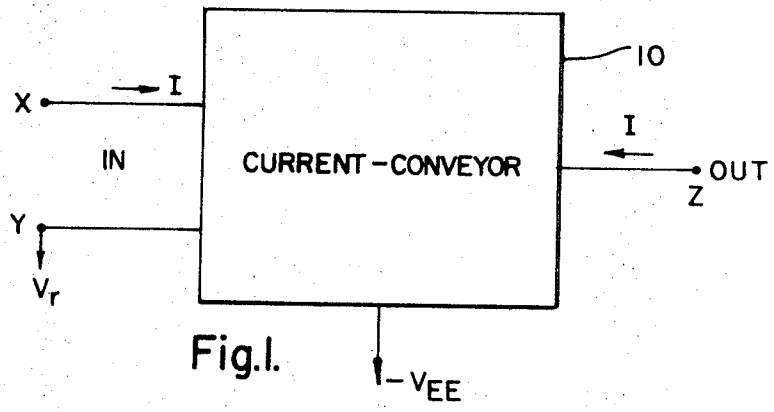


Fig.1.

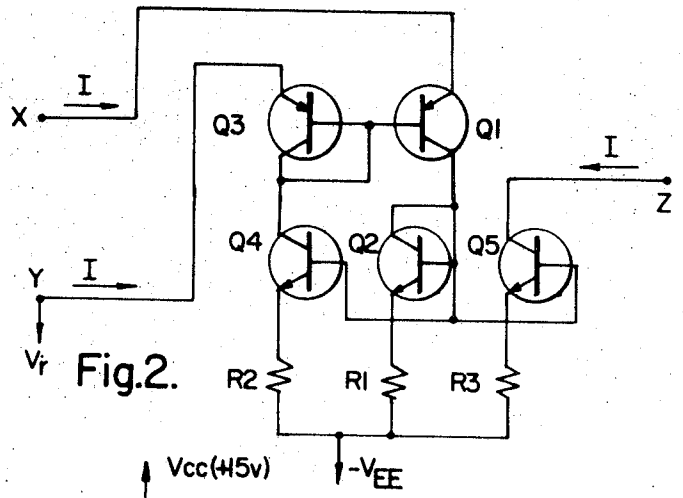


Fig.2.

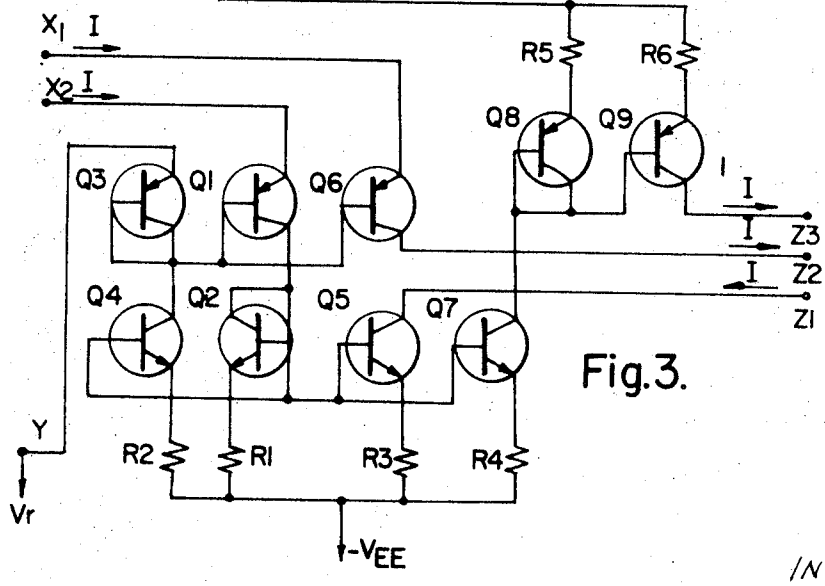


Fig.3.

INVENTORS
KENNETH C. SMITH
ADEL S. SEDRA
By J. R. Hughes
AGENT

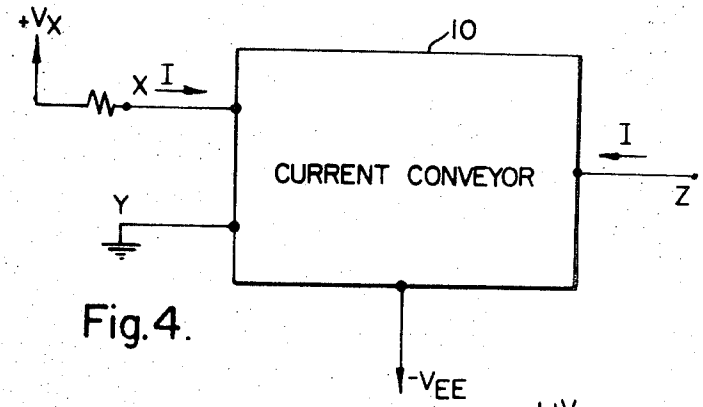


Fig.4.

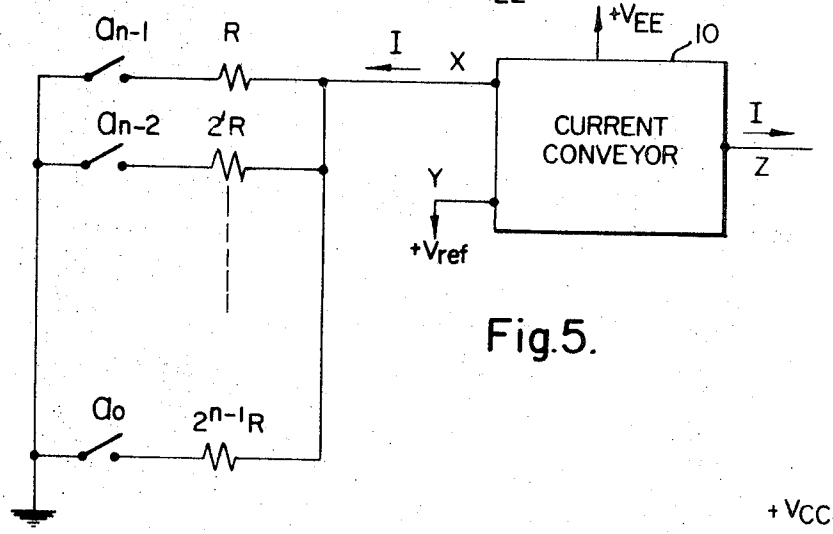


Fig.5.

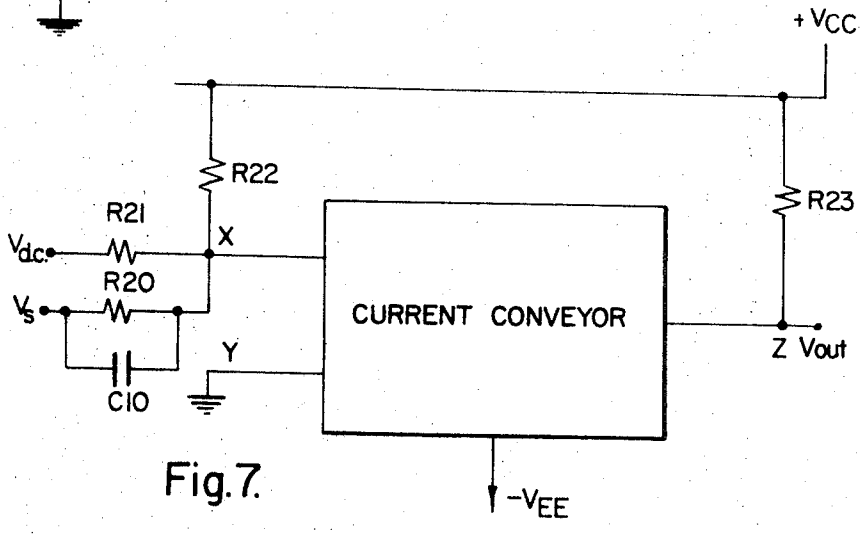


Fig.7.

INVENTORS
KENNETH C. SMITH
ADEL S. SEDRA
By J. K. Douglas
AGENT

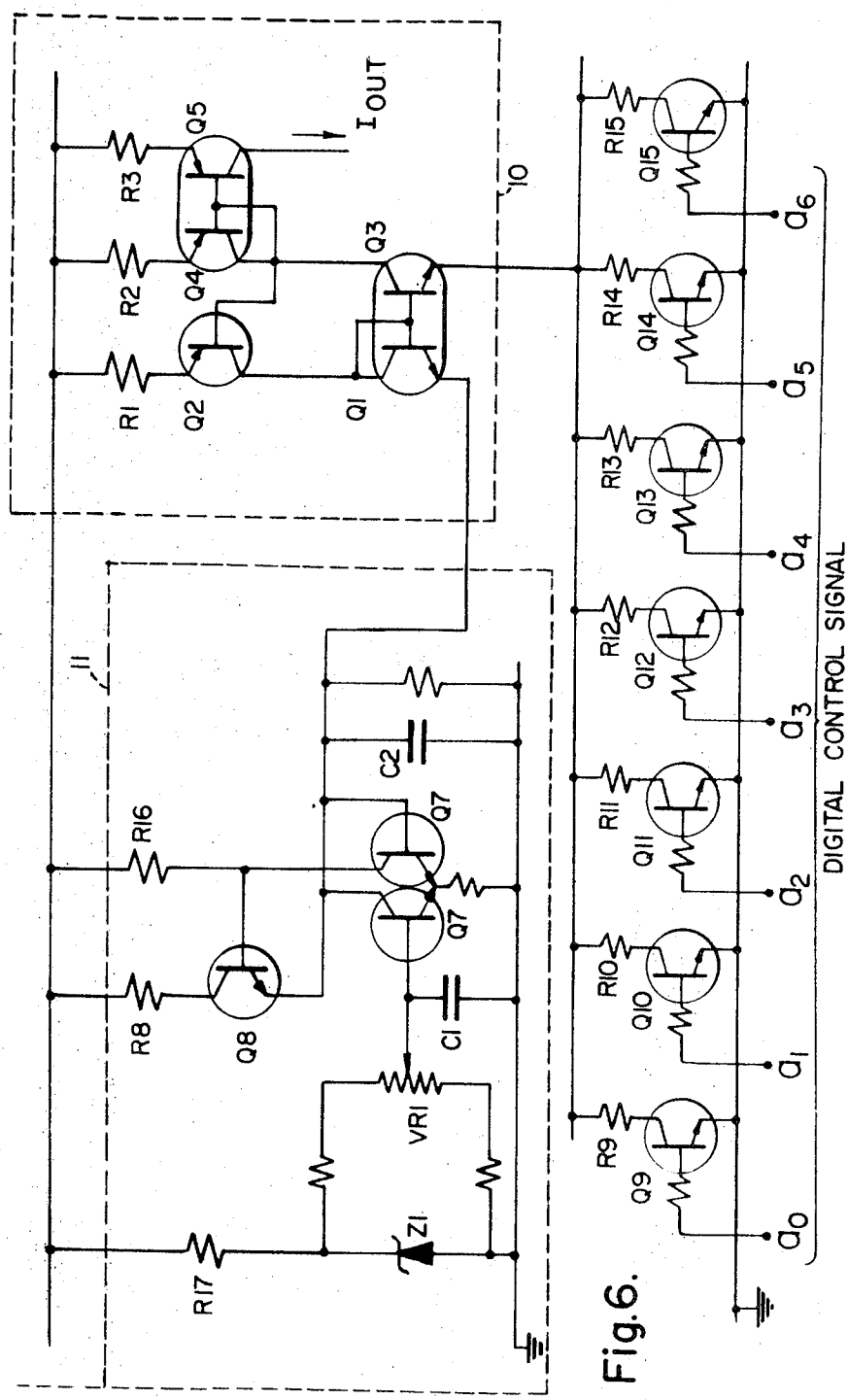


Fig.6.

INVENTORS
KENNETH C. SMITH
ADEL S. SEDRA
By J. R. Hughes
AGENT

CURRENT CONVEYOR WITH VIRTUAL INPUT REFERENCE POTENTIAL

This invention relates to a current conveyor circuit with virtual input reference potential and more particularly to a method and apparatus for accepting a current at one terminal and conveying it or a current related to it in a predetermined manner to an output terminal.

The invention described herein introduces a new electrical circuit principle or concept which will be referred to as "Current Conveying" and the circuit for doing this is called a "Current Conveyor." As the name implies the circuit accepts a current at one terminal and conveys it to another. A special input terminal sets a reference potential to which all other input terminals appear to be connected irrespective of the value of the input current. This gives the input the property of virtual zero input impedance and permits the forcing of any desirable input current which the circuit in turn conveys and reproduces at a high output impedance in the manner of an ideal current source. An additional property of the reference terminal is that its current is determined directly by the current through the input terminal irrespective of the value of the reference voltage. In this way, the reference terminal exhibits a virtual open circuit incremental characteristic. Morever the current in the reference terminal is in the same direction as the current in the input terminal and does not correspond to the polarity of the reference terminal voltage.

A more precise definition of circuit terminal properties can be obtained in terms of hybrid-h two-port parametric notation. The matrix relating the input terminal to the output terminal with the reference terminal held fixed is

$$H_{xz}=\begin{bmatrix}0 & 0\\ 1 & 0\end{bmatrix}$$

. The matrix relating the input terminal to the reference terminal with the output terminal held constant in potential is

$$H_{xy}=\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}$$

. The circuit described, because of its unique properties including that of an "impedance transformer" for currents and which therefore has some relation to the now conventional cathode and emitter follower configurations, is foreseen to have many and varied interesting applications some of which will be described below.

It is an object of the invention to provide a circuit method and apparatus for conveying a current accepted at one input terminal at a low including zero impedance level to an output terminal at a different impedance level.

It is another object of the invention to provide a current source that approaches the idealized state.

It is another object of the invention to provide a basic circuit building block that can be readily adapted, complemented, added to, or multiplied to obtain devices that can be used as, for example, a wide range current source, a digital to analog converter, a wideband current-measuring probe, a negative impedance converter, etc.

It is another object of the invention to provide a circuit that is reasonably well suited to integrated circuit production and that has very good temperature stability characteristics.

These and other objects of the invention are achieved by a basic circuit comprising a first transistor having an input terminal for introduction of a current, and output connected to a diode-connected second transistor, and a control electrode connected to the control electrode of a diode-connected third transistor whose output is adapted for connection to a reference potential source source and whose input is connected to the output of a fourth transistor, said second and fourth transistors having their control electrodes interconnected and the output of the second and the input of the fourth connected via equal resistors to a power supply source such that the current flowing in the first and second transistors is substantially equally reproduced in the third and fourth transistors and means for extracting a current equal to or related to these currents and feeding it to an output terminal. In actual practice the first and third transistors would be a matched pair, the second and fourth would be a matched pair, and the two resistors would also be matched. The current extractor means would preferably be a fifth transistor matched to the second and fourth having its control electrode connected to the control electrodes of the second and fourth transistors and its input connected via a matched resistor to the power supply such that its output will engender an output current that is a replica of the currents flowing through the second and fourth transistors.

In drawings which illustrate embodiments of the invention,

FIG. 1 is a block representation of the current conveyor,

FIG. 2 is a circuit implementation of the basic current conveyor,

FIG. 3 is a more complex form of the circuit of FIG. 2 which provides additional output terminals,

FIG. 4 shows in block form an adaptation and application of the device as a wide range current source,

FIG. 5 shows an adaptation of the device as a digital to analog converter,

FIG. 6 is a circuit representation of the device of FIG. 5, and

FIG. 7 shows an adaptation of the device as a wideband level shifter.

Referring to FIG. 1 a block representation of the current conveyor is shown generally as **10**. Terminals x and y are the input terminals and z is the output current source terminal. In its simplest form, the circuit requires only a single supply voltage ($-V_{EE}$). For some applications the y terminal is connected to a reference voltage V_r. An equal potential V_r (except for a negligible offset) will appear on the input terminal x. Having virtually established the potential of the input terminal x, it becomes easy to force the required amount of current I through x. An almost equal amount of current I will be supplied through the output terminal z at a high impedance level providing an almost idealized current source. It should be noted that the virtual potential appearing on terminal x will not be affected by the value of the current I. Hence, the device shows, in this sense, a zero input impedance and represents a virtual short circuit input characteristic. Also, as will be seen later, the circuit operation is independent, within limits, of the value of the supply voltage ($-V_{EE}$).

FIG. 2 is the circuit implementation to provide the characteristics of the block of FIG. 1. A first transistor Q1 has its input connected to the x terminal and its output connected to a diode-connected second transistor Q2 whose output is connected via a resistor R1 to a power supply source ($-V_{EE}$). The control electrode or base of Q1 is interconnected to the base of a diode-connected third transistor Q3 whose output is connected to terminal y. The input of Q3 is connected to the output of a fourth transistor Q4 whose input is connected via resistor R2 to the power supply ($-V_{EE}$) and whose control electrode is connected to the control electrode of Q2. It is preferable that Q1 and Q3 be a matched pair, Q2 and Q4 a matched pair, and R1 and R2 be matched resistors. It would be possible to replace Q2 and Q3 with diodes but this would make matching a much more difficult problem and it is standard practice to use diode-connected transistors as diodes especially in integrated circuit applications. A fifth transistor Q5 is used to extract a current equal to that in Q2 and Q4 and has its input connected via a third resistor R3, preferably matched to the others, to the power supply ($-V_{EE}$) and its control electrode connected to the control electrodes of Q2 and Q4. The output of this transistor Q5 actually provides an output current ($-I$) to terminal z that is equal to or closely related to input current I.

In operation, if a current I is forced through the emitter of transistor Q1, this current is sent to the diode-connected transistor Q2 and hence establishes the potential of its base. Assuming that Q2 and Q4 are a matched pair of high current gain (h_{FE} or β) transistors and that R1=R2, then Q4 will carry an equal current I (irrespective of the value of the negative supply voltage $-V_{EE}$). Q4 extracts this current I from the

diode-connected transistor Q3 which, if matched to Q1 will have a base-emitter drop equal to that of Q1. In this way, the emitter of Q1 will be held at a virtual potential equal to V_r irrespective of the value of the current I. As the potential of terminal x may thus be established at will, the current I can be easily forced through Q1 from standard sources. Q5 provides the necessary output current at terminal z which is an inflowing current I similar to that flowing into terminals x and y. A current conveyor complementary to the one shown in FIG. 2 with all current directions and voltage polarities reversed is also feasible.

FIG. 3 shows a circuit similar to that of FIG. 2 but has additions to provide for a complementary output current I on terminal z_2 and a current I at a higher voltage level on terminal z_3. In this circuit transistor Q7 extracts a current I and supplies to the "dual" arrangement of transistors Q8 and Q9 and resistors R5 and R6 which are connected to a positive supply voltage. Again the circuit operation is independent of supply voltage and an output current at a higher voltage level and reversed to that of FIG. 2 is obtained at terminal z_3. An output positive (complementary) current I is obtained at terminal z_2 via transistor Q6 connected to input terminal x_2. Terminal z_1 still provides the same output current as the circuit of FIG. 2. Following the same procedure, more output terminals can be provided. It may be noted that by using the complementary form of each transistor and reversed voltage polarities, a complementary circuit with reversed current directions can be provided and this may be useful for some applications.

The design depends upon matched pairs (and sometimes triples or quadruples) of transistors and resistors. The exact values of resistors used are not of primary importance. To provide for exact tracking of the various junction drops, the matched transistors should preferably be kept in the same environment. All the transistors should have a high current gain and in some applications involving AC signals should have low junction capacitances. Although in the prototype tested matched pairs of transistors in the same package were used, better results will definitely be obtained, if the circuit is integrated. The circuit is felt to be suitable for production with integrated circuit techniques due to the fact that it uses complementary transistors (PNP and NPN) hybrid circuit techniques are more suitable. However, improved economical techniques for producing high h_{FE} PNP and NPN transistors integrated on the same chip appear to be available shortly. The choice of resistor values should be made in connection with choosing the supply voltage values, on the basis of ensuring linear operation of all the transistors throughout the required current range, and at the same time providing sufficient voltage to mask second order variations in transistor junction drops. Reasonable choices are 1K for all resistors and +15 and −15 volts for the supply voltages. This conveniently provides currents from zero to over 10 *ma.*

FIG. 4 shows in block form an application of the basic concept as an accurate widerange current source. Terminal y is at ground level and thus terminal x will be held at virtual ground. The current I will be directly proportional to the control voltage V_x which provides current I via resistor R_x i.e., $I=V_x/R_x$.

FIG. 5 and FIG. 6 show a digital to analog converter or what is in essence a digitally controlled current source. This application makes use of the potential tracking of the input terminals. The current conveyor **10** shown is the complement of the device of FIGS. 1 and 2 and has input terminal y connected to reference supply $+V_{ref}$. Terminal x at the virtual potential of $+V_{ref}$, is connected to ground through a parallel series of binary weighted resistors 2^0R, 2^1R,.....,$2^{n1}R$. These resistors are switched in and out by switches a_o, a_1,.....a_{n1} which are controlled by an n bit digital signal with the decimal equivalent of P

$$I=P\left(\frac{V_{\text{ref}}}{2^{n-1}R}\right)$$

. FIG. 6 shows a complete circuit of such a system. The current conveyor **10** functions as described above and the circuitry in block **11** is required to stabilize V_{ref} against load variations. The switches comprise a series of transistors Q9 to Q15 with attendant resistors R9 to R15. These latter should be individually trimmed to compensate for any offset in the conveyor and for the saturation drops of the transistor switches.

FIG. 7 shows the application of the device as a wideband level shifter. This circuit accepts input signals (within certain limits) and DC levels (also within limits) and produces the sum of both. Terminal x which is at virtual ground is the summing point for a biasing current V_{cc}/R_{22}, the DC level V_{DC}, and the input signal V_s. The biasing current allows the circuit to handle bipolar inputs. By taking the output V_{out} across R23 (where R23=R22=R21=R20) the biasing is independent of the precise value of supply voltage $+V_{cc}$. The output of the circuit $V_{out}=V_s+V_{dc}$. The full circuit implementation can be readily put into effect and is not described further here. It should be noted that the level shifter will require an impedance transforming stage of unit voltage gain between the output terminal and the load to operate satisfactorily. Amplifiers of this type are available.

The Current Conveyor described can also be readily adapted to a negative impedance converter whose transfer characteristic is linear over a wide range and moreover is directly coupled with no offset, such that its graphical transfer characteristic passes through the origin. The fact that both current conveyor input terminals x and y (of FIGS. 1 and 2) draw currents in the same direction allows the use of the conveyor in this fashion. This is demonstrated by the hybrid-h matrix relating input to reference, namely,

$$H_{xy}=\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}$$

. For example, if in the circuit of FIG. 2, the output terminal is grounded and if V_r is a negative voltage changing towards zero, then the same voltage appears at terminal x. Thus if terminal x is connected via a resistor R_x (not shown) to ground, then as V_r increases the current I through x and hence through y decreases giving $V_r/I=-R_x$ or the negative impedance characteristic.

The circuits described above show the flexibility and wide adaptation and application of the basic current conveyor circuit. Other uses and modifications will suggest themselves to those skilled in this field.

We claim:

1. A current conveyor circuit for accepting a current at an input at low or zero impedance and providing an output current of the same or a related value at high impedance comprising:
   a. a first transistor having an input for introduction of a current,
   b. a diode connected second transistor whose input is connected to the output of the first transistor and whose output is connected via a first resistor to a voltage supply,
   c. a diode connected third transistor whose output is connected to a reference voltage terminal,
   d. a fourth transistor whose control electrode is connected to the control electrode of said second transistor and whose input is connected via a second resistor, equal in value to the first resistor, to the voltage supply, and whose output is connected to the input of said third transistor,
   e. the control electrode of the third transistor being connected to the control electrode of the first transistor, and
   f. a fifth transistor whose input is connected via a third resistor equal in value to the first and second resistors to the voltage supply, whose control electrode is connected to the control electrodes of the second and fourth transistors, and which supplies an output current to an output terminal equal in value to the current flowing in the second and fourth transistors.

2. A current conveyor as in claim 5 wherein the first and third transistors are a matched pair of high current gain transistors and the second and fourth transistors are a matched pair of high current gain transistors, and the first and second resistors are a matched pair of resistors.