The present invention provides an improvement on the use of flexible circuit connectors for electrically coupling IC devices to one another in a stacked configuration by use of the flexible circuit to provide the connection of the stacked IC module to other circuits. Use of the flexible circuit as the connection of the IC module allows the flexible circuit to provide strain relief and allows stacked IC modules to be assembled with a lower profile than with previous methods. The IC module can be connected to external circuits through the flexible circuit connectors by a variety of means, including solder pads, edge connector pads, and socket connectors. This allows for IC devices to occupy less space than with previous methods, which is beneficial in modules such as memory modules with multiple, stacked memory devices.
STACKED INTEGRATED CIRCUIT MODULE

RELATED APPLICATIONS

[0001] This application is a divisional of U.S. patent application Ser. No. 11/330,307, filed Jan. 11, 2006, which is hereby incorporated by reference herein.

TECHNICAL FIELD

[0002] This invention relates to stacking ledged integrated circuit devices and, in particular, to stacks and stacking integrated circuits in leaded packages.

BACKGROUND

[0003] A variety of systems and techniques are known for stacking packaged integrated circuits. Some techniques are devised for stacking chip-scale packaged devices (CSPs) while other systems and methods are better directed to leaded packages such as those that exhibit a set of leads extending from at least one lateral side of a typically rectangular package.

[0004] Memory devices are packaged in both chip-scale (CSP) and leaded packages. However, techniques for stacking CSP devices are typically not optimum for stacking leaded devices. Although CSP devices are gaining market share, in many areas, integrated circuits continue to be packaged in high volumes in leaded packages. For example, the well-known flash memory integrated circuit is typically packaged in a leaded package with finned-pitch leads emerging from one or both sides of the package. A common package for flash memory is the thin small outline package, commonly known as the TSOP typified by leads emerging from one or more (typically a pair of opposite sides) lateral sides of the package. Thin small outline packages, commonly known as the TSOP typified by leads emerging from one or more (typically a pair of opposite sides) lateral sides of the package.

[0005] The assignee of the present invention, Staktek Group L.P., has developed a wide variety of techniques, systems and designs for stacks and stacking with both leaded and CSP devices. In leaded package stacking, Staktek Group L.P. has developed, for example, U.S. Pat. No. 6,572,387 issued Jun. 3, 2003 and U.S. patent application Ser. No. 10/449,242 published as Pub. No. 2003/0203663 A1 which disclose and claim various techniques and apparatus related to stacking leaded packages.

[0006] Many other techniques have been developed for interconnecting the leads of the stacked devices. For example, U.S. Pat. No. 4,696,525 to Collier et al. purports to teach a socket connector for coupling adjacent devices in a stacked configuration to one another. The socket has external conductors that interconnect leads from like, adjacent devices to one another. Sockets, however, are limited in several respects. They are not versatile in their ability to implement complex interconnections. In addition, such sockets, which have relatively thick, plastic bodies, act as thermal insulators between upper and lower package surfaces, and inhibit the module's overall ability to dissipate heat.

[0007] Although the art has many techniques for stacking leaded devices, a new system and method for stacking leaded package devices is a welcome development. Accordingly, the present application discloses improved systems and methods for electrically and thermally coupling adjacent integrated circuit devices in stacked modules.

SUMMARY OF THE INVENTION

[0008] The present invention provides a system and method for stacks and stacking leaded package IC's packages. A flex circuit is disposed between leaded IC's to be stacked. In a preferred embodiment, leads of constituent leaded IC packages are configured to allow the lower surface of the leaded IC packages to contact the surface of the flex circuitry that provides connection between an upper and lower leaded IC package. In an optional embodiment, a part of the flex circuitry emerges from between the leaded IC's and provides a connective facility for connection to external or application environments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is an exploded view of a stacked module devised in accordance with a preferred embodiment of the present invention.

[0010] FIG. 2 is a side view of a stacked module devised in accordance with a preferred embodiment of the present invention.

[0011] FIG. 3 is a plan view of one side of a flex circuit in accordance with an embodiment of the present invention.

[0012] FIG. 4 is a plan view of another side of a flex circuit in accordance with an embodiment of the present invention.

[0013] FIG. 5 depicts the area marked “A” in FIG. 2.

[0014] FIG. 6 is a side view of a stacked module in accordance with an alternative preferred embodiment of the present invention.

[0015] FIG. 7 is a plan view of a stacked module in accordance with an alternative preferred embodiment of the present invention.

[0016] FIG. 8 is a plan view of a stacked module in accordance with another alternative preferred embodiment of the present invention.

[0017] FIG. 9 is a plan view of a stacked module in accordance with another alternative preferred embodiment of the present invention.

[0018] FIG. 10 is a plan view of another side of a stacked module in accordance with another alternative preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0019] FIG. 1 is an exploded view of an exemplar stacked module 10 devised in accordance with a preferred embodiment of the present invention. Exemplar module 10 is comprised of leaded IC's 20 and 22 each having upper and lower sides or surfaces 23 and 25, respectively, and lateral sides S1 and S2 which, as those of skill will recognize, may be in the character of edges or sides and need not be perpendicular in aspect to the upper and lower surfaces 23 and 25. Leads 24 are emergent from sides S1 and S2. In a preferred embodiment, leads 24 are deflected to remain within the space defined by planes PL and PU defined by lower surfaces 25 and 23 respectively of the respective IC's to allow the lower surfaces 25 of each of the respective leaded packaged IC's to be in contact with the respective surfaces 15 and 17 of flex circuit 12 when the IC's are connected to the flex. In this disclosure, contact between the lower surface 25 of a leaded IC and the surfaces of flex circuit 12 includes not only direct contact between surface or side 25 and flex but shall include those instances
where intermediate materials such as adhesive is used between the respective leaded IC and flex.

[0020] The present invention may also be employed with circuitry other than or in addition to memory such as the flash memory depicted in a number of the present Figs. Other exemplary types of circuitry that may be aggregated in stacks in accordance with embodiments of the invention include, just as non-limiting examples, DRAMs, FPGAs, and system stacks that include logic and memory as well as communications or graphics devices. It should be noted, therefore, that the depicted profile for ICs 20 and 22 is not a limitation and that upper and lower leaded ICs 20 and 22 respectively need not be TSOPs or TSOP-like and the packages employed may have more than one die or leads emergent from one, two, three or all sides of the respective package body. For example, a module 10 in accordance with embodiments of the present invention may employ leaded ICs 20 and 22 that have more than one die within each package and may exhibit leads emergent from only one side of the package. In such cases, adhesives will typically be employed between the IC and flex circuit. Further, a module 10 in accord with the present invention need not have two ICs as the invention may be employed to devise a stacked module 10 with two or more ICs as those of skill will understand after appreciating this disclosure. Further, techniques disclosed herein may be employed to stack a leaded IC in a leaded-CSP combination stack.

[0021] In the depicted preferred embodiment, flex circuit 12 (e.g., "flex", "flex circuitry", "flex circuit" etc.) is disposed between leaded ICs 20 and 22 and exhibits a first side 15 having two pluralities of connective sites 34 and 36 adapted for connection to a leaded IC and, in this embodiment, another optional plurality of connective sites 32. Flex circuit 12 also exhibits a second side 17 having two pluralities of connective sites 44 and 46. Those of skill will recognize that flex circuit 12 may be comprised from traditional flexible circuitry or, in some of the alternative embodiments, what is sometimes called rigid-flex may be employed. Such rigid flex exhibits rigid areas and flexible areas to provide an interconnection function required of flex circuit 12 in the present invention.

[0022] Pluralities 34 and 36 and 44 and 46 of connective sites are adapted for connection to the leads of leaded packages IC 20 and IC 22, respectively, each of which has a plurality, individual ones of which sites are identified as S1 and S2. Optional third plurality of connective sites 32 is adapted for connection of module 10 to an external circuit or environment.

[0023] Plural leads 24 are emergent from at least one of the plural sides of the ICs and typically, a plurality of leads 24 is emergent from one of the plural sides of each of the ICs 20 and 22 and a second plurality of leads 24 is emergent from another one of the plural sides of each of ICs 20 and 22. Lead ed ICs 20 and 22 are connected to flex circuit 12 through the leads 24 of leaded ICs 20 and 22. As those of skill will recognize, many techniques exist for connecting the leads of leaded ICs 20 and 22 to the connective sites. Such techniques include, as a non-limiting example, use of solder or other conductive attachment. Other forms of bonding other than solder between the connecting sites and leads 24 may also be employed (such as brazing or welding for example) but soldering techniques are well understood and adapted for use in large scale manufacturing.

[0024] FIG. 2 depicts a side perspective view of a stacked module 10 devised in accordance with a preferred embodiment of the present invention. As depicted, lower side 25 of each of leaded ICs 20 and 22 are adjacent to sides 15 and 17 respectively, of flex circuit 12. To realize the adjacent and, preferably, contact (touching) relationship between the lower side 25 of a selected leaded IC and the respective flex circuit side, leads 24 typically require modification or reconfiguration which is preferably performed before mounting of the leaded IC to flex circuit 12. Those of skill will note that a preferred method for reconfiguration of leads 24 comprises use of a jig to fix the position of body 29 of the respective leaded IC and, preferably, support the lead at the point of emergence from the body at sides S1 and S2 of leaded ICs 20 and 22 before deflection of the respective leads toward the upper plane PU to confine leads 24 to the space between planes PL and PU of the respective leaded IC as earlier shown in FIG. 1. This is because typically, leaded ICs such as TSOPs are configured with leads that extend beyond the lower plane PL. In order for the lower surface 25 of the respective leaded packaged ICs to contact (either directly or through an adhesive or thermal intermediary) the respective surfaces of the flex circuit, the leads 24 must be typically reconfigured.

[0025] FIG. 3 depicts a plan view of side 15 of the flex circuit. As depicted, side 15 exhibits three pluralities of connective sites, 32, 34, and 36, each comprised of individual connective sites 32C, 34C, and 36C, respectively. First and second pluralities 34 and 36 are adapted for connection to leaded IC 20 through leads 24, with optional plurality of connective sites 32 being adapted for connecting module 10 to an external circuit or environment.

[0026] FIG. 4 depicts a plan view of side 17 of flex circuit 12. As depicted, side 17 exhibits two pluralities of connective sites 44 and 46 respectively, each comprised of multiple connective sites 44C and 46C, respectively, these sites being adapted for connection to leaded IC 22 through leads 24.

[0027] FIG. 5 depicts the area identified by “A” in earlier FIG. 2. As depicted, the standard lead shape is modified or reconfigured to reduce the profile X of module 10 as lower surfaces 25 of leaded ICs 20 and 22 are adjacent to and, preferably, in contact with surfaces 15 and 17, respectively, of flex circuit 12. Profile X is the distance between respective upper planes PU20 and PU22. Leads 24 of leaded ICs 20 and 22 are preferably configured to allow leaded ICs 20 and 24 to be in either direct or indirect (through intermediary adhesive for example) contact with flex 12.

[0028] Leads 24 of leaded ICs 20 and 22 employed in an exemplar module 10 are shown in contact with connective sites 34C and 44C, for example, while lower surface 25 of the leaded ICs 20 and 22 are in contact with the respective sides 15 and 17 of flex circuit 12.

[0029] FIG. 6 depicts an exemplar module 10 having connective sites 32 for connection to an external circuit or environment. Those of skill will recognize that when a third plurality of connective sites such as the depicted reference 32 are employed, they may be disposed on either side 15 or 17 of flex circuit 12. In this depiction, adhesive 33 is shown between lower surfaces 25 and respective sides of flex circuit 12.

[0030] FIG. 7 illustrates that, in devising a module in accordance with the present invention, some embodiments may be constructed where connective sites 32 take the form of edge connector pads for connection with an edge connector such as, for example, those typically found in computer applications for memory expansion.
FIG. 8 illustrates a plan view of an exemplar module 10 in accordance with an alternative preferred embodiment of the present invention. FIG. 8 employs a socket connector as the third plurality of connective sites 32 for connecting stacked module 10 to an external circuit or environment.

FIG. 9 illustrates a module 10 in accordance with an alternative preferred embodiment of the present invention, showing alternative arrangements of the pluralities of connection sites on side 15 of the flex circuit. In the depiction of FIG. 9, the first and second pluralities of connective sites are oriented in a first direction while the third plurality of connective sites for connection of the circuit module to an application environment are oriented in a direction perpendicular to the orientation of the first and second pluralities of connective sites.

FIG. 10 is a plan view of another side of the stacked module depicted in FIG. 9, sharing alternative arrangements of the pluralities of connective sites on side 17 of the flex circuit.

It will be seen by those skilled in the art that many embodiments taking a variety of specific forms and reflecting changes, substitutions, and alternations can be made without departing from the spirit and scope of the invention. Therefore, the described embodiments illustrate but do not restrict the scope of the claims.

1. A method for devising a circuit module comprising the steps of:
   - providing first and second leaded packaged integrated circuits each with upper and lower major surfaces and leads emergent from first and second peripheral sides of the respective packages;
   - providing a flex circuit along the first surface of which are disposed first and second pluralities of connective sites and along the second major surface of which are disposed first and second pluralities of connective sites; and
   - reconfiguring the leads of the first and second leaded packaged integrated circuits so as to confine the leads to a space defined by first and second planes defined by the upper and lower major surfaces of the respective packages;
   - attaching the leads emergent from the first peripheral side of the first leaded packaged integrated circuit to the first plurality of connective sites of the first major surface of the flex circuit and attaching the leads emergent from the second peripheral side of the first leaded packaged integrated circuit to the second plurality of connective sites of the first major surface of the flex circuit so as to realize contact between the lower major surface of the first leaded packaged integrated circuit and the first major surface of the flex circuit and connecting the second leaded packaged integrated circuit to the first and second pluralities of connective sites of the second major surface of the flex circuit.

2. The method of claim 1 in which the flex circuit provided exhibits a third plurality of connective sites for connection of the circuit module to an application environment.

3. The method of claim 1 in which an adhesive is disposed between the lower major surface of the first leaded packaged memory circuit and the first major surface of the flex circuit.

4. The method of claim 2 in which the third plurality of connective sites is configured for connection to an edge connector.

5. The method of claims 1 in which the first and second leaded packaged integrated circuits are flash memory circuits.

* * * * *