

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
14 February 2002 (14.02.2002)

PCT

(10) International Publication Number
WO 02/012995 A3

(51) International Patent Classification⁷: **G06F 7/60**,
7/50, 7/52, 17/50

(21) International Application Number: PCT/GB01/03415

(22) International Filing Date: 27 July 2001 (27.07.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0019287.2 4 August 2000 (04.08.2000) GB
0101961.1 25 January 2001 (25.01.2001) GB

(71) Applicant (for all designated States except US): **AUTO-MATIC PARALLEL DESIGNS LIMITED** [GB/GB];
7200 The Quorum, Oxford Business Park, Oxford, Ox-fordshire OX4 2JZ (GB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **MEULEMANS**,

Peter [NL/GB]; 1 Latham Road, Coventry CV5 6HR (GB). **RUMYNIN, Dmitriy** [GB/RU]; 258 Sir Henry Parkes Road, Coventry CV4 8GG (RU). **TALWAR, Sunil** [GB/GB]; 26a Binswood Avenue, Leamington Spa, Warwickshire CV32 5SQ (GB).

(74) Agent: **COLLINS, John, David**; Marks & Clerk, 57-60 Lincoln's Inn Fields, London WC2A 3LS (GB).

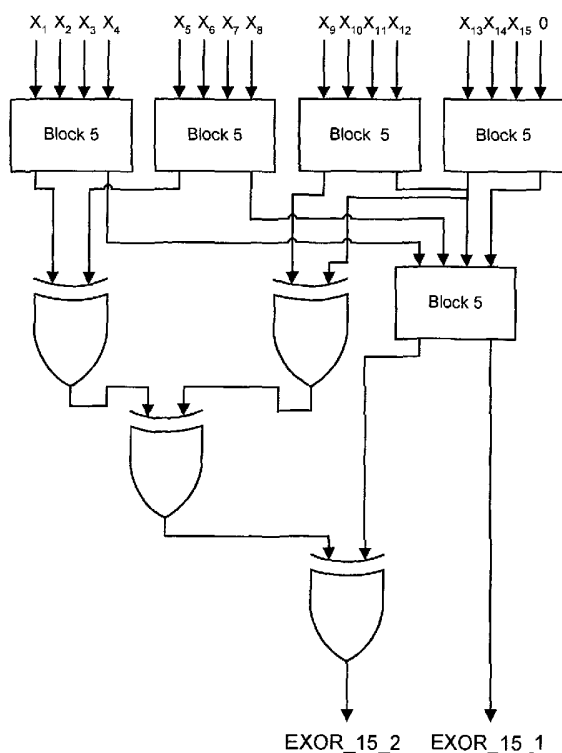
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European

[Continued on next page]

(54) Title: A PARALLEL COUNTER AND A LOGIC CIRCUIT FOR PERFORMING MULTIPLICATION

BLOCK 6



(57) Abstract: A logic circuit such as a parallel counter comprises logic for generating output bits as elementary symmetric functions of the input bits. The parallel counter can be used in a multiplication circuit. A multiplication circuit is also provided in which an array of combinations of each bit of a binary number with each other bit of another binary number is generated having a reduced form in order to reduce the steps required in array reduction.



patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(88) Date of publication of the international search report:

13 March 2003

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 01/03415

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F7/60 G06F7/50 G06F7/52 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, COMPENDEX, IBM-TDB, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 757 098 A (WRIGHT C) 4 September 1973 (1973-09-04) figure 2 ---	1,2, 6-10, 16-19, 43-45, 48-57, 61-65, 78,79, 83-87, 93-96, 120-122
X	US 5 175 862 A (WOODSMANSEE MICHAEL A ET AL) 29 December 1992 (1992-12-29) figure 3 --- -/--	1-3, 78-80,82



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

A document defining the general state of the art which is not considered to be of particular relevance

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L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

Z document member of the same patent family

Date of the actual completion of the international search

18 October 2002

Date of mailing of the international search report

14 11 2002

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Verhoof, P

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 01/03415

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 634 658 A (BROWN RICHARD R) 11 January 1972 (1972-01-11) figure 3 ---	1-3, 10, 16, 19, 20, 43-45, 48-57, 61-70, 78-80, 83, 87, 93, 96, 97, 120-122
X	US 5 524 082 A (HORSTMANN PAUL W ET AL) 4 June 1996 (1996-06-04) figure 4 ---	123-132
A	DRECHSLER R ET AL: "Sympathy: fast exact minimization of fixed polarity Reed-Muller expressions for symmetric functions" IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, JAN. 1997, IEEE, USA, vol. 16, no. 1, pages 1-5, XP002217407 ISSN: 0278-0070 page 2, right-hand column, paragraph 3 - paragraph 6; table IV ---	123-132
A	EP 0 168 650 A (IBM) 22 January 1986 (1986-01-22) figure 2 ---	123-132
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A	DRECHSLER R ET AL: "Sympathy: fast exact minimization of fixed polarity Reed-Muller expressions for symmetric functions" EUROPEAN DESIGN AND TEST CONFERENCE, 1995. ED&TC 1995, PROCEEDINGS. PARIS, FRANCE 6-9 MARCH 1995, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 6 March 1995 (1995-03-06), pages 91-97, XP010148035 ISBN: 0-8186-7039-8 abstract --- -/--	133, 136, 139, 142

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 01/03415

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 023 566 A (ROY SUMIT ET AL) 8 February 2000 (2000-02-08) column 5, line 26 - line 34; figure 3C ---	145-151
X	NIENHAUS H A: "Efficient multiplexer realizations of symmetric functions" IEEE SOUTHEASTCON 1981 CONFERENCE PROCEEDINGS, HUNTSVILLE, AL, USA, 5-8 APRIL 1981, pages 522-525, XP010277476 1981, New York, NY, USA, IEEE, USA page 522, right-hand column, line 1 -page 524, right-hand column, line 25 ---	145-151
X	EP 0 309 292 A (MATSUSHITA ELECTRIC IND CO LTD) 29 March 1989 (1989-03-29) page 9, line 11 - line 26; figure 11 ---	145-151
X	CHAKRABORTY S ET AL: "Synthesis of symmetric functions for path-delay fault testability" VLSI DESIGN, 1999. PROCEEDINGS. TWELFTH INTERNATIONAL CONFERENCE ON GOA, INDIA 7-10 JAN. 1999, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 7 January 1999 (1999-01-07), pages 512-517, XP010320035 ISBN: 0-7695-0013-7 page 513 -page 514 -----	145-151

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB 01/03415

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☒ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
1-10, 16-20, 43-45, 47-57, 61-70, 78-87, 93-97, 120-142, 145-151
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/SA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-10,16-20,43-45,47-57,61-70,78-87,93-97,120-122

A parallel counter with a specific AND/EXOR or AND/OR combination

2. Claims: 11-15,46,88-92

A parallel counter with selector logic

3. Claims: 21-42,71-77,98-119

A hierarchy of logical modules with intermediate outputs

4. Claims: 58-60

A logic circuit for multiplying, comprising array deformation

5. Claims: 123-132

Threshold logic function design, identifying pairs of logic elements reducable to one threshold logic function

6. Claims: 133-142

Logic circuit design replacing exclusive OR logic with OR logic

7. Claims: 145-151

Logic circuit design using inversion of a symmetric function for performing another symmetric function

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/GB 01/03415

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